Data Transmission Circuit and Method, and Memory device

Cross References to Related Applications

[0001] This application claims the benefit of priority to Chinese patent application CN2021103366255 filed with the Chinese Patent Office on March 29, 2021, entitled "Data Transmission Circuit and Method, and Memory device" the content of the application is incorporated herein by reference in its entirety.

Technical Field

[0002] This disclosure relates to, but is not limited to, to a data transmission circuit and method, and a memory device.

Background

[0003] A semiconductor memory device generally includes a memory array region and a peripheral circuit region. The memory array region is provided with a memory cell array including a plurality of memory cells; the peripheral circuit region is provided with a control circuit for controlling reading and writing functions and a mode register for storing mode register data. The mode register data stored in the mode register can be read out by issuing a read command of the mode register.

~~**[0004]** If operating parameter requirements of a particular type of the semiconductor memory device are met, a time of responding to a read command of the mode register to read data of the mode register is set to match a time of responding to a read command of the array region to read data of the array region, to realize a transmission path of the read command of the mode register to read the data of the mode register, which is the same as a transmission path timing of the data of the array region in response to the data read command of the array region.~~

Summary

~~**[0005]**~~**[0004]** A first aspect of the present disclosure provides a data transmission circuit, including a data memory unit of a mode register, and a data memory unit of an array region. The data memory unit of the mode register is configured to output data of the mode register in response to a first clock signal; an output terminal of the data memory unit of the mode register and an output terminal of the data memory unit of the array region are both connected to a first node. The data memory unit of the array region is configured to receive data of the array region in response to a first pointer signal, and is further configured to output the data of the array region in response to a second pointer signal.

~~**[0006]**~~**[0005]** In the data transmission circuit of the above embodiment, the data memory unit of the mode register is configured to output the data of the mode register in response to the first clock

signal, and the output terminal of the data memory unit of the array region and the output terminal of the data memory unit of the mode register are both connected to the first node, which is used to receive data of the array region in response to the first pointer signal, and to output data of the array region in response to the second pointer signal, to realize different control of the data memory unit of the mode register and the data memory unit of the array region, so that a response time for the readout of the data of the mode register in response to a read command of the mode register matches a response time for the readout of the data of the array region in response to a data read command of the array region, so as to precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn.

~~[0007]~~[0006] A second aspect of the disclosure provides a data transmission circuit, including a controllable delay module, a data processing unit of a mode register, a data memory unit of an array region, and a data memory unit of the mode register. The controllable delay module is configured to generate a preset read latency signal in response to a read command of the mode register. The data processing unit of the mode register is connected to the controllable delay module, and is used to read mode register data from the mode register in response to the read command of the mode register, and is also configured to output the mode register data to the data memory unit of the mode register in response to the preset read latency signal; the output terminal of the data memory unit of the array region and the output terminal of the data memory unit of the mode register are both connected to a first node, and are used to receive data of the array region in response to a first pointer signal, and also configured to output the data of the array region in response to a second pointer signal; and the data memory unit of the mode register is configured to output the data of the mode register in response to a first clock signal.

~~[0008]~~[0007] In the data transmission circuit in the above embodiment, the controllable delay module is set to generate the preset read latency signal in response to the read command of the mode register, so that the data processing unit of the mode register can read the data of the mode register from the mode register in response to the read command of the mode register, and output the data of the mode register to the data memory unit of the mode register in response to the preset read latency signal. The data memory unit of the mode register is set to output the data of the mode register in response to the first clock signal, and the output terminal of the data memory unit of the array region and the output terminal of the data memory unit of the mode register are both connected to the first node, and the data memory unit of the array region can receive the data of the array region in response to the first pointer signal and output the data of the array region in response to the second pointer signal, so as to realize different control between the data memory unit of the mode register and the

data memory unit of the array region, so that a time of responding to a read command of the mode register to read data of the mode register can match a time of responding to a read command of the array region to read data of the array region, to precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn. Once the operation delay of the controllable delay module in this disclosure is determined, it is less affected by changes in the working environment, which can effectively avoid control errors in the data transmission path due to the influence of the working environment; and the operation delay of the controllable delay module can be controlled and adjusted, which can meet the operating parameter requirements of different types of semiconductor memory devices.

~~[0009]~~[0008] A third aspect of the disclosure provides a data transmission circuit, including a delay module, a data processing unit of a mode register, a data memory unit of an array region, and a data memory unit of the mode register. The delay module is configured to generate a preset read latency signal after delaying a first preset time from a moment of receiving a read command of the mode register. The data processing unit of the mode register is connected to the delay module, and is configured to read data of the mode register from the mode register in response to the read command of the mode register, and is also configured to output the data of the mode register to the data memory unit of the mode register in response to the preset read latency signal. An output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node, to receive data of the array region in response to a first pointer signal, and to output data of the array region in response to a second pointer signal. The data memory unit of the mode register is configured to output data of the mode register in response to a first clock signal.

~~[0010]~~[0009] In the data transmission circuit according to the above embodiment, the delay module is set to generate the preset read latency signal after delaying the first preset time from the moment of receiving the read command of the mode register, so that the data processing unit of the mode register can read the data of the mode register from the mode register in response to the read command of the mode register, and output the data of the mode register to the data memory unit of the mode register in response to the preset read latency signal. The data memory unit of the mode register is set to output the data of the mode register in response to the first clock signal. The output terminal of the data memory unit of the array region and the output terminal of the data memory unit of the mode register are both connected to the first node. The data memory unit of the array region can receive data of the array region in response to the first pointer signal and output the data of the array region in response to the second pointer signal, so as to realize different control between the data

memory unit of the mode register and the data memory unit of the array region, so that a time of responding to a read command of the mode register to read data of the mode register can match a time of responding to a read command of the array region to read data of the array region, to precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn.

~~[0011]~~[0010] A fourth aspect of the present disclosure provides a memory device, including a memory cell array, a mode register, and any of the data transmission circuits described in the embodiments of the present disclosure. The memory cell array is configured to store data of the array region, and the mode register is configured to store data of the mode register. In this embodiment, a time of responding to a read command of the mode register to read the data of the mode register matches a time of responding to a read command of the array region to read data of the array region, and a timing sequence of a transmission path of responding to the read command of the mode register to read the mode register data is the same as a timing sequence of a transmission path of responding to the read command of the array region to read out the data of the array region.

~~[0012]~~[0011] A fifth aspect of the present disclosure provides a data transmission method, including the following.

~~[0013]~~[0012] A data memory unit of a mode register outputs data of the mode register in response to a first clock signal.

~~[0014]~~[0013] A data memory unit of an array region receives data of the array region in response to a first pointer signal, and outputs the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

~~[0015]~~[0014] The sixth embodiment of this disclosure provides a data transmission method, including the following.

~~[0016]~~[0015] A controllable delay module generates a preset read latency signal in response to a read command of a mode register.

~~[0017]~~[0016] A data processing unit of the mode register reads data of the mode register in response to a read command of the mode register, and outputs the data of the mode register to a data memory unit of the mode register in response to a preset read latency signal.

~~[0018]~~[0017] The data memory unit of the mode register outputs the mode register data in response to a first clock signal.

~~[0019]~~[0018] A data memory unit of the array region receives data of the array region in response to a first pointer signal, and outputs the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

~~[0020]~~[0019] The seventh embodiment of the present disclosure provides a data transmission method, including the following.

~~[0021]~~[0020] A delay module generates a preset read latency signal after delaying a first preset time from a moment of receiving a read command of the mode register.

~~[0022]~~[0021] A data processing unit of the mode register reads data of the mode register from the mode register in response to a read command of the mode register, and outputs the mode register data to a data memory unit of the mode register in response to a preset read latency signal.

~~[0023]~~[0022] A data memory unit of the mode register outputs data of the mode register in response to a first clock signal.

~~[0024]~~[0023] A data memory unit of the array region receives data of the array region in response to a first pointer signal, and outputs the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit in the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

Brief Description of the Drawings

~~[0025]~~[0024] To more clearly describe the embodiments of the present disclosure, the following will briefly introduce the drawings in the description of the embodiments. The drawings in the following description illustrate embodiments of the present disclosure. For those of ordinary skill in the art, other drawings can be obtained based on these drawings without creative work.

~~[0026]~~[0025] FIG. 1 is a structural block diagram of a data transmission circuit provided according to a first embodiment of this disclosure;

~~[0027]~~[0026] FIG. 2 is a structural block diagram of a data transmission circuit provided according to a second embodiment of this disclosure;

~~[0028]~~[0027] FIG. 3 is a structural block diagram of a data transmission circuit provided according to a third embodiment of this disclosure;

~~[0029]~~[0028] FIG. 4 is a structural block diagram of a data transmission circuit provided according to a fourth embodiment of this disclosure;

~~[0030]~~[0029] FIG. 5a is a structural block diagram of a data transmission circuit provided according to a fifth embodiment of this disclosure;

~~[0031]~~[0030] FIG. 5b is a structural block diagram of a data transmission circuit provided according to a sixth embodiment of this disclosure;

~~[0032]~~[0031] FIG. 6 is a structural block diagram of a first-in first-out data processing unit in a data transmission circuit provided according to an embodiment of the disclosure;

~~[0033]~~[0032] FIG. 7 is a structural block diagram of a first-in first-out data processing unit in a data transmission circuit provided according to another embodiment of the disclosure;

~~[0034]~~[0033] FIG. 8a is a structural block diagram of a data transmission circuit provided according to a seventh embodiment of this disclosure;

~~[0035]~~[0034] FIG. 8b is a structural block diagram of a data transmission circuit provided according to an eighth embodiment of this disclosure;

~~[0036]~~[0035] FIG. 8c is a structural block diagram of a data transmission circuit provided according to a ninth embodiment of this disclosure;

~~[0037]~~[0036] FIG. 8d is a structural block diagram of a data memory unit of an array region in a data transmission circuit provided according to an embodiment of the disclosure;

~~[0038]~~[0037] FIG. 8e is a structural block diagram of a data transmission circuit provided according to a tenth embodiment of this disclosure;

~~[0039]~~[0038] FIG. 8f is a structural block diagram of a data transmission circuit provided according to an eleventh embodiment of this disclosure;

~~[0040]~~[0039] FIG. 8g is a schematic diagram of an embodiment of FIG. 8f;

~~[0041]~~[0040] FIG. 9a is a structural block diagram of a data transmission circuit provided according to a twelfth embodiment of this disclosure;

~~[0042]~~[0041] FIG. 9b is a structural block diagram of a data transmission circuit provided according to a thirteenth embodiment of this disclosure;

~~[0043]~~[0042] FIG. 9c is a structural block diagram of a data transmission circuit provided according to a fourteenth embodiment of this disclosure;

~~[0044]~~[0043] FIG. 9d is a structural block diagram of a data transmission circuit provided according to a fifteenth embodiment of this disclosure;

~~[0045]~~[0044] FIG. 9e is a structural block diagram of a data transmission circuit provided according to a sixteenth embodiment of this disclosure;

~~[0046]~~[0045] FIG. 9f is a schematic diagram of an embodiment of FIG. 9e;

~~[0047]~~[0046] FIG. 10a is a schematic diagram of a timing sequence of a data transmission circuit responding to a read command according to an embodiment of the disclosure;

~~[0048]~~[0047] FIG. 10b is a schematic diagram of an operating timing sequence of a data transmission circuit provided according to an embodiment of the disclosure;

~~[0049]~~[0048] FIG. 11a is a structural block diagram of a delay circuit for responding to a read command of the mode register;

~~[0050]~~[0049] FIG. 11b is a schematic diagram of the operating timing sequence of FIG. 11a;

~~[0051]~~[0050] FIG. 11c is a block diagram of another delay circuit for responding to the read command of the mode register;

~~[0052]~~[0051] FIG. 12 is a schematic flowchart of a data transmission method provided according to an embodiment of this disclosure;

~~[0053]~~[0052] FIG. 13 is a schematic flowchart of a data transmission method provided according to another embodiment of this disclosure; and

~~[0054]~~[0053] FIG. 14 is a schematic flowchart of a data transmission method provided according to yet another embodiment of this disclosure.

~~[0055]~~[0054] Description of reference numbers:

100. Data transmission circuit; 1. Data memory unit of mode register; 3. Data memory unit of array region; 4. Delay module; 31. First memory unit; 10. Controllable delay module; 20. Data processing unit of mode register; 200. Mode register; 11. Reference delay unit; 12. Controllable delay unit; 121. Delay unit; 122. First controllable switch unit; 41. First delay unit; 42. Second delay unit; 43. Third delay Unit; 431. First sub-delay unit; 432. Second sub-delay unit; 1101. First read operation delay unit; 1201.Column selection control module; 1301. Third read operation delay unit; 21. First-in first-out pointer processing Unit; 22. First-in first-out data processing unit; 23. Read command processing unit of mode register; 221. Second memory unit; 2211. Memory sub-unit; 2212. Driver; 30. Command decoding circuit; 40. Data processing unit of array region; 300. Memory unit array; 50. First selector; 51. First-in first-out memory unit; 52. Selection module; 511. Third memory unit; 60. First-in first-out memory; 70. Serial- parallel conversion

circuit; 80. Data driving module; 90. Data terminal; 501. First flip-flop; 502. Second flip-flop; 503. Third flip-flop; 504. Fourth flip-flop; 400. Delay chain; 1000. Memory device; 2000. Delay circuit.

Detailed Description of the Preferred Embodiments

~~[0056]~~[0055] In order to facilitate the understanding of this disclosure, the following will make a more comprehensive description of this disclosure with reference to the relevant drawings. The preferred embodiment of the disclosure is shown in the accompanying drawings. However, this disclosure can be implemented in many different forms and is not limited to the embodiments described herein. On the contrary, the purpose of providing these embodiments is to make the disclosure of this disclosure more thorough and comprehensive.

~~[0057]~~[0056] Unless otherwise defined, all technical and scientific terms used herein have the same meaning as commonly understood by those skilled in the technical field of this disclosure. The terminology used in the specification of the disclosure herein is only for the purpose of describing specific embodiments, and is not intended to limit the disclosure.

~~[0058]~~[0057] In addition, certain terms used throughout the specification and the following claims refer to specific elements. Those skilled in the art will understand that manufacturers can refer to components with different names. This document does not intend to distinguish between components with different names but the same function. In the following description and examples, the terms "including" and "comprising" are used openly, and therefore should be interpreted as "including, but not limited to...". Likewise, the term "connection" is intended to express an indirect or direct electrical connection. Correspondingly, if one device is connected to another device, the connection can be done through a direct electrical connection, or through an indirect electrical connection between the other equipment and the connector.

~~[0059]~~[0058] It should be understood that although the terms "first", "second", etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only configured to distinguish one element from another element. For example, without departing from the scope of the present disclosure, the first element may be referred to as the second element, and similarly, the second element may be referred to as the first element.

~~[0060]~~[0059] Referring to FIG. 1, in an embodiment of the present disclosure, a data transmission circuit 100 is provided, including a data memory unit of a mode register 1 and a data memory unit of an array region 3. The data memory unit of the mode register 1 is configured to output data of the

mode register MrrData2 in response to a first clock Signal. An output terminal of the data memory unit of the array region 3 and an output terminal of the data memory unit of the mode register 1 are both connected to a first node A. The data memory unit of the array region 3 is configured to receive array data ArrayData in response to a first pointer signal FifoIn_array, and to output array data ArrayData in response to a second pointer signal FifoOut_array.

~~[0061]~~[0060] As an example, continuingly referring to FIG. 1, the data memory unit of the mode register 1 is set to output the mode register data MrrData2 in response to the first clock signal MrrClk. Before outputting the mode register data MrrData2 in response to the first clock signal MrrClk, the data memory unit of the mode register 1 read a mode register data MrrData1 from a previous data line. The output terminal of the data memory unit of the array region 3 and the output terminal of the data memory unit of the mode register 1 are both connected to the first node A. In response to the first pointer signal FifoIn_array, the data memory unit of the array region 3 receives the data of the array region ArrayData. In response to the second pointer signal FifoOut_array, the data memory unit of the array region 3 outputs the data of the array region ArrayData. In this way, a different control of the data memory unit of the mode register 1 and the data memory unit of the array region 3 is realized, so that a response time for reading the data of the mode register MrrData in response to a read command of the mode register can match a response time for reading the data of the array region ArrayData in response to a data read command of the array region, so as to precisely control the data of the mode register MrrData and the data of the array region ArrayData to output through a respective output channel in turn. The MrrData1 and MrrData2 can be the same or can match a preset algorithm.

~~[0062]~~[0061] Further, referring to FIG. 2, in an embodiment of the present disclosure, the data memory unit of the array region 3 includes eight first memory units 31, and an output terminal of each first memory unit 31 is connected to the first node A. An input terminal of each first memory unit 31 is connected to a first data signal line ArrayDataL, and the first data signal line ArrayDataL is configured to transmit the array data ArrayData, so as to realize precise control of the transmission of the array data ArrayData.

~~[0063]~~[0062] Further, continuingly referring to FIG. 2, in an embodiment of the present disclosure, a driving clock frequency of the first pointer signal FifoIn_array and a driving clock frequency of the second pointer signal FifoOut_array are the same, so that the input data and output data of the data memory unit of the array region 3 can be set to maintain a consistent transmission rate to allow data in while out.

~~[0064]~~[0063] Further, referring to FIG. 3, in an embodiment of the present disclosure, the data

transmission circuit 100 further includes a serial-parallel conversion circuit 70 and a data driving module 80. An input terminal of the serial-parallel conversion circuit 70 is connected to the first node A; the data driving module 80 is connected to an output terminal of the serial-parallel conversion circuit 70 for outputting the mode register data MrrData2 or the array data ArrayData. By using the serial-parallel conversion circuit 70 to convert the received data into serial data and then provide the serial data to the data driving module 80 for outputting, it is convenient to improve the efficiency of data transmission.

~~[0065]~~[0064] Further, referring to FIG. 4, in an embodiment of the present disclosure, the data transmission circuit 100 further includes a data processing unit of the mode register 20, and the data processing unit of the mode register 20 includes a first-in first-out pointer processing unit 21 and a first-in first-out data processing unit 22 and a read command processing unit of the mode register 23. The first-in first-out pointer processing unit 21 is configured to generate the third pointer signal MrFifoIn and the fourth pointer signal MrFifoOut in response to the read command of the mode register MrrCmd. The first-in first-out data processing unit 22 is connected to both the first-in first-out pointer processing unit 21 and the data memory unit of the mode register 1, to read the mode register data MrrData0 from the mode register 200 in response to the third pointer signal MrFifoIn, and to output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the fourth pointer signal MrFifoOut. The read command processing unit of the mode register 23 is configured to generate the first clock signal MrrClk according to a received read command of the mode register MrrCmd, the second clock signal Clk, and the preset read latency signal Read Latency. A time for mode register data MrrData1 to be outputted from the data memory unit of the mode register 1 can be controlled according to the read command of the mode register MrrCmd, the second clock signal Clk and the preset read latency signal Read Latency, so as to precisely control the data of the mode register MrrData0 and the data of the array region ArrayData to output through a respective output channel in turn. The MrrData0 and MrrData1 here can be the same or can match a preset algorithm.

~~[0066]~~[0065] As an example, continuingly referring to FIG. 4, in an embodiment of the present disclosure, a driving clock frequency of the third pointer signal MrFifoIn and a driving clock frequency of the fourth pointer signal MrFifoOut are the same, so as to realize precise control of a time difference between reading data and outputting data by the first-in first-out data processing unit 22.

~~[0067]~~[0066] Further, referring to FIGs. 5a and 5b, in an embodiment of the present disclosure, the data transmission circuit 100 further includes a command decoding circuit 30 and a data processing

unit of the array region 40. A first output terminal of the command decoding circuit 30 is connected to both the input terminal of the read command processing unit of the mode register 23 and the input terminal of the first-in first-out pointer processing unit 21, and is configured to receive the read command Read, to decode the read command Read and to judge whether the read command is the read command of the mode register MrrCmd. If yes, the command decoding circuit 30 outputs the read command of the mode register MrrCmd. Otherwise, the command decoding circuit 30 generates the data read command of the array region ReadCmd. An input terminal of the data processing unit of the array region 40 is connected to a second output terminal of the command decoding circuit 30 to read the data of the array region ArrayData from the memory unit array in response to the data read command of the array region ReadCmd, and provide the data of the array region ArrayData to the data memory unit of the array region 3. In this embodiment, the mode register data MrrData2 and the data of the array region ArrayData are read out via a data transmission circuit 100, as compared to a solution of using different data transmission paths to read the mode register data MrrData and the data of the array region ArrayData respectively, the integration of semiconductor storage devices is further improved.

~~[0068]~~[0067] As an example, referring to FIG. 5b, in an embodiment of the present disclosure, a selection module 52 is set to receive the mode register data MrrData1 and the data of the array region ArrayData, and an output terminal of the selection module 52 is connected to the first-in first-out memory unit 51. The first-in first-out memory unit 51 includes j third memory units 511 connected in parallel, j is a positive integer, and j can be set to be equal to a bit width of the data of the array region ArrayData. The mode register data MrrData1 and the data of the array region ArrayData are sequentially output through the first-in first-out memory unit 51, the serial-parallel conversion circuit 70, the data driving module 80, and the data terminal 90 by controlling the switching of the selection module 52. Referring to both FIG. 5a and FIG. 5b, the mode register data MrrData0 and the data of the array region ArrayData in FIG. 5a are transmitted to the parallel-serial conversion circuit 70 through different FIFOs (first-in first-out registers). The mode register data MrrData0 and the array data ArrayData in FIG. 5b is transmitted to the parallel-serial conversion circuit 70 through a same FIFO. The technical solution in FIG. 5a is more flexible for the timing control of the data transmission circuit, and the technical solution in FIG. 5b can make the area of the data transmission circuit smaller.

~~[0069]~~[0068] As an example, referring to FIG. 6, in an embodiment of the present disclosure, the first-in first-out data processing unit 22 includes a plurality of second memory units 221, and the output terminals of the plurality of second memory units 221 are all connected to a second node O. Each second memory unit 221 includes a memory subunit 2211 and a driver 2212. An input terminal

of the driver 2212 is connected to an output terminal of the memory subunit 2211. The memory subunit 2211 is driven by a third pointer signal MrFifoIn to receive a mode register data MrrData0. The driver 2212 is driven by a fourth pointer signal MrFifoOut to output a mode register data MrrData1, so that the first-in first-out data processing unit 22 cooperates with the first-in first-out pointer processing unit 21 to achieve precise control of the time of responding to the read command of the mode register MrrCmd to read the mode register data MrrData1, thereby precisely controlling the time of responding to the read command of the mode register MrrCmd to read the mode register data MrrData1 to match the time of responding to the data read command of the array region ReadCmd to read the array data ArrayData.

~~[0070]~~[0069] As an example, referring to FIG. 7, in an embodiment of the present disclosure, the data input terminal of each memory subunit 2211 is connected to the mode register 200, so that each memory subunit 2211 can read the mode register data MrrData0 from the mode register 200 in response to the third pointer signal MrFifoIn, and each driver 2212 can output the mode register data MrrData1 in response to the fourth pointer signal MrFifoOut.

~~[0071]~~[0070] As an example, referring to FIG. 7, in an embodiment of the present disclosure, a driving clock frequency of the third pointer signal MrFifoIn and a driving clock frequency of the fourth pointer signal MrFifoOut are the same, so as to realize precise control of a time difference between reading data and outputting data by the first-in first-out data processing unit 22.

~~[0072]~~[0071] Referring to FIG. 8a, in an embodiment of the present disclosure, a data transmission circuit 100 is provided, including a controllable delay module 10, a data processing unit of a mode register 20, a data memory unit of an array region 3, and a data memory unit of the mode register 1. The controllable delay module 10 is configured to generate a preset read latency signal Read Latency in response to a read command of the mode register MrrCmd. The data processing unit of the mode register 20 is connected to the controllable delay module to read from the mode register 200 in response to the read command of the mode register MrrCmd to output the mode register data MrrData0, and is also configured to output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the preset read latency signal Read Latency. An output terminal of the data memory unit of the array region 3 and an output terminal of the data memory unit of the mode register 1 are connected to a first node A. The data memory unit of the array region 3 is configured to receive data of the array region ArrayData in response to a first pointer signal FifoIn_array, and to output the data of the array region ArrayData in response to a second pointer signal FifoOut_array. The data memory unit of the mode register 1 is configured to output the data of the mode register MrrData2 in respond to a first clock signal MrrClk.

~~[0073]~~[0072] As an example, continuingly referring to FIG. 8a, the controllable delay module 10 is set to generate the preset read latency signal Read Latency in response to the read command of the mode register MrrCmd, so that the data processing unit of the mode register 20 can read the mode register data MrrData0 from the mode register 200 in response to the read command of the mode register MrrCmd, and output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the preset read latency signal Read Latency. The data memory unit of the mode register 1 is set to output the mode register data MrrData2 in response to the first clock signal MrrClk. The output terminal of the data memory unit of the array region 3 and the output terminal of the data memory unit of the mode register 1 are both connected to the first node A. The data memory unit of the array region 3 can receive the data of the array region ArrayData in response to the first pointer signal FifoIn_array, and output the data of the array region ArrayData in response the second pointer signal FifoOut_array, so as to realize different control between the data memory unit of the mode register 1 and the data memory unit of the array region 3, so that a time of responding to a read command of the mode register MrrCmd to read data of the mode register MrrData2 can match a time of responding to a read command of the array region ReadCmd to read data of the array region ArrayData, to precisely control the data of the mode register MrrData2 and the data of the array region ArrayData to output through a respective output channel in turn. Once the operation delay of the controllable delay module 10 in this disclosure is determined, it is less affected by changes in the working environment, which can effectively avoid control errors in the data transmission path due to the influence of the working environment; and the operation delay of the controllable delay module 10 can be controlled and adjusted, which can meet the operating parameter requirements of different types of semiconductor memory devices.

~~[0074]~~[0073] As an example, continuingly referring to FIG. 8a, in an embodiment of the present disclosure, a time difference between a start time when the data processing unit of the mode register 20 outputs the data of the mode register MrrData1 and a moment when the controllable delay module 10 receives the read command of the mode register MrrCmd is a first preset threshold, so that the time for responding to the read command of the mode register MrrCmd to read the mode register data MrrData1 matches the time for responding to the data read command of the array region ReadCmd to read the data of the array region ArrayData.

~~[0075]~~[0074] Further, referring to FIG. 8b, in an embodiment of the present disclosure, the controllable delay module 10 includes a reference delay unit 11 and a controllable delay unit 12. The reference delay unit 11 is configured to generate an initial preset read latency signal Read Latency in response to the read command of the mode register MrrCmd. The controllable delay unit 12 is

connected to an output terminal of the reference delay unit 11 and an input terminal of the data processing unit of the mode register 20, and is configured to generate a preset read latency signal Read Latency after delaying a preset delay time from the moment of receiving the initial preset read latency signal Read Latency. A sum of an operation delay of the controllable delay unit 12 and an operation delay of the reference delay unit 11 is equal to a first preset threshold. By setting the sum of the operation delay of the reference delay unit 11 and the operation delay of the controllable delay unit 12 to be equal to the first preset threshold, the operation delay range of the controllable delay unit 12 is reduced, which can increase the efficiency and accuracy for adjusting the operation delay of the controllable delay module 10 to the first preset threshold.

~~[0076]~~[0075] Further, referring to FIG. 8c, in an embodiment of the present disclosure, the controllable delay unit ~~10~~ 12 includes three delay units 121 connected in series. Each of two delay units 121 are connected in parallel with a first controllable switch unit 122. By controlling the turn-on and turn-off of each first controllable switch unit 122, the number of delay units 121 connected in series between the reference delay unit 11 and the data processing unit of the mode register 20 in the controllable delay unit 12 is changed to adjust the operation delay of the controllable delay unit. The operation delay of the controllable delay unit 12 realizes the gradient control, so as to improve the efficiency and accuracy of adjusting the operation delay of the controllable delay module 10 to the first preset threshold.

~~[0077]~~[0076] As an example, referring to FIG. 8d, in an embodiment of the present disclosure, the data memory unit 3 of the array region includes a plurality of first memory units 31, and each of the output terminals of the plurality of first memory units 31 is connected to the first node A, each of the input terminals of the plurality of first memory units 31 is connected to a first data signal line ArrayDataL. The first data signal line ArrayDataL is configured to transmit the data of the array region ArrayData, so as to realize precise control of the transmission of the data of the array region ArrayData.

~~[0078]~~[0077] As an example, continuingly referring to FIG. 8d, in an embodiment of the present disclosure, a driving clock frequency of the first pointer signal FifoIn_array and a driving clock frequency of the second pointer signal FifoOut_array are the same, so as to set the input data and output data of the data memory unit 3 of the array region to maintain a consistent transmission rate to allow data in while out.

~~[0079]~~[0078] Further, referring to FIG. 8e, in an embodiment of the present disclosure, the data processing unit of the mode register 20 includes a mode first-in first-out pointer processing unit 21, a first-in first-out data processing unit 22, and a read command processing unit of a mode register 23.

The read command processing unit of the mode register 23 is configured to generate the first clock signal MrrClk according to the received read command of the mode register MrrCmd, the second clock signal Clk and the preset read latency signal Read Latency. The first-in first-out pointer processing unit 21 is configured to generate a third pointer signal MrFifoIn and a fourth pointer signal MrFifoOut in response to the read command of the mode register MrrCmd. The first-in first-out data processing unit 22 is connected to the first-in first-out pointer processing unit 21 and the data memory unit of the mode register 1, to reads the mode register data MrrData0 from the mode register 200 in response to the third pointer signal MrFifoIn, and to output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the fourth pointer signal MrFifoOut.

~~[0080]~~[0079] As an example, continuingly referring to FIG. 8e, in an embodiment of the present disclosure, a driving clock frequency of the third pointer signal MrFifoIn and a driving clock frequency of the fourth pointer signal MrFifoOut are the same, so as to realize precise control of a time difference between reading data and outputting data by the first-in first-out data processing unit 22.

~~[0081]~~[0080] Further, referring to FIG. 8f, in an embodiment of the present disclosure, the data transmission circuit 100 further includes a command decoding circuit 30 and a data processing unit of the array region 40. A first output terminal of the command decoding circuit 30 is connected to an input terminal of the read command processing unit of the mode register 23 and an input terminal of the first-in first-out pointer processing unit 21, to receive a read command, decode the read command Read and determine whether the read command Read is the read command of the mode register MrrCmd. If yes, the command decoding circuit 30 outputs the read command of the mode register MrrCmd, otherwise, the command decoding circuit 30 generates a data read command of the array region ReadCmd. An input terminal of the data processing unit of the array region 40 is connected to a second output terminal of the command decoding circuit 30, and is configured to read the data of the array region ArrayData from the memory unit array 300 in response to the data read command of the array region ReadCmd, and to provide the data of the array region ArrayData to the data memory unit of the array region 3.

~~[0082]~~[0081] As an example, referring to FIG. 8g, it can be set that the reference delay unit 11 includes a plurality of sub-delay units connected in series. The sub-delay units can be configured to replicate operation delay of a functional unit with fixed delay time in the path where the data processing unit of the array region 40 reads the data of the array region in response to the data read command of the array region, and to set the operation delay of the controllable delay unit to match the delay time of a functional unit with variable delay time in the path where the data processing unit of

the array region 40 reads the data of the array region in response to the data read command of the array region, thereby realizing gradient control of the operation delay of the controllable delay unit, and improving the efficiency and accuracy of adjusting the operation delay of the controllable delay module to the first preset threshold.

~~[0083]~~[0082] Referring to FIG. 9a, in an embodiment of the present disclosure, a data transmission circuit 100 is provided, including a delay module 4, a data processing unit of a mode register 20, a data memory unit of an array region 3, and a data memory unit of the mode register 1. The delay module 4 is configured to generate a preset read latency signal Read Latency after delaying a first preset time from a moment of receiving the read command of the mode register MrrCmd. The data processing unit of the mode register 20 is connected to the delay module 4 and the data memory unit of the mode register 1. The data processing unit of the mode register 20 is configured to read the mode register data MrrData0 from the mode register 200 in response to the read command of the mode register MrrCmd, and to output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the preset read latency signal Read Latency. An output terminal of the data memory unit of the array region 3 and an output terminal of the data memory unit of the mode register 1 are both connected to a first node A. The data memory unit of the array region 3 is configured to receive the array data ArrayData in response to the first pointer signal FifoIn_array, and to output the data of the array region ArrayData in response to the second pointer signal FifoOut_array. The data memory unit of the mode register 1 is configured to output the mode register data MrrData2 in response to the first clock signal MrrClk.

~~[0084]~~[0083] As an example, referring to FIG. 9a, the delay module 4 is set to generate the preset read latency signal Read Latency after delaying the first preset time from the moment when the read command of the mode register MrrCmd is received, so that the data processing unit of the mode register 20 can read the mode register data MrrData0 from the mode register 200 in response to the read command of the mode register MrrCmd, and output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the preset read latency signal Read Latency. The data memory unit of the mode register 1 is set to output the mode register data MrrData2 in response to the first clock signal MrrClk. The output terminal of the data memory unit of the array region 3 and the output terminal of the data memory unit of the mode register 1 are both connected to the first node, and the data memory unit of the array region 3 can receive the data of the array region ArrayData in response to the first pointer signal FifoIn_array, and output the data of the array region ArrayData in response to the second pointer signal FifoOut_array, which realizes the different control of the data memory unit of the mode register 1 and the array data memory unit 3, so that the time of responding

to the read command of the mode register MrrCmd to read the mode register data MrrData2 can match the time of responding to the data read command of the array region ReadCmd to read the data of the array region ArrayData, and the mode register data MrrData2 and the data of the array region ArrayData can be controlled to be sequentially output through their respective output channel in turn.

~~[0085]~~[0084] Further, referring to FIG. 9b, in an embodiment of the present disclosure, the delay module 4 includes a first delay unit 41, a second delay unit 42, and a third delay unit 43. The first delay unit 41 is configured to generate a first preset read latency signal after delaying a second preset time from the moment of receiving a read command of the mode register MrrCmd. The second delay unit 42 is connected to an output terminal of the first delay unit 41 to generate a second preset read latency signal after delaying a third preset time from the moment of receiving the first preset read latency signal, and the third preset time is equal to an operation delay of the column selection control module (not labeled). The third delay unit 43 is connected to an output terminal of the second delay unit 42 and an input terminal of the data processing unit of the mode register 20, and is configured to generate a preset read latency signal Read Latency after delaying a fourth preset time from the moment of receiving the second preset read latency signal. A sum of the second preset time, the third preset time, and the fourth preset time is equal to the first preset time. This embodiment can avoid the influence of the operation delay of the column selection control module in a specific type of semiconductor memory device on the transmission circuit.

~~[0086]~~[0085] Further, referring to FIG. 9c, in an embodiment of the present disclosure, the third delay unit 43 includes a first sub-delay unit 431 and a second sub-delay unit 432. The first sub-delay unit 431 is connected to an output terminal of the second delay unit 42, and is configured to generate a third preset read latency signal after delaying a fifth preset time from the moment of receiving the second preset read latency signal, and the fifth preset time is equal to an operation delay of the read-write amplifier. The second sub-delay unit 432 is connected to an output terminal of the first sub-delay unit 431 and an input terminal of the data processing unit of the mode register 20, and is configured to generate a preset read latency signal delay Read Latency after delaying a sixth preset time from the moment of receiving the third preset read latency signal. A sum of the fifth preset time and the sixth preset time is equal to the fourth preset time. This embodiment can avoid the influence of the operation delay of the read-write amplifier in a specific type of semiconductor memory device on the transmission circuit.

~~[0087]~~[0086] As an example, continuingly referring to FIG. 9c, in an embodiment of the present disclosure, the data memory unit of the array region 3 includes a plurality of first memory units 31 (not labelled in FIG. 9c), and an output terminal of each first memory units 31 is connected to the first

node A, an input terminal of each first memory unit 31 is connected to the first data signal line, and the first data signal line is configured to transmit the data of the array region ArrayData.

~~[0088]~~[0087] As an example, continuingly referring to FIG. 9c, in an embodiment of the present disclosure, a driving clock frequency of the first pointer signal FifoIn_array and a driving clock frequency of the second pointer signal FifoOut_array are the same.

~~[0089]~~[0088] Further, referring to FIG. 9d, in an embodiment of the present disclosure, the data processing unit of the mode register 20 includes a first-in first-out pointer processing unit 21, a first-in first-out data processing unit 22, and a read command processing unit of the mode register 23. The read command processing unit of the mode register 23 is configured to generate the first clock signal MrrClk according to the received read command of the mode register MrrCmd, the second clock signal Clk and the preset read latency signal Read Latency. The first-in first-out pointer processing unit 21 is configured to generate a third pointer signal MrFifoIn and a fourth pointer signal MrFifoOut in response to the read command of the mode register MrrCmd. The first-in first-out data processing unit 22 is connected to the first-in first-out pointer processing unit 21 and the data memory unit of the mode register 1, and is configured to read the mode register data MrrData0 from the mode register 200 in response to the third pointer signal MrFifoIn, and to output the mode register data MrrData1 to the data memory unit of the mode register 1 in response to the fourth pointer signal MrFifoOut. In an embodiment of the present disclosure, a driving clock frequency of the third pointer signal MrFifoIn and a driving clock frequency of the fourth pointer signal MrFifoOut are the same.

~~[0090]~~[0089] Further, referring to FIGs. 9e and 9f, in an embodiment of the present disclosure, the data transmission circuit 100 further includes a command decoding circuit 30 and an array data processing unit 40. A first output terminal of the command decoding circuit 30 is connected to an input terminal of a read command processing unit of a mode register 23 and an input terminal of the first-in first-out pointer processing unit 21. The command decoding circuit 30 is configured to receive a read command, decode the read command Read and determine whether the read command Read is the read command of the mode register MrrCmd. If yes, the command decoding circuit 30 outputs the read command of the mode register MrrCmd. Otherwise, the command decoding circuit 30 generates the data read command of the array region ReadCmd. An input terminal of the data processing unit of the array region is connected to a second output terminal of the command decoding circuit 30, to read the data of the array region ArrayData read from the memory unit array 300 in response to the data read command of the array region ReadCmd, and to provide the data of the array region ArrayData to the data memory unit of the array region 3.

~~[0091]~~[0090] As an example, continuing referring to FIG. 9f, a delay time of the data processing unit of the array region40 reading the data of the array region in response to the data read command of the array region can be equivalent to a sum of a delay time of the first read operation delay unit 1101, an operation delay of column selection control module 1201 and a delay time of the third read operation delay unit 1301. The second delay unit ~~12~~ 42 is set to replicate the operation delay of the column selection control module 1201, the delay time of the first delay unit ~~11~~ 41 is set to match the operation delay of the first read operation delay unit, and the delay time of the third delay unit ~~13~~ 43 is set to match the delay time of the third read operation delay unit 1301, so that the time of responding to the read command of the mode register MrrCmd to read the setup parameter MrrData2 can match the time of responding to the data read command of the array region to read the data of the array region.

~~[0092]~~[0091] Further, continuingly referring to FIG. 7, in an embodiment of the present disclosure, the difference between the operation delay of the data processing unit of the array region 40 and the first preset time may be set to a preset threshold, so as to satisfy requirements of operating parameters of a specific type of semiconductor memory devices, such as dynamic random access memory (DRAM).

~~[0093]~~[0092] As an example, referring to FIG. 10a and FIG. 10b, in an embodiment of the present disclosure, a frequency of the third pointer signal MrFifoIn and a frequency of the read command of the mode register MrrCmd can be set the same, and a frequency of the fourth pointer signal MrFifoOut and a frequency of the preset read latency signal Read Latency can be set the same. A time difference between a time of driving the preset read latency signal Read Latency and a time of driving the read command of the mode register MrrCmd is set to be the first preset time Td. A time difference between the operation delay of the data processing unit of the array region 40 and the first preset time Td is set to be a preset threshold, so that the time for responding to the read command of the mode register MrrCmd to read the set parameter MrrData2 can match the time for responding to the data read command of the array region ReadCmd to read the data of the array region ArrayData.

~~[0094]~~[0093] As an example, in an embodiment of the present disclosure, the preset threshold may be set to an integer multiple of the column refresh period, to meet the requirements of the operation parameters of a specific type of semiconductor memory device, such as LPDDR4.

~~[0095]~~[0094] FIG. 11a is a delay circuit 2000 that reads the setting parameter MrrData0 from the mode register 200 in response to the read command of the mode register MrrCmd in a data transmission circuit, and FIG. 11b is a schematic diagram of the operating timing sequence of FIG. 11a. The delay circuit 2000 includes a first flip-flop 501, a second flip-flop 502, a third flip-flop 503,

a fourth flip-flop 504, and a delay chain 400. The delay chain 400 is configured to generate a first clock signal Clk1, a second clock signal Clk2, a third clock signal Clk3, a fourth clock signal Clk4, and a preset read latency signal Read Latency in response to the read command of the mode register MrrCmd. The first flip-flop 501 is configured to receive the setting parameter MrrData0 in response to the first clock signal Clk1, and the second flip-flop 502 is configured to receive data provided by the first flip-flop 501 in response to the second clock signal Clk2, the third flip-flop 503 is configured to receive data provided by the second flip-flop 502 in response to the third clock signal Clk3, and the fourth flip-flop 504 is configured to receive the data provided by the third flip-flop 503 in response to the fourth clock signal Clk4 and to output the setting parameter MrrData1. By controlling the driving time of the delay chain 400 generating the first clock signal Clk1, the second clock signal Clk2, the third clock signal Clk3, the fourth clock signal Clk4, and the preset read latency signal Read Latency, the time of responding to the data command of the mode register MrrCmd to read the set parameter MrrData2 can be controlled to match the time of responding to the data read command of the array region ReadCmd to read the data of the array region ArrayData.

~~[0096]~~[0095] Refer to both FIG. 11a and FIG. 11c, each clock (Clk1, Clk2, Clk3, Clk4) in FIG. 11a needs to be deployed to ensure the correct timing sequence from MrrData1 to MrrData2. On the contrary, FIG. 11c only needs to deploy the timing sequence from MrrCmd to Read Latency, and the technical solution of FIG. 11c is easier to deploy.

~~[0097]~~[0096] In an embodiment of the present disclosure, a memory device is provided, including a memory cell array 300, a mode register 200, and any data transmission circuit in the above embodiments of the present disclosure. The memory cell array 300 is configured to store data of the array region ArrayData, the mode register 200 is configured to store the data of the mode register MrrData0. This embodiment realizes the different control of the data memory unit of the mode register 1 and the data memory unit of the array region 3, so that the time for responding to the read command of the mode register to read the mode register data MrrData2 can match the time for responding to the data read command of the array region 3 to read the data of the array region ArrayData, and the mode register data MrrData2 and the array data ArrayData can be precisely controlled to be output through their respective output channel in turn.

~~[0098]~~[0097] Referring to FIG. 12, a data transmission method is provided according to an embodiment of the present disclosure, the method includes the following steps.

~~[0099]~~[0098] At a step 502, a data memory unit of a mode register outputs data of the mode register in response to a first clock signal.

~~[00100]~~[0099] At a step 504, a data memory unit of an array region receives data of the array region in response to a first pointer signal, and outputs the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

~~[00101]~~[00100] As an example, continuingly referring to FIG. 12, the data memory unit of the mode register outputs data of the mode register in response to the first clock signal, the data memory unit of the array region receives data of the array region in response to the first pointer signal, and outputs the data of the array region in response to the second pointer signal, wherein the output terminal of the data memory unit of the array region and the output terminal of the data memory unit of the mode register are both connected to a first node, thereby realizing different control of the data memory unit of the mode register and the data memory unit of the array region, so that a response time for the readout of the data of the mode register in response to a read command of the mode register matches a response time for the readout of the data of the array region in response to a data read command of the array region, so as to precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn.

~~[00102]~~[00101] Referring to FIG. 13, in an embodiment of the present disclosure, a data transmission method is provided, including the following steps.

~~[00103]~~[00102] At a step 602, a controllable delay module generates a preset read latency signal in response to a read command of a mode register.

~~[00104]~~[00103] At a step 604, a data processing unit of the mode register reads the mode register data from the mode register in response to a read command of the mode register, and outputs the mode register data to a data memory unit of the mode register in response to the preset read latency signal.

~~[00105]~~[00104] At a step 606, the data memory unit of the mode register outputs the mode register data in response to a first clock signal.

~~[00106]~~[00105] At a step 608, the data memory unit of the array region receives the data of the array region, in response to a first pointer signal, and outputs the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

~~[00107]~~[00106] As an example, continuingly referring to FIG. 13, the controllable delay module generates the preset read latency signal in response to the read command of a mode register, the data processing unit of the mode register reads the mode register data in response to the read command of the mode register, and outputs the mode register data to the data memory unit of the mode register in

response to the preset read latency signal; the data memory unit of the mode register outputs the mode register data in response to the first clock signal; the data memory unit of the array region receives the data of the array region, in response to the first pointer signal, and outputs the data of the array region in response to the second pointer signal, wherein the output terminal of the data memory unit of the array region and the output terminal of the data memory unit of the mode register are both connected to the first node, thereby realizing different control of the data memory unit of the mode register and the data memory unit of the array region, so that a response time for the readout of the data of the mode register in response to a read command of the mode register matches a response time for the readout of the data of the array region in response to a data read command of the array region, so as to precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn. Once the operation delay of the controllable delay module in this disclosure is determined, it is less affected by changes in the working environment, which can effectively avoid control errors in the data transmission path due to the influence of the working environment; and the operation delay of the controllable delay module can be controlled and adjusted, thereby the operation can meet the operating parameter requirements of different types of semiconductor memory devices. ~~Once the operation delay of the controllable delay module in this disclosure is determined, it is less affected by changes in the working environment, which can effectively avoid control errors in the data transmission path due to the influence of the working environment; and the operation delay of the controllable delay module can be controlled and adjusted, which can meet the operating parameter requirements of different types of semiconductor memory devices.~~

~~[00108]~~[00107] Referring to FIG. 14, in an embodiment of the present disclosure, a data transmission method is provided, including the following steps.

~~[00109]~~[00108] At a step 702, a delay module generates a preset read latency signal after delaying a first preset time from a moment of receiving a read command of the mode register.

~~[00110]~~[00109] At a step 704, a data processing unit of the mode register reads the mode register data from the mode register in response to a read command of the mode register, and outputs the mode register data to a data memory unit of the mode register in response to a preset read latency signal.

~~[00111]~~[00110] At a step 706, the data memory unit of the mode register outputs the mode register data in response to a first clock signal.

~~[00112]~~[00111] At a step 708, the data memory unit of the array region receives the data of the array region in response to a first pointer signal, and outputs the data of the array region in response to a

second pointer signal, wherein an output terminal of the data memory unit in the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

~~[00113]~~[00112] As an example, continuingly referring to FIG. 14, the delay module generates the preset read latency signal after delaying the first preset time from the time of receiving the read command of the mode register; the data processing unit of the mode register reads the mode register data from the mode register in response to the read command of the mode register, and outputs the mode register data to the data memory unit of the mode register in response to the preset read latency signal; the data memory unit of the mode register outputs the mode register data in response to the first clock signal; the data memory unit of the array region receives the data of the array region in response to the first pointer signal, and outputs the data of the array region in response to the second pointer signal, wherein the output terminal of the data memory unit in the array region and the output terminal of the data memory unit of the mode register are both connected to the first node; thereby realizing different control of the data memory unit of the mode register and the data memory unit of the array region, so that a response time for the readout of the data of the mode register in response to a read command of the mode register matches a response time for the readout of the data of the array region in response to a data read command of the array region, so as to precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn.

~~[00114]~~[00113] For the specific features of the data transmission method in the above embodiment, please refer to the above description of the data transmission circuit, which will not be repeated here.

~~[00115]~~[00114] It should be understood that although the various steps in the flowcharts of FIGS. 12-14 are displayed in sequence as indicated by the arrows, these steps are not necessarily performed in sequence in the order indicated by the arrows. Unless there is a clear description in this article, there is no strict order for the execution of these steps, and these steps can be executed in other orders. Moreover, at least part of the steps in FIG.s 12-14 may include multiple steps or multiple stages. These steps or stages are not necessarily executed at the same time, but can be executed at different times. The order of execution is not necessarily performed sequentially, but may be performed alternately or alternately with other steps or at least a part of the steps or stages in other steps.

~~[00116]~~[00115] A person of ordinary skill in the art can understand that all or part of the processes in the above-mentioned embodiment methods can be implemented by instructing relevant hardware through a computer program. The computer program can be stored in a non-volatile computer readable storage. In the medium, when the computer program is executed, it may include the procedures of the above-mentioned method embodiments. Wherein, any reference to memory, storage, database or other

media used in the embodiments provided in this disclosure may include non-volatile and/or volatile memory. Non-volatile memory may include read only memory (ROM), programmable ROM (PROM), electrically programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM), or flash memory. Volatile memory may include random access memory (RAM) or external cache memory. As an illustration and not a limitation, RAM is available in many forms, such as static RAM (SRAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), double data rate SDRAM (DDRSDRAM), enhanced SDRAM (ESDRAM), synchronous chain Channel (Synchlink) DRAM (SLDRAM), direct memory bus dynamic RAM (DRDRAM), and memory bus dynamic RAM (RDRAM), etc.

~~[00117]~~[00116] Please note that the above-mentioned embodiments are only for illustrative purposes and are not meant to limit the present invention.

~~[00118]~~[00117] The technical features of the above-mentioned embodiments can be combined arbitrarily. In order to make the description concise, all possible combinations of the various technical features of the above-mentioned embodiments are not described. However, as long as there is no contradiction in the combination of these technical features, they should be It is considered as the range described in this specification.

~~[00119]~~[00118] The above-mentioned embodiments only express several implementation modes of the present disclosure, and their descriptions are relatively specific and detailed, but they should not be understood as limiting the scope of the patent disclosure. It should be pointed out that for those of ordinary skill in the art, without departing from the concept of this disclosure, several modifications and improvements can be made, and these all fall within the protection scope of this disclosure. Therefore, the scope of protection of the patent in this disclosure shall be subject to the appended claims.

Claims

1. A data transmission circuit, comprising:

a data memory unit of a mode register configured to output data of the mode register in response to a first clock signal; and

a data memory unit of an array region configured to receive data of the array region in response to a first pointer signal, and to output data of the array region in response to a second pointer signal;

wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

2. The data transmission circuit according to claim 1, wherein the data memory unit of the array region comprises a plurality of first memory units, wherein an output terminal of each of the plurality of first memory units is connected to the first node, wherein an input terminal of each of the plurality of first memory units is connected to a first data signal line, and wherein the first data signal line is configured to transmit data of the array region.

3. The data transmission circuit according to claim 2, wherein a driving clock frequency of the first pointer signal and a driving clock frequency of the second pointer signal are the same.

4. The data transmission circuit according to any one of claims 1-3, further comprising:

a serial-parallel conversion circuit, wherein an input terminal of the serial-to-parallel conversion circuit is connected to the first node; and

a data driving module connected to an output terminal of the serial-parallel conversion circuit, and configured to output data of the mode register or data of the array region.

5. The data transmission circuit according to any one of claims 1-3, further comprising a data processing unit of the mode register, wherein the data processing unit of the mode register comprises:

a read command processing unit of the mode register configured to generate the first clock signal according to a received read command of the mode register, a second clock signal, and a preset read latency signal;

a first-in first-out pointer processing unit configured to generate a third pointer signal and a fourth pointer signal in response to the read command of the mode register; and

a first-in first-out data processing unit connected to the first-in first-out pointer processing unit, the data memory unit of the mode register and the mode register, wherein the first-in first-out data processing unit is configured to read data of the mode register from the mode register in response to

the third pointer signal and to output the data of the mode register to the data memory unit of the mode register in response to the fourth pointer signal.;

6. The data transmission circuit according to claim 5, wherein a driving clock frequency of the third pointer signal and a driving clock frequency of the fourth pointer signal are the same.

76. The data transmission circuit according to claim 5, further comprising:

a command decoding circuit comprising a first output terminal connected to an input terminal of the read command processing unit of the mode register and an input terminal of the first-in first-out pointer processing unit, wherein the command decoding circuit is configured to receive a read command, decode and judge whether the read command is a read command of the mode register; and wherein the command decoding circuit is configured to output the read command of the mode register in response to the read command being the read command of the mode register, and to generate an data read command of the array region in response to the read command not being the read command of the mode register; and

a data processing unit of the array region comprising an input terminal connected to a second output terminal of the command decoding circuit, wherein the data processing unit of the array region is configured to read data of the array region from a memory unit array in response to the data read command of the array region, and to provide the data of the array region to the data memory unit of the array region.

87. The data transmission circuit according to claim 5, wherein the first-in first-out data processing unit comprises:

a plurality of second memory units, wherein an output terminal of each of the plurality of second memory units is connected to a second node;

wherein each of the plurality of second memory units comprises a memory sub-unit and a driver, wherein an input terminal of the driver is connected to an output terminal of the memory sub-unit, wherein the memory sub-unit is configured to receive data of the mode register under a driving of the third pointer signal, wherein the driver is configured to output data of the mode register under a driving of the fourth pointer signal.;

9. The data transmission circuit according to claim 8, wherein an input terminal of each memory sub-unit is connected to the mode register.

108. A data transmission circuit, comprising:

a controllable delay module configured to generate a preset read latency signal in response to a

read command of a mode register;

a data processing unit of the mode register connected to the controllable delay module, wherein the data processing unit of the mode register is configured to read data of the mode register from the mode register in response to a read command of the mode register, wherein the data processing unit of the mode register is further configured to send the data of the mode register to a data memory unit of the mode register in response to the preset read latency signal; and

a data memory unit of the array region, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node, and wherein the data memory unit of the array region is configured to receive data of the array region in response to a first pointer signal, and to output the data of the array region in response to a second pointer signal;

wherein the data memory unit of the mode register is configured to output the data of the mode register in response to a first clock signal.

~~11~~9. The data transmission circuit according to claim ~~10~~8, wherein a time difference between a start time when the data processing unit of the mode register outputs the data of the mode register and a time when the controllable delay module receives the read command of the mode register is a first preset threshold.

~~12~~10. The data transmission circuit according to claim ~~11~~9, wherein the controllable delay module comprises:

a reference delay unit configured to generate an initial preset read latency signal in response to the read command of the mode register; and

a controllable delay unit connected to an output terminal of the reference delay unit and an input terminal of the data processing unit of the mode register, wherein the controllable delay unit is configured to generate a preset read latency signal after delaying a preset delay time from a moment of receiving the initial preset read latency signal;

wherein a sum of an operation delay of the controllable delay unit and an operation delay of the reference delay unit is equal to the first preset threshold.

~~13~~11. The data transmission circuit according to claim ~~12~~10, wherein the controllable delay unit comprises at least two delay units connected in series;

wherein at least one of the delay units is connected in parallel with a first controllable switch unit;

wherein the data transmission circuit is configured to change the number of delay units connected in series between the reference delay unit and the data processing unit of the mode register in the controllable delay unit by controlling turn-on or turn-off of the respective first controllable switch unit, to adjust an operation delay of the controllable delay unit.

~~14~~12. The data transmission circuit according to any one of claims ~~10~~8-~~13~~11, wherein the data memory unit of the array region comprises a plurality of first memory units, wherein an output terminal of each of the plurality of first memory units is connected to the first node, an input terminal of each of the plurality of first memory units is connected to a first data signal line, and wherein the first data signal line is configured to transmit the data of the array region~~.~~;

~~15. The data transmission circuit according to claim 14,~~ wherein a driving clock frequency of the first pointer signal and a driving clock frequency of the second pointer signal are the same.

~~16~~13. The data transmission circuit according to any one of claims ~~10~~8-~~13~~11, wherein the data processing unit of the mode register comprises:

a read command processing unit of the mode register configured to generate a first clock signal according to a received read command of the mode register, a second clock signal, and a preset read latency signal;

a first-in first-out pointer processing unit configured to generate a third pointer signal and a fourth pointer signal in response to the read command of the mode register; and

a first-in first-out data processing unit connected to both the first-in first-out pointer processing unit and the data memory unit of the mode register, wherein the first-in first-out data processing unit is configured to read data of the mode register from the mode register in response to the third pointer signal, and to output the data of the mode register to the data memory unit of the mode register in response to the fourth pointer signal~~.~~;

~~17. The data transmission circuit according to claim 16,~~ wherein a driving clock frequency of the third pointer signal and a driving clock frequency of the fourth pointer signal are the same.

~~18~~14. The data transmission circuit according to claim ~~17~~13, further comprising:

a command decoding circuit, comprising a first output terminal connected to an input terminal of the read command processing unit of the mode register and an input terminal of the first-in first-out pointer processing unit, wherein the command decoding circuit is configured to receive a read command, decode and judge whether the read command is a read command of the mode register; and wherein the command decoding circuit is configured to output the read command of the mode register

in response to the read command being the read command of the mode register, and to generates a data read command of the array region in response to the read command not being the read command of the mode register; and

a data processing unit of the array region, comprising an input terminal connected to a second output terminal of the command decoding circuit, wherein the data processing unit of the array region is configured to read data of the array region from a memory unit array in response to the data read command of the array region, and to provide the data of the array region to the data memory unit of the array region.

~~19~~15. A data transmission circuit, comprising:

a delay module configured to generate a preset read latency signal after delaying a first preset time from a moment of receiving a read command of the mode register;

a data processing unit of the mode register, connected to the delay module and configured to read data of the mode register from the mode register in response to the read command of the mode register, and to output the data of the mode register to the data memory unit of the mode register in response to the preset read latency signal; and

a data memory unit of an array region, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node; wherein the data memory unit of the array region is configured to receive data of the array region in response to a first pointer signal, and to output the data of the array region in response to a second pointer signal;

wherein the data memory unit of the mode register is configured to output data of the mode register in response to a first clock signal.

~~20~~16. The data transmission circuit according to claim ~~19~~15, wherein the delay module comprises:

a first delay unit configured to generate a first preset read latency signal after delaying a second preset time from a moment of receiving the read command of the mode register;

a second delay unit connected to an output terminal of the first delay unit and configured to generate a second preset read latency signal after delaying a third preset time from a moment of receiving the first preset read latency signal, wherein the third preset time is equal to an operation delay of a column selection control module; and

a third delay unit connected to both an output terminal of the second delay unit and an input terminal of the data processing unit of the mode register; wherein the third delay unit is configured to

generate a preset read latency signal after delaying a fourth preset time from a moment of receiving the second preset read latency signal;

wherein, a sum of the second preset time, the third preset time and the fourth preset time is equal to the first preset time.

~~21~~17. The data transmission circuit according to claim ~~20~~16, wherein the third delay unit comprises:

a first sub-delay unit connected to the output terminal of the second delay unit, wherein the first sub-delay unit is configured to generate a third preset read latency signal after delaying a fifth preset time from a moment of receiving the second preset read latency signal, wherein the fifth preset time is equal to an operation delay of a read-write amplifier; and

a second sub-delay unit connected to an output terminal of the first sub-delay unit and the input terminal of the data processing unit of the mode register; wherein the second sub-delay unit is configured to generate the preset read latency signal after delaying a sixth preset time from a moment of receiving the third preset read latency signal; and

wherein a sum of the fifth preset time and the sixth preset time is equal to the fourth preset time~~.~~;

~~22. The data transmission circuit according to any one of claims 19-21,~~ wherein the data memory unit of the array region comprises a plurality of first memory units, and an output terminal of each of the plurality of first memory unit is connected to a first node, wherein an input terminal of each of plurality of first memory units is connected to a first data signal line, and wherein the first data signal line is configured to transmit the data of the array region~~.~~;

~~23. The data transmission circuit according to claim 22,~~ wherein a driving clock frequency of the first pointer signal and a driving clock frequency of the second pointer signal are the same.

~~24~~18. The data transmission circuit according to any one of claims ~~19~~15-~~21~~17, wherein the data processing unit of the mode register comprises:

a read command processing unit of the mode register, configured to generate the first clock signal according to a received read command of the mode register, a second clock signal, and the preset read latency signal;

a first-in first-out pointer processing unit, configured to generate a third pointer signal and a fourth pointer signal in response to the read command of the mode register; and

a first-in first-out data processing unit connected to both the first-in first-out pointer processing

unit and the data memory unit of the mode register, wherein the first-in first-out data processing unit is configured to read data of the mode register from the mode register in response to the third pointer signal, and to output the data of the mode register to the data memory unit of the mode register in response to the fourth pointer signal~~.~~;

~~25. The data transmission circuit according to claim 24,~~ wherein a driving clock frequency of the third pointer signal and a driving clock frequency of the fourth pointer signal are the same.

~~26~~19. The data transmission circuit according to claim ~~24~~18, further comprising:

a command decoding circuit, comprising a first output terminal connected to an input terminal of the read command processing unit of the mode register and an input terminal of the first-in first-out pointer processing unit, wherein the command decoding circuit is configured to receive a read command, decode the read command and judge whether the read command is a read command of the mode register; and wherein the command decoding circuit is configured to output the read command of the mode register in response to the read command being the read command of the mode register, and to generates an data read command of the array region in response to the read command not being the read command of the mode register; and

a data processing unit of the array region, comprising an input terminal connected to a second output terminal of the command decoding circuit, wherein the data processing unit of the array region is configured to read data of the array region from a memory unit array in response to the data read command of the array region and to provide the data of the array region to the data memory unit of the array region.

~~27~~20. A memory device, comprising:

a memory unit array configured to store data of an array region;

a mode register configured to store data of the mode register; and

a data transmission circuit according to any one of claims 1-~~26~~19.

~~28. A data transmission method, comprising:~~

~~outputting, by a data memory unit of a mode register, data of the mode register in response to a first clock signal; and~~

~~receiving, by a data memory unit of an array region, data of the array region in response to a first pointer signal, and outputting the data of the array region in response to a second pointer signal;~~

~~wherein an output terminal of the data memory unit of the array region and an output terminal of~~

the data memory unit of the mode register are both connected to a first node.

29. A data transmission method, comprising:

generating, by a controllable delay module, a preset read latency signal in response to a read command of a mode register;

reading, by a data processing unit of the mode register, data of the mode register in response to the read command of the mode register, and outputting the mode register data to a data memory unit of the mode register in response to the preset read latency signal;

outputting, by the data memory unit of the mode register, the data of the mode register in response to a first clock signal; and

receiving, by a data memory unit of an array region, data of the array region in response to a first pointer signal, and outputting the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.

30. A data transmission method, comprising:

generating, by a delay module, a preset read latency signal after delaying a first preset time from a moment of receiving a read command of a mode register;

reading, by a data processing unit of the mode register, data of the mode register in response to the read command of the mode register, and outputting the mode register data to a data memory unit of the mode register in response to the preset read latency signal;

outputting, by the data memory unit of the mode register, the data of the mode register in response to a first clock signal; and

receiving, by a data memory unit of an array region, data of the array region in response to a first pointer signal, and outputting the data of the array region in response to a second pointer signal, wherein an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to a first node.