CLAIMS

What is claimed is:

1. A microelectronic structure comprising:

a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface, wherein the microelectronic substrate includes a plurality of conductive routes extending from the substrate first surface and a plurality of conductive routes extending from the substrate cavity bottom surface;

a bridge, disposed within the microelectronic substrate cavity, having a plurality of signal lines formed on or in a first surface of the bridge and a plurality of through-bridge conductive vias extending from the bridge first surface to an opposing second surface of the bridge, wherein the plurality of through-bridge conductive vias are electrically connected to the plurality of conductive routes extending from the microelectronic substrate bottom surface; and

a plurality of microelectronic devices, wherein each of the plurality of microelectronic devices are electrically connected to at least one of the plurality of conductive routes extending from the substrate first surface, at least one of the plurality of the bridge signal lines, and at least one of the plurality of through-bridge conductive vias.

2. The microelectronic structure of claim 1, wherein the bridge comprises silicon-containing components.

3. The microelectronic structure of claim 1, wherein the bridge comprises a passive structure.

4. The microelectronic structure of claim 1, wherein the bridge comprises an active structure.

5. The microelectronic structure of claim 1, wherein the bridge comprises a silicon substrate having an interconnection layer on a first surface thereof, wherein the interconnection layer comprises at least one dielectric layer formed on the silicon substrate first surface; wherein a plurality of bridge first surface bond pads and the plurality of bridge signal lines are formed in or on the dielectric layer; and further comprising a dielectric liner disposed between the through-bridge conductive vias and the silicon substrate.

6. The microelectronic structure of claim 1, wherein the microelectronic substrate comprises a plurality of dielectric layers having the plurality of conductive routes formed therein.

7. The microelectronic structure of claim 6, wherein the conductive routes comprise at least one conductive trace formed on at least one of the plurality of dielectric layers and at least one conductive via extending through at least one of the plurality of dielectric layers.

8. The microelectronic structure of claim 1, wherein at least one of the plurality of microelectronic devices is attached to the microelectronic substrate and to the bridge through a plurality of interconnects.

9. The microelectronic structure of claim 8, wherein at least one of the plurality of interconnects extends between one of a plurality of bond pads on an active surface of one microelectronic device and a corresponding substrate bond pads, and another of the plurality of interconnects extends between another of plurality of the microelectronic device bond pads and a corresponding bond pad of a plurality of bond pads on a first surface of the bridge.

10. The microelectronic structure of claim 1, further including a plurality of bond pads formed in or on the bridge second surface to contact corresponding through-bridge conductive vias and attached to corresponding substrate cavity bond pads formed in or on the substrate cavity bottom surface through a plurality of bridge-to-substrate interconnects.

11. A computing device, comprising:

a board;

a microelectronic device attached to the board; and

a microelectronic structure disposed within the microelectronic device, wherein the microelectronic structure comprises:

a microelectronic substrate having a cavity defined therein extending from a first surface of the microelectronic substrate, wherein the cavity includes at least one sidewall and a bottom surface, wherein the microelectronic substrate includes a plurality of conductive routes extending from the substrate first surface and a plurality of conductive routes extending from the substrate cavity bottom surface;

a bridge disposed within the microelectronic substrate having a plurality of signal lines formed on or in a first surface of the bridge and a plurality of through-bridge conductive vias extending from the bridge first surface to an opposing second surface of the bridge, wherein the plurality of through-bridge conductive vias are electrically connected to the plurality of conductive routes extending from the microelectronic substrate bottom surface; and

a plurality of microelectronic devices, wherein each of the plurality of microelectronic devices are electrically connected to at least one of the plurality of conductive routes extending from the substrate first surface, at least one of the plurality of the bridge signal lines, and at least one of the plurality of through-bridge conductive vias.

12. The computing device of claim 11, wherein the bridge comprises a silicon substrate having an interconnection layer on a first surface thereof, wherein the interconnection layer comprises at least one dielectric layer formed on the silicon substrate first surface; wherein a plurality of bridge first surface bond pads and the plurality of bridge signal lines are formed in or on the dielectric layer; and

further comprising a dielectric liner disposed between the through-bridge conductive vias and the silicon substrate.

13. The computing device of claim 11, wherein at least one of the plurality of microelectronic devices is attached to the microelectronic substrate and to the bridge through a plurality of interconnects, wherein at least one of the plurality of interconnects extends between one of a plurality of bond pads on an active surface of one microelectronic device and a corresponding substrate bond pads, and another of the plurality of interconnects extends between another of plurality of the microelectronic device bond pads and a corresponding bond pad of a plurality of bond pads on a first surface of the bridge.

14. The computing device of claim 11, further including a plurality of bond pads formed in or on the bridge second surface to contact corresponding through-bridge conductive vias and attached to corresponding substrate cavity bond pads formed in or on the substrate cavity bottom surface through a plurality of bridge-to-substrate interconnects.

15. The computing device of claim 11, wherein the bridge comprises silicon-containing components.

16. The computing device of claim 11, wherein the bridge comprises a passive structure.

17. The computing device of claim 11, wherein the bridge comprises an active structure.

18. The computing device of claim 11, wherein the microelectronic substrate comprises a plurality of dielectric layers having the plurality of conductive routes formed therein.

19. The computing device of claim 11, wherein the conductive routes comprise at least one conductive trace formed on at least one of the plurality of dielectric layers and at least one conductive via extending through at least one of the plurality of dielectric layers.

20. The computing device of claim 11, wherein at least one of the plurality of microelectronic devices is attached to the microelectronic substrate and to the bridge through a plurality of interconnects.