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SEMICONDUCTOR PLANARIZATION PROCESS

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The invention relates to the planarization of glass layers used in semiconductors.

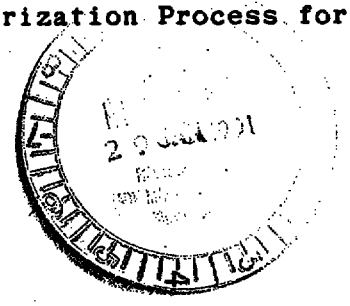
2. Prior Art.

Glass layers are frequently used in the fabrication of semiconductor integrated circuits. For example, these insulative layers are used in metal-oxide-semiconductor (MOS) circuits over polysilicon members to insulate them from overlying metal lines, and between layers of metal lines.

When a glass layer is deposited over underlying members an undulating contour frequently results. When a metal layer is formed on this surface, several problems occur which are a direct result of the non-planarized surface. For instance, stress cracks can occur in the metal at abrupt corners and voids beneath the metal.

An early solution to this problem consisted of reflowing the glass layer after its formation. See U.S. Patent 3,825,442. It is not always possible to reflow the glass layer. This reflow does not provide a sufficiently planar surface for overlying metal layers in many processes.

Another solution to this problem is to planarize (e.g., flatten) this glass surface through etching. In one technique a spin-on-glass is formed on the surface. The spin-on-glass, because of the spinning during formation, provides a planar surface. Then a plasma etching step is used which etches away both the spin-on-glass and deposited glass until a planar surface of the deposited glass is reached. This technique is described in "A Planarization Process for



Double Metal CMOS Using Spin-on-Glass as a Sacrificial Layer" by Elkins, Reinhart and Tang, IEEE V-MIC Conference, June 9-10, 1986. For other uses of spin-on-glass, see U.S. Patent No. 4,587,138. Also see Application Serial No. 870,234, Filed June 3, 1986, entitled ETCH-BACK PLANARIZATION FOR DOUBLE METAL VLSI, and assigned to the assignee of the present invention.

The present invention is an improvement on the process described in the above-referenced article.

SUMMARY OF THE INVENTION

A planarization process for use in the fabrication of semiconductor integrated circuits is disclosed. A glass layer is coated with a spin-on-glass layer. The glass layer is then cured in an atmosphere of steam in the temperature range of 600 to 650 degrees C. Then the layers are wet etched using an etchant of hydrofluoric acid and nitric acid diluted with acetic acid.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional elevation view of a substrate which includes polysilicon circuit members covered by two layers of glass.

Figure 2 illustrates the substrate of Figure 1 after a glass reflow step.

Figure 3 illustrates the substrate of Figure 2 after a spin-on-glass has been formed and cured.

Figure 4 illustrates the substrate of Figure 3 after a wet etching step.

DETAILED DESCRIPTION OF THE INVENTION

A process for planarizing a glass layer such as used during the fabrication of a metal-oxide-semiconductor integrated circuit is described. In the following description, numerous specific details are set forth such as layer thicknesses in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processing steps have not been described in order not to unnecessarily obscure the present invention in detail.

Referring to Figure 1, a substrate 10 is shown along with two polycrystalline silicon (polysilicon) or refractory metal circuit members 12. This cross-section is intended to show a typical MOS circuit commonly used in p-channel, n-channel or CMOS processing. The invented planarization process can be used over any underlying layers which can withstand the temperatures used in the planarization process. The circuit members 12 are covered with a glass layer 13. In the currently preferred embodiment, layer 13 is a chemical vapor deposited (CVD) boron silicate glass. By way of example, this glass layer may be 4000A thick. In the currently preferred embodiment, a dual glass structure is used, and accordingly, a second glass layer 14 is deposited over layer 13. The second layer comprises a CVD boron and phosphorus silicate glass approximately 1.5 microns thick. This dual glass layer is not, however, necessary for the present invention.

As shown in Figure 1, the upper surface of layer 14 includes numerous abrupt contours such as shown at 15. Generally, these

contours result from the glass layers covering edges of underlying circuit elements such as the polysilicon members 12. If a metal layer is formed on layer 14, the abrupt contours, as mentioned above, can cause problems. When double metal layers are used it is even more important that the upper surface of layer 14 be relatively planar.

In the currently preferred embodiment, the structure of Figure 1 is subject to a reflow step as is commonly used in the semiconductor industry. The substrate is placed in a furnace and the temperature raised to cause the glass layers to reflow. The temperature at which reflow occurs is a function of the particular glass used. For purposes of illustration, the layers 13 and 14 of Figure 1 is are shown as a single layer 16 in Figure 2 after the reflow. Note the upper surface 17 of layer 16 has more gentle contours than layer 14. In practice, even after reflow, the contours of the glass layer are abrupt enough to cause problems with overlying metal layers or planarization of overlying layers such as the insulative layer used between overlying metal layers.

With the present invention, a spin-on-glass layer 19 is formed over the surface 17. Any one of numerous commercially available spin-on-glasses may be used such as one of the inorganic spin-on-glasses. Layer 19 is on the average 3000A thick in the currently preferred embodiment. Since the spin-on-glass is in fact spun-on its upper surface is flat.

Now the spin-on-glass is cured in an atmosphere of steam at a temperature of between approximately 600 degrees C to 650 degrees C. This curing reduces the etching rate of the spin-on-glass in subsequent processing.

Now the substrate is dipped in a wet etchant which preferably etches both the spin-on-glass and underlying glass layer 16 at the same rate. This preserves the planar nature of the structure of Figure 3 and results in the relatively flat surface 20 shown in Figure 4. That is, the structure of Figure 3 is etched down to line 20a shown in Figure 3. By way of example, approximately 1 micron of layer 16 is etched away leaving a thickness of approximately 1 micron on the substrate. With the etchant described below, this requires an approximate 3 minute dip with the etchant at room temperature.

To obtain a 1-to-1 etchant selectivity between layers 16 and 19, a mixture of hydrofluoric acid, nitric acid, diluted in acetic acid is used. By way of example, one part by volume of hydrofluoric acid is mixed with 10 parts of nitric acid in 25 parts of acetic acid. The acetic acid does not assist in the selectivity, but rather is used to dilute the solution and to prevent etching of the wafer back.

Thus, a planarization process has been described which is particularly useful for planarizing a glass surface disposed above polysilicon members which receives a first metal layer.

CLAIMS

1. In the fabrication of a semiconductor integrated circuit, a process for planarizing a glass layer comprising the steps of:

covering said glass layer with a spin-on-glass layer;

curing said spin-on-glass layer in an atmosphere of steam;

wet etching said layers;

whereby a planarized glass layer is formed.

2. The process defined by Claim 1 wherein said curing occurs at a temperature of approximately 600 degrees C to 650 degrees C.

3. The process defined by Claim 2 wherein said wet etching comprises the use of hydrofluoric and nitric acids.

4. The process defined by Claim 3 wherein said acids are diluted.

5. The process defined by Claim 4 wherein said acids are diluted with acetic acid.

6. The process defined by Claims 1 or 3 wherein said glass layer is heated to a sufficient temperature to cause glass reflow prior to covering said glass layer with said spin-on-glass layer.

7. In the fabrication of a semiconductor integrated circuit,

a process for planarizing a glass layer which is formed over underlying polysilicon members comprising the steps of:

covering said glass layer with a spin-on-glass layer;

curing said spin-on-glass layer in an atmosphere of steam at a temperature or approximately 600 degrees C. to 650 degrees C.;

wet etching said layers with an etchant which etches both said layers at approximately the same rate;

whereby a planarized glass layer is formed.

8. The process defined by Claim 7 wherein said wet etchant comprises hydrofluoric and nitric acids.

9. The process defined by Claim 8 wherein said acids are diluted in acetic acid.

10. The process defined by Claims 7 or 9 wherein prior to covering said glass layer with said spin-on-glass layer, said glass layer is subjected to an elevated temperature so as to cause glass reflow.

11. In the fabrication of a semiconductor integrated circuit, a process for planarizing a glass layer substantially as hereinbefore described with reference to the accompanying drawing.

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