22C987

METHOD FOR MAKING A BiCMOS SEMICONDUCTOR DEVICE

This invention relates to a method for making a semiconductor device, and particularly, although not exclusively, to a method for making a semiconductor device having bipolar transistors, CMOS transistors, and MOS capacitors and resistors, formed on a single crystal silicon semiconductor substrate.

A semiconductor device having bipolar transistors and CMOS transistors on a single semiconductor substrate, is generally called a BiCMOS device. Known VLSI-class BiCMOS technology is mainly suitable for use in high-integration and high-speed logic or memory devices, because it has been primarily developed for such devices. Known BiCMOS technology for high-performance memory and logic devices, has been disclosed in ISSCC Digest of Technical Papers, page 212, February 1986 and in CICC Technical Digest, page 68, May 1986, respectively.

In known technology, there are often limits to the performance and application of digital and analogue VLSI devices provided on a single chip, because such devices are not optimized and prepared specifically for MOS elements, bipolar elements, resistors and capacitors, which simultaneously perform precise analog and high-speed, high-integration digital functions. The influence that the interface between a single-crystal emitter region, and polycrystalline silicon in a polycrystalline silicon emitter bipolar transistors element, has upon the characteristic of elements and circuits, has been disclosed in IEEE, ED-34 NO.6, pp 1346-1353, June 1987 and in Symposium VLSI Technical Digest papers, pp 47-48, May 1986.

Preferred embodiments of the present invention aim to improve upon the aforementioned, by providing a method of making a BiCMOS semiconductor device which can be used both in high-integration, high-speed digital devices, and in precise analog devices.

Also, preferred embodiments of the present invention aim to provide an advantageous method of providing, on a single semiconductor chip comprising MOS and bipolar transistors, elements such as MOS capacitors and resistors with effective interconnections.

According to one aspect of the present invention, there is provided a method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping, into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(g) depositing a second polycrystalline silicon layer on the whole substrate, and then etching the second polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor provided in the third substrate region;

(h) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar

transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(i) connecting to a conductive layer through said windows; and

(j) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

According to another aspect of the invention, there is provided a method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping, into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form each first source and drain region of said second MOSFET on a second substrate region;

(g) sequentially growing a third and fourth oxide layer on the whole substrate surface;

(h) forming an oxide spacer in gate sidewalls of the MOSFETs provided in said first and second substrate regions, by etching said third and fourth oxide layers without utilizing a separate mask;

(i) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, collector connecting regions of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and second drain and source regions of the second MOSFET;

(j) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second

substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(k) activating the impurities ion-implanted by the processes of (i) and (j), and, after growing a fifth oxide layer on the whole substrate surface, raising the density of the fifth oxide layer by a thermal process;

(l) forming a window in order to produce an emitter region of the first bipolar transistor provided in the third substrate region, and ion-implanting with the second conductivity-type through said window;

(m) depositing a second polycrystalline silicon layer on the whole substrate, and then etching the second polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor provided in the third substrate region;

(n) ion-implanting, with the second conductivity-type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a sixth oxide layer on the whole substrate, and then activating the ion-implanted impurities by a thermal process, in order to raise the density of the sixth oxide layer;

(o) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(p) connecting to a conductive layer through said windows; and

(q) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

According to yet another aspect of the present invention, there is provided a method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping into the whole surface thereof, with the second conductivity-type, and

then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, each collector connecting region of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and a drain and a source region of the second MOSFET;

(g) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(h) activating the impurities ion-implanted by the processes of (f) and (g), and, after growing a fifth oxide layer on the whole substrate surface, raising the density of the fifth oxide layer by a thermal process;

(i) forming a window in order to produce an emitter region of the first bipolar transistor provided in the third substrate region, and ion-implanting with the second conductivity-type through said window;

(j) depositing a second polycrystalline silicon layer on the whole substrate, and then etching the second polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor provided in the third substrate region;

(k) ion-implanting, with the second conductivity-type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a sixth oxide layer on the whole substrate, and then activating the ion-implanted impurities by a thermal process, in order to raise the density of the sixth oxide layer;

(l) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(m) connecting to a conductive layer through said windows; and

(n) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

According to still another aspect of the present invention, there is provided a method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping, into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form each first source and drain region of said second MOSFET on a second substrate region;

(g) sequentially growing a third and fourth oxide layer on the whole substrate surface;

(h) forming an oxide spacer in gate sidewalls of the MOSFETs provided in said first and second substrate regions, by etching said third and fourth oxide layers without utilizing a separate mask;

(i) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, collector connecting regions of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and second drain and source regions of the second MOSFET;

(j) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(k) after growing a fifth oxide layer on the whole substrate, performing a thermal process for the activation of the impurities ion-implanted by the processes of (i) and (j) and for raising the density of the fifth oxide layer surface, followed by the formation of an emitter connecting region window of the first bipolar transistor;

(l) after depositing a second polycrystalline silicon layer on the whole substrate, etching the second polycrystalline silicon layer in order to produce a

connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor;

(m) ion-implanting, with the second conductivity type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a sixth oxide layer on the whole substrate, forming an emitter region of the first bipolar transistor through the activation of said ion-implanted impurities, and then performing a thermal process in order to raise the density of the sixth oxide layer;

(n) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(o) connecting to a conductive layer through said windows; and

(p) depositing a protective layer on the whole surface and then exposing a pad for wire-welding.

Another aspect of the present invention includes a method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is

subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form each base region of said first and second bipolar transistors and then activating these to ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, each collector connecting region of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and a drain and a source region of the second MOSFET;

(g) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting

region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(h) after growing a third oxide layer on the whole substrate, performing a thermal process for the activation of the impurities ion-implanted by processes (f) and (g), and for raising the density of the third oxide layer surface;

(i) after depositing the second polycrystalline silicon layer on the whole substrate, etching a second polycrystalline silicon layer on the third substrate region in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor;

(j) forming a window for producing an emitter region of the first bipolar transistor on the third substrate region and ion-implanting with the second conductivity-type through said window;

(k) ion-implanting, with the second conductivity-type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a fourth oxide layer on the whole substrate, and then performing a thermal process in order to activate said ion-implanted impurities and raise the density of the fourth oxide layer so as to produce an emitter region of the first bipolar transistor;

(l) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and

collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(m) connecting to a conductive layer through said windows; and

(n) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

The invention has various alternative and/or optional features, and other aspects of the invention are recited in Claims 2 to 4, 6 to 8, 10 to 12, 14 to 16, and/or 18 appended hereto.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

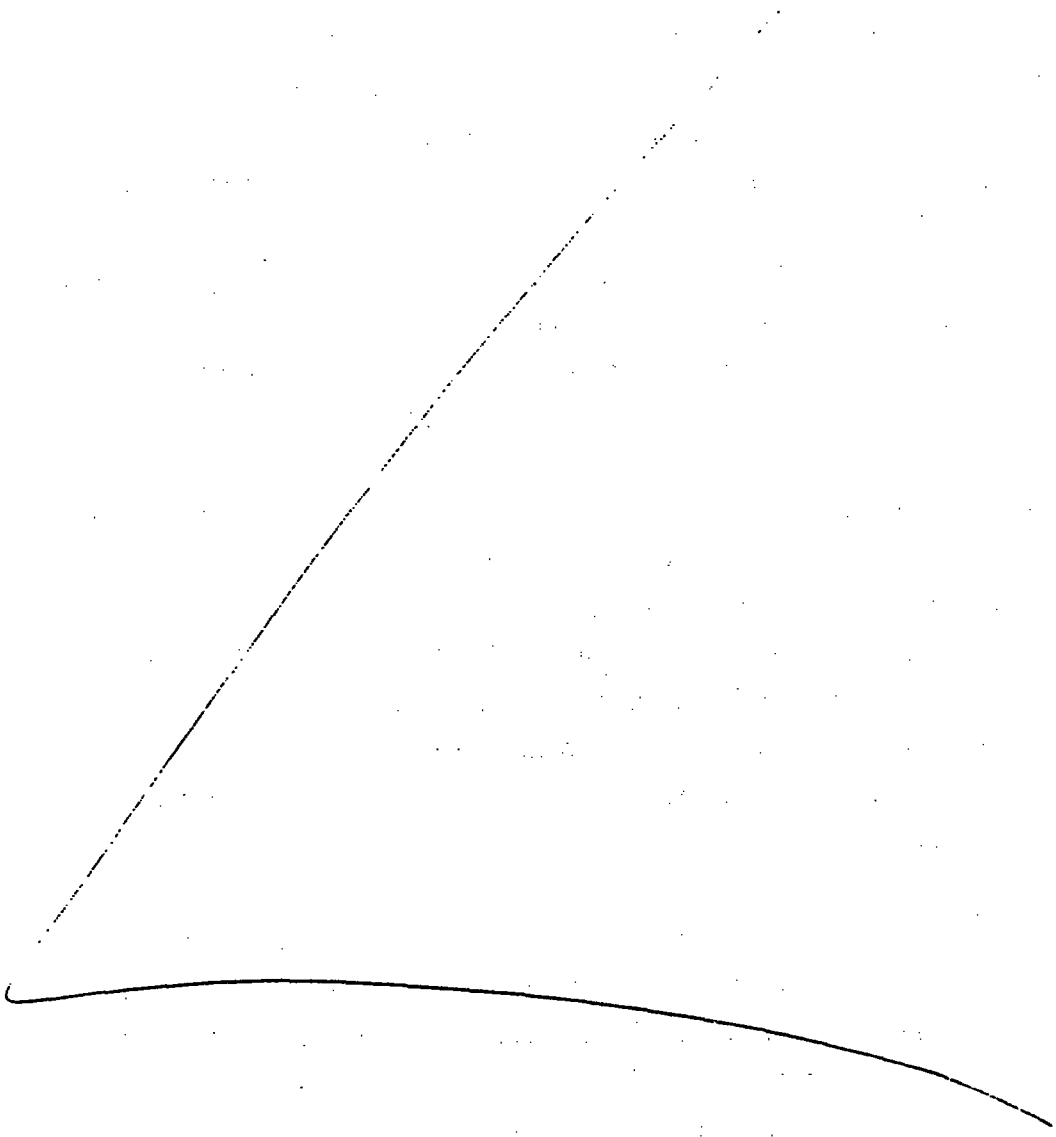
Figures 1 (A)-(T) are cross-sectional views illustrating sequentially processing steps of a preferred embodiment, according to the present invention;

Figures 1(A')-(T') are views, illustrating the cross-section of respective Figure 1(A)-(T) continuing from the right hand side thereof;

Figure 2 is a cross-sectional view of a device fabricated according to the present invention;

Figure 3 is a cross-sectional view of an active element portion in another preferred embodiment according to the present invention;

Figure 4(N)-(T) are cross-sectional views



illustrating process steps of another preferred embodiment according to the present invention.

Referring to Figures 1(A) and 1(A'), a masking silicon oxide layer 2, is coated with <100> orientation and resistivity of 2 - 20 Ω.Cm, on the whole substrate surface of a P-type single crystal silicon substrate 1, by means of a conventional oxidation process. Next, a first photoresist 3 is deposited on the oxide layer 2, and windows 4, 5 and 6 are made by a conventional photolithographic technique, in order to form a substrate region (or well) of a PMOS transistor, and the collector regions of both a polycrystalline silicon emitter NPN transistor, and a metal contact emitter NPN transistor. Next, N-type ion-implanted regions 7, 8 and 9 are formed by means of ion implantation of a group V impurity, such as phosphorus (P), having an energy of about 160 KeV and at a dose of 10^{12} - 10^{14} ions/cm^2. The photoresist 3 acts as a mask during this ion-implantation step.

Upon removal of the photoresist 3 (Figures 1(B) and 1(B')), an N-type first substrate region 10, an N-type third substrate region 11, and an N-type fourth substrate region 12, each having a depth of about 2.5um, are formed, by means of activating and diffusing the N-type ion-implanted regions 7, 8 and 9 under an atmosphere of oxygen and nitrogen and at a temperature between 1000°C and 1200°C.

The substrate region 1, between the first substrate region 10 and the third substrate region 11, may subsequently define a second substrate region wherein a NMOS transistor is formed. After removing all the oxide layer 2 from the substrate 1, an oxide layer 13, having a thickness of about 500Å, is deposited on the

surface of substrate 1, and a nitride layer 14 of Si_3N_4, having a thickness of about 1500Å, is deposited on the oxide layer 13 by conventional Low Pressure CVD (Chemical Vapor Deposition). The oxide layer 13 and nitride layer 14 act as masking layers, in order to prevent the oxidation of silicon on the substrate surface 1 below the masking layers, during the following oxidation process.

A second photoresist 15 is coated on the masking layers 13, 14 by a conventional method. The photoresist 15 covers, a connecting region 100 and a region 101 on the first substrate region 10 which is to be formed into a PMOS FET, a connecting region 103 and a region 102 on the second substrate region which is to be formed into a NMOS FET, regions 104 and 105 which are to be formed into NPN transistors, a MOS capacitor region 106, a resistor region 107 and a connecting region 108.

The second photoresist 15 is next used as an etching mask, so that etching of any nitride layer of nitride layer 14 which is not covered with the mask 15, may be carried out. The second photoresist 15 is then removed.

In order to electrically isolate elements, a third photoresist 16 is deposited, as shown in Figures 1(D) and 1(D'). After forming a P-type ion-implanted region 17, by means of ion implantation of a group III impurity, such as boron having a low energy of about 30 KeV and at a dose of 10^{12} - 10^{14} ions/cm^2, the third photoresist 16 is removed, and a second oxide layer 18 is formed, in regions shown in Figures 1(E) and 1(E'), as follows.

In this oxidation process, an oxide layer is not

grown on a silicon substrate below the masking layers 13, 14, but grown on a region of silicon substrate not protected by the masking layers 13, 14. In addition the ion-implanted region 17 is activated, as shown in Figures 1(E) and 1(E'), so that a high concentration P+ channel stopper 19 is formed, which prevents the formation of a channel between elements. After growing the second oxide layer 18 as aforementioned, the nitride layer 14 may be removed by a conventional etching method without using a mask, and a sacrificial oxide layer 20 (Figures 1(F) and 1(F')) is formed, by a process of thermal sacrificial oxidation, in order to purify the substrate surface.

Next, a fourth photoresist 21 is deposited, in order to form a MOS capacitor as a passive element, as shown in Figures 1(G) and 1(G'). After forming, by means of ion implantation of a group V impurity such as Arsenic (As) at a dose of 10^{15} - 10^{16} ions/cm^2, an N-type ion implanted region 22, in a MOS capacitor region 109, the photoresist 21 is removed. Then, by etching the thin sacrificial oxide layer 20, not by means of a mask, but by means of HF solution, a new second oxide layer 18 is formed, having a thickness equal to the oxide layer 18 plus the oxide layer 20, the remaining part of the substrate being exposed.

Next, an oxide layer 23 is deposited, by a conventional thermal oxidation process to a thickness of 200 - 500 Å on the exposed substrate, in order to form a gate oxide layer of an MOS element and the dielectric of a capacitor, as shown in Figures 1(H) and 1(H'). Between the steps shown in Figures 1(G) and 1(G') to Figures 1(H) and 1(H'), the ion-implanted region 22 is activated to form an electrode region 24 (Figure 1(H')) of an MOS capacitor.

Then, in order to control the threshold voltages of NMOS and PMOS FET's, ion implantation of a group III impurity, such as boron (B) having an energy of about 30 KeV and at a dose of 10^{11} - 10^{13} ions/cm^2, is performed upon the whole silicon substrate. Next, a first polycrystalline silicon 25 is formed by a conventional method. The polycrystalline silicon 25 provides, on the whole silicon substrate, gate electrode material and connecting element material for the MOS transistors, and electrode plate material having a constant area over the dielectric of a capacitor. Group V impurities, such as Phosphorus (P), may be injected to lower the resistance of the first polycrystalline silicon layer 25. For example, the sheet resistance of the first polycrystalline silicon may be about 20Ω/□, measured by way of POCl3, at a temperature 900°.

Next, as shown in Figures 1(I) and 1(I'), a fifth photoresist 26 is provided, in order to leave a polycrystalline silicon layer region 110 over a gate of a PMOS FET, a polycrystalline silicon layer region 111 over a gate of an NMOS FET, a polycrystalline silicon layer 112 of an upper electrode plate region of a capacitor dielectric layer, and a polycrystalline silicon layer region of connecting elements which connect, in a subsequent process, a first polycrystalline silicon region 113 to a second polycrystalline silicon layer.

The polycrystalline silicon layer 25 is removed by a conventional method, followed by the removal of the fifth photoresist 26. Then, a sixth photoresist 27 is deposited in order to form a base region of a bipolar transistor, as shown in Figures 1(J) and 1(J'). A P-type active base region 28 is also formed which region 28 is

subsequently formed into a non-compensated emitter region, by means of ion implantation of a group III impurity such as boron (B) having an energy of about 70 KeV and at a dose of 1 x 10^{12} - 5 x 10^{13} ions/cm^2. After removing the sixth photoresist 27 used as a masking layer, a thermal process is carried out using a conventional method, in order to activate the group III impurity (e.g. boron), implanted into the base region.

Then, a seventh photoresist 29 for a Lightly Doped Drain (LDD) is coated on the silicon surface, as shown in Figures 1(K) and 1(K'). Ion implantation of a group V impurity, such as phosphorus (P), having an energy of about 30 KeV and at a dose of 10^{12} - 10^{14} ions/cm^2, into only a source/drain region of the NMOS FET, results in the formation of source and drain regions 30 of an LDD-type NMOS transistor. After forming the source/drain regions and removing the seventh photoresist 29, an oxide layer 31, having a thickness of about 500 A, is deposited on the first polycrystalline silicon layer, 25 by a conventional thermal oxidation process at a temperature 900°C, and secondly an oxide layer 32 is deposited on the whole silicon surface, by a conventional CVD method, as shown in Figures 1(L) and 1(L').

Thereafter, by processing the oxide layer 31, deposited by the thermal oxidation process, and the oxide layer 32, deposited by the CVD method, through a conventional dry etching method, oxide layer spacers 33, 34 (Figure 1(M)), of side walls of gate electrodes of NMOS and PMOS transistors, are formed, as is a connecting region 114 for a lower electrode of an MOS capacitor. The oxide layer spacer 33 subsequently becomes a mask in an ion implantation process to form high-concentration drain and source regions of an NMOS transistor having LDD

structure, thereby achieving an NMOS transistor having a LDD structure.

An eighth photoresist 35 (Figures 1(N) and 1(N')) is then coated on the silicon surface. Subsequently, by performing ion implantation of a group V impurity, such as Arsenic, having an energy of 40 - 80 KeV and at a dose of 10^{14} - 10^{16} ions/cm^2, there are formed a connecting region 36 of the first substrate region 10 of the PMOS FET, a source/drain region 37 of the NMOS FET, and emitter region 38 of the metal contact emitter NPN transistor, a collector connecting region 39 of the third substrate region 11 of the polycrystalline silicon emitter NPN transistor, a collector connecting region 40 of the fourth substrate region 12 of the metal contact emitter NPN transistor, and a lower region 41 of a resistor. The eighth photoresist 35, is then removed.

In a preferred embodiment of the invention, the NPN transistor is formed after selectively performing LDD ion-implantation with the eleventh photoresist 29 in position, but, in a case wherein the base concentration of the NPN transistor is high enough not to be largely affected by the LDD ion implantation, the NPN transistor with LDD structure, may be formed by carrying out LDD ion-implantation without depositing the seventh photoresist 29.

Referring to Figures 1(O) and 1(O'), a ninth photoresist is deposited on the substrate surface, and a group III impurity, such as boron (B), having a low energy of about 30 KeV, and at a dose of 10^{15} - 10^{16} ions/cm^2 is implanted, thereby to form a source/drain region 43 of the PMOS FET, a connecting region 44 of the substrate 1 of the NMOS FET, a connecting region 45 of

the base 28 of the polycrystalline silicon emitter bipolar NPN transistor, and a connecting region 46 of the base 28 of the metal contact emitter NPN transistor. The ninth photoresist 42 is then removed.

After this processing, an oxide layer 47 is deposited on the whole substrate surface by a conventional CVD method, the density and quality of this oxide layer being determined by a conventional method.

Thereafter, a tenth photoresist 48 is coated on the silicon oxide layer 47. Windows are formed, by a general photolithographic technique, on an emitter region 49 of the polycrystalline silicon emitter NPN transistor, a butting contact 50 of a resistor region, and a contacting region 51 of a first and second polycrystalline silicon. Then a group V impurity , such as Arsenic (As), having an energy of 40 KeV and at a dose of 10^{15} - 10^{16} ions/cm^2, is ion-implanted. Consequently, as shown in Figure 1(P), there are formed an emitter region 52 of the polycrystalline silicon emitter NPN bipolar transistor, a butting contact region 50 of a high-concentration resistor portion adequate for ohmic contact, and a contacting portion 51 of first and second polycrystalline silicon. After removing the tenth photoresist 48, there is formed, by a conventional method, on all the silicon substrate surface, a second polycrystalline silicon layer 53, which can be used for electrode material of a polycrystalline silicon emitter, passive resistor elements made of polycrystalline silicon and connecting material.

As shown in Figures 1(Q) and 1(Q'), an eleventh photoresist 54 is deposited, so as to leave a polycrystalline silicon region 117, a butting contact

region, a second polycrystalline silicon region 118 of the resistor element having sheet resistance of the order of Giga ohms per square (G Ω/[]) unit, a resistor element region 119 of several hundreds Ω/[] which region 119 utilize the second polycrystaline silicon layer of the second polycrystalline silicon portion 120 only in regions to be connected with the first polycrystalline silicon. After removing the polycrystalline silicon layer by a general photolithographic technique, the eleventh photoresist 54 is removed by a conventional method.

Thereafter, a twelfth photoresist 55 is deposited, as shown in Figure 1 (R') in order to selectively control the electrical characteristics of a passive element which is made of polycrystalline silicon. In order to ion-implant a group V impurity such as Arsenic (As) at an appropriate dose concentration into the butting contact portion 50, the portion connecting first and second polycrystalline silicon, and the polycrystalline silicon emitter region, the resistor region 118a having G Ω/[] resistance is masked to protect it from the ion-implantation. This ion-implantation results in polycrystalline silicon having a sheet resistance of several hundreds of Ω/[]. Then, the twelfth photoresist 55 is removed by conventional method.

Next a conventional CVD oxide layer 56 is deposited on the whole silicon surface, and the activation of impurities implanted into the regions 43, 44, 45, 46, 36, 37, 38 and 52, and the cohesion of the oxide layer 56 are carried out by a thermal annealing process.

As shown in Figures 1(S) and 1(S'), a thirteenth photoresist 57 is coated on the whole substrate. Then

the connecting region window 121 of the first substrate region and the source/drain region window 122 in the PMOS FET, the source/drain region window 123 and the connecting region window 124 of the second substrate 1 in the NMOS FET, the base connecting region window 125, the emitter connecting region window 126 and the collector connecting region window 127 in the polycrystalline emitter bipolar NPN transistor, the emitter connecting region window 128, the base connecting region window 129 and the collector connecting region window 130 in the metal contact emitter NPN transistor, and finally, the first and second polycrystalline silicon contacts 131 to 134, are etched.

After removing the thirteenth photoresist 57, a metal layer 58 (Figures 1(T) and 1(T')) is deposited by a conventional vacuum evaporation method.

Next, a fourteenth photoresist is deposited and a metal layer 58 is etched. Consequently, a connecting electrode 135 of the first substrate region 10 and source/drain electrode 136 of the PMOS FET, the source/drain electrode 137 and the second substrate connecting electrode 138 of the NMOS FET, the emitter electrode 139 and the base electrode 140 and the third substrate collector electrode 141 of the polycrystalline silicon emitter bipolar NPN transistor, the emitter electrode 142, the base electrode 143 and the fourth substrate collector electrode 144 of the metal contact emitter bipolar transistor, electrodes 145, 146 of the MOS capacitor, electrodes 147 to 149 of the resistor region having the order of some GΩ/□ or several hundreds of Ω/□ , and an electrode 150 of the contacting region of the first and second polycrystalline silicon, are formed. Then, the fourteenth photoresist 59

is removed by a conventional method.

After removing the fourteenth photoresist 59, the semiconductor device is coated with a protecting layer 60 in order to protect it.

In a preferred embodiment for forming the emitter region of the polycrystalline silicon emitter NPN transistor, as shown in Figure 1(P), the emitter region is formed by means of ion-implantation; the second polycrystalline silicon layer is deposited above the emitter region; N-type ion implantation is carried out on the second polycrystalline silicon layer; the oxide layer is formed over all of the substrate; the ion-implanted impurities are then activated by the thermal process.

However, the emitter region of polycrystalline silicon emitter NPN transistor may also be formed by the following method.

After the step shown in Figure 1(O), the mask layer on the substrate may be removed and the CVD oxide layer formed on the whole substrate. Then, the impurities implanted by the process are activated, and a window for forming the emitter region of the first NPN transistor is made. A connecting part for the second polycrystalline silicon layer is formed on the emitter region with the window and thereon ion-implanted thereon to a high concentration. Then, A CVD oxide layer is deposited on the whole substrate and the thermal process is performed, by which the impurities, implanted into the second polycrystalline silicon layer, are activated, so that the emitter region of the N-type first bipolar transistor, having high concentration, can be formed towards the base region.

Figure 2 shows a cross-sectional view of a complete BiCMOS device manufactured by the fabrication processes according to the present invention, wherein region 'a' comprises the PMOS transistor, region 'b' comprises the NMOS transistor with LDD structure, region 'c' the polycrystalline silicon emitter NPN transistor; region 'd' comprises the metal emitter NPN transistor; region 'e' comprises the MOS capacitor; region 'f' comprises the polycrystalline silicon resistor region having resistance of the order of GΩ/.□; region 'g' comprises the butting contact; region 'h' comprises the polycrystalline silicon resistor of several hundreds of Ω/□; and region 'i' comprises a contacting region which connects the first polycrystalline silicon layer to the second polycrystalline silicon layer.

Figure 3 is a final cross-sectional view showing a portion of active elements in another preferred embodiment according to the present invention. In the previous embodiment shown in Figures 1(A) to (T) and Figures 1(A') to (T), the description of the invention refers mainly to triple diffusion structures of the active elements. However, it should be noted, that the invention will be suitable for the formation of a BiCMOS structure comprising a standard bipolar transistor with a buried layer, and an epitaxial layer, as illustrated in Figure 3.

Referring to the BiCMOS structure, after forming, at low concentration, second conductivity-type buried layers 62, 63, 64 (Figure 3) on a first conductivity-type of single crystal silicon substrate 61, a first conductivity-type of epitaxial layer 65, at high concentration is grown on the whole substrate surface 61.

Thereafter, a first substrate region 66, forming a first MOS transistor having a first conductivity-type channel, and third and fourth substrate regions 67, 68 which comprise first and second bipolar transistors, are formed on the second conductivity-type buried layer 62, 63, and 64 respectively. An epitaxial layer 65, between the first and third substrate regions 66, 67, may be a second substrate region for forming a second MOS transistor. By sequentially performing the processes as shown in Figures 1(C) to 1(T), a BiCMOS semiconductor device of Figure 3 may be manufactured, comprising a P-channel FET, an N-channel FET, a polycrystalline silicon emitter bipolar transistor and a metal contact emitter bipolar transistor. In practice, after an N+ buried layer, located above a P-type single crystal silicon substrate having <100> orientation and resistivity of 0.006 - 0.1 Ω.Cm, has been formed, a P-type epitaxial layer having resistivity of 5 Ω.Cm is grown, and N-type first, third and fourth substrates are formed. Thus, by sequentially carrying out the processes according to Figures 1(C) to 1(T), the BiCMOS device may be manufactured.

Referring to Figure 4 which shows each fabrication step in an another preferred embodiment according to the present invention, processes identical to those shown in Figures 1(A) to 1(J) may be performed on the substrate in which the P-type epitaxial layer of high concentration is deposited, on the P-type single crystal silicon substrate as shown in Figure 1, or on the P-type single crystal silicon layer of low concentration, as shown in Figure 3. Thereafter, the remaining photoresist 27 above the substrate, and the oxide layer 23 above regions for forming elements, are removed.

As shown in Figure 4(N), the eighth photoresist

35 is deposited on the silicon substrate surface and a group V impurity, such as Arsenic (As), with an energy of 40 - 80 KeV, and at a dose of 10^{14} - 10^{16} ions/cm^2, is implanted. Then, a connecting region 36 of the first substrate 10 of the PMOS transistor, a source/drain region 37 of the second substrate of the NMOS transistor, an emitter region 38 of the metal contact emitter NPN transistor, a collector connecting region 39 of the third substrate region 11 of the polycrystalline silicon emitter NPN transistor, a collector connecting region 40 of the fourth substrate region 12 of the metal contact emitter NPN transistor and a lower region 41 (not shown in Figure 4) of the resistor, are formed. Next, the eighth photoresist 35 is removed.

The subsequent processes, after the process of Figure 4(O), are identical to the corresponding ones shown in Figures 1(O) to 1(T).

In Figures 4(N) to 4(T) and Figures 1(N) to 1(T), like reference numerals are used to represent like elements and regions in the same fabrication process.

Figures 4(N) to 4(T) show active elements of a BiCMOS transistor according to the present invention. A portion of passive elements of the Bi-CMOS transistor which is not illustrated in Figures 4(N) to 4(T), may be formed by the aforementioned processes illustrated in Figures 1(A') to 1(T'). The BiCMOS device manufactured in this way, comprises a conventional NMOS transistor, instead of the NMOS transistor with LDD structure shown in the preferred embodiment of Figure 3.

Thus, the invention may provide high integration, high performance MOS transistors in a BiCMOS

semiconductor device, and may further provide high-performance, high precision bipolar transistors having good matching characteristics, together with the formation of an NMOS transistor, thereby enabling their use in precise analog circuits. Also, the invention may be of utility in polycrystalline silicon emitter NPN transistors having a small emitter area, which transistors are particularly suitable in high-speed digital devices and in metal contact emitter NPN transistors which are useful for precise analog circuits and high-load driving power.

Furthermore, the invention may allow optimisation of integration in high quality MOS capacitors. This may be particularly necessary in analog MOS circuits and for polycrystalline silicon resistors providing bias and load in various circuits. The invention may also allow more convenient inter-connections between various elements.

Thus, the invention may provide a high performance digital VLSI circuit such as a logic circuit, a memory, etc. or an analog VLSI circuit, such as a data converter, a switched capacitor circuit, etc. or a composite circuit comprising both, which may be advantageous over known examples.

While the invention has been described with reference to the illustrated embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrated embodiments, and other embodiments of the invention, will be apparent to persons skilled in the art, upon reference to the aforementioned description, without departing from the scope of the invention.

CLAIMS

1. A method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping, into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-

implanted regions;

(f) ion-implanting with the second conductivity-type in order to form each first source and drain region of said second MOSFET on a second substrate region;

(g) sequentially growing a third and fourth oxide layer on the whole substrate surface;

(h) forming an oxide spacer in gate sidewalls of the MOSFETs provided in said first and second substrate regions, by etching said third and fourth oxide layers without utilizing a separate mask;

(i) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, collector connecting regions of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and second drain and source regions of the second MOSFET;

(j) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(k) activating the impurities ion-implanted by the processes of (i) and (j), and, after growing a fifth oxide layer on the whole substrate surface, raising the density of the fifth oxide layer by a thermal process;

(l) forming a window in order to produce an emitter region of the first bipolar transistor provided in the third substrate region, and ion-implanting with the second conductivity-type through said window;

(m) depositing a second polycrystalline silicon layer on the whole substrate, and then etching the second polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor provided in the third substrate region;

(n) ion-implanting, with the second conductivity-type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a sixth oxide layer on the whole substrate, and then activating the ion-implanted impurities by a thermal process, in order to raise the density of the sixth oxide layer;

(o) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(p) connecting to a conductive layer through said windows; and

(q) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

2. A method according to Claim 1, further comprising the steps of:

forming the first oxide layer between said respective element regions with the exception of a region to thereon form a capacitor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to form a lower electrode of a capacitor in the capacitor region after process (b);

forming an oxide dielectric layer over the lower electrode of the capacitor in addition to forming the gate oxide layers of the first and the second MOSFETs in process (c);

forming an upper electrode of the capacitor in addition to forming the polycrystalline silicon gates of the first and the second MOSFETs in process (d);

forming a connector region for the lower electrode of the capacitor, in addition to forming the oxide spacer of gate sidewalls of the first and the second MOSFETs in process (h);

forming a connecting window for the capacitor region in addition to forming windows for every region in process (o);

connecting to the conductive layer through said windows in said process (p); and

depositing a protective layer on the whole substrate surface and then exposing the pad for wire-welding in process (q).

3. A method according to Claim 1 or 2, further comprising the steps of:

forming the first oxide layer between said respective element regions and a resistor region with the exception of a region to form a substrate connecting region of the resistor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

forming an ion-implantation region under the substrate connecting region of said resistor in process (i);

forming a connecting window, and ion-implanting a butting contact portion of the resistor region in process (l);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (m);

ion implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (n);

forming a connecting window for the resistor region in said process (o);

connecting to the conductive layer through said windows in process (p); and

depositing the protective layer and exposing the pad for wire-welding in process (q).

4. A method according to Claim 3, further comprising the steps of:

forming the first oxide layer between said regions with the exception of the regions to form the capacitor region and the substrate connecting region of the resistor, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to produce a lower electrode of the capacitor in the capacitor region after process (b);

growing an oxide dielectric layer over the lower electrode of the capacitor in process (c);

forming the upper electrode of said capacitor in process (d);

forming the lower electrode connecting region of said capacitor and the substrate connecting region of the resistor in process (h);

forming an ion-implantation region below a substrate connecting region of said resistor in process (i);

forming a connecting window and ion-implanting the butting contact portion of said resistor region in process (l);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (m);

* C L M S *

ion-implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (n);

forming connecting windows for the resistor and the capacitor regions in process (o);

connecting to the conductive layer through said windows in process (p); and

depositing the protective layer and exposing the pad for wire-welding in process (q).

5. A method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, each collector connecting region of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and a drain and a source region of the second MOSFET;

(g) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(h) activating the impurities ion-implanted by the processes of (f) and (g), and, after growing a fifth oxide layer on the whole substrate surface, raising the density of the fifth oxide layer by a thermal process;

(i) forming a window in order to produce an emitter

* C L M S *

region of the first bipolar transistor provided in the third substrate region, and ion-implanting with the second conductivity-type through said window;

(j) depositing a second polycrystalline silicon layer on the whole substrate, and then etching the second polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor provided in the third substrate region;

(k) ion-implanting, with the second conductivity-type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a sixth oxide layer on the whole substrate, and then activating the ion-implanted impurities by a thermal process, in order to raise the density of the sixth oxide layer;

(l) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(m) connecting to a conductive layer through said windows; and

(n) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

6. A method according to Claim 5, further comprising the steps of:

forming the first oxide layer between said respective element regions with the exception of a region to thereon form a capacitor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to form a lower electrode of a capacitor in the capacitor region after process (b);

forming an oxide dielectric layer over the lower electrode of the capacitor in addition to forming the gate oxide layers of the first and the second MOSFETs in process (c);

forming an upper electrode of the capacitor, in addition to forming the polycrystalline silicon gates of the first and the second MOSFETs in process (d);

forming a connector region for the lower electrode of the capacitor, after process (e);

forming a connecting window for the capacitor region in addition to forming said windows for every region in process (l);

connecting to the conductive layer through said windows in process (m); and

depositing a protective layer on the whole substrate surface and then exposing the pad for wire-welding in process (n);

7. A method according to Claim 6, further comprising the steps of:

* C L M S *

forming the first oxide layer between said respective element regions and a resistor region with the exception of a region to form a substrate connecting region of the resistor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

forming the substrate connecting region of the resistor after process (e);

forming an ion-implantation region under the substrate connecting region of said resistor in process (f);

forming a connecting window and ion-implanting the butting contact portion of the resistor region in process (i);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (j);

ion-implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (k);

forming a connecting window for the resistor region in process (l);

connecting to the conductive layer through said windows in process (m); and

depositing the protecting layer and exposing the pad for wire-welding in process (n).

8. A method according to Claim 7, further comprising the steps of:

forming the first oxide layer between said regions with the exception of the regions to form the capacitor region and the substrate connecting region of the resistor, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to produce a lower electrode of the capacitor in the capacitor region after process (b);

growing an oxide dielectric layer over the lower electrode of the capacitor in process (c);

forming the upper electrode of said capacitor in process (d);

forming the lower electrode connecting region of said capacitor and the substrate connecting region of the resistor after process (e);

forming an ion-implantation region below a substrate connecting region of said resistor in process (f);

forming a connecting window and ion-implanting the butting contact portion of said resistor region in process (i);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (j);

* C L M S *

ion-implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (k);

forming connecting windows for the resistor and the capacitor regions in process (l);

connecting to the conductive layer through said windows in process (m); and

depositing the protective layer and exposing the pad for wire-welding in process (n).

9. A method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer

of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping, into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form each first source and drain region of said second MOSFET on a second substrate region;

(g) sequentially growing a third and fourth oxide layer on the whole substrate surface;

(h) forming an oxide spacer in gate sidewalls of the MOSFETs provided in said first and second substrate regions, by etching said third and fourth oxide layers without utilizing a separate mask;

(i) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, collector connecting regions of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and second drain and source regions of the second MOSFET;

(j) ion-implanting with the first conductivity-type in order to form drain and source regions of the first

MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(k) after growing a fifth oxide layer on the whole substrate, performing a thermal process for the activation of the impurities ion-implanted by the processes of (i) and (j) and for raising the density of the fifth oxide layer surface, followed by the formation of an emitter connecting region window of the first bipolar transistor;

(l) after depositing a second polycrystalline silicon layer on the whole substrate, etching the second polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor;

(m) ion-implanting, with the second conductivity type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a sixth oxide layer on the whole substrate, forming an emitter region of the first bipolar transistor through the activation of said ion-implanted impurities, and then performing a thermal process in order to raise the density of the sixth oxide layer;

(n) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(o) connecting to a conductive layer through said windows; and

(p) depositing a protective layer on the whole surface and then exposing a pad for wire-welding.

10. A method according to Claim 9, further comprising the steps of:

forming the first oxide layer between said respective element regions with the exception of a region to thereon form a capacitor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to form a lower electrode of a capacitor in the capacitor region after process (b);

forming an oxide dielectric layer over the lower electrode of the capacitor in addition to forming the gate oxide layers of the first and the second MOSFETs in process (c);

forming an upper electrode of the capacitor, in addition to forming the polycrystalline silicon gates of the first and the second MOSFETs in process (d);

forming a connector region for the lower electrode of the capacitor, in addition to forming the oxide spacer of gate sidewalls of the first and the second MOSFETs in process (h);

forming a connecting window for the capacitor region in addition to forming windows for every region in

process (n);

connecting to the conductive layer through said windows in process (o); and

depositing a protective layer on the whole substrate surface and then exposing the pad for wire-welding in process (p).

11. A method according to Claim 10, further comprising the steps of:

forming the first oxide layer between said respective element regions and a resistor region with the exception of a region to form a substrate connecting region of the resistor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

forming the substrate connecting region of the resistor in process (h);

forming an ion-implantation region under the substrate connecting region of said resistor and then forming a connecting window of butting contact portion of the resistor region in process (i);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (l);

ion-implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (m);

forming a connecting window for the resistor region in process (n);

connecting to the conductive layer through said windows in process (o); and

depositing the protective layer and exposing the pad for wire-welding in process (p).

12. A method according to Claim 11, further comprising the steps of:

forming the first oxide layer between said regions with the exception of the regions to form the capacitor region and the substrate connecting region of the resistor, and the first conductively-type of channel stopper region below the first oxide layer in said process (b);

ion-implanting in order to produce a lower electrode of the capacitor in the capacitor region after process (b);

growing an oxide dielectric layer over the lower electrode of the capacitor in process (c);

forming the upper electrode of said capacitor in process (d);

forming the lower electrode connecting region of said capacitor and the substrate connecting region of the resistor in process (h);

forming an ion-implantation region below a

substrate connecting region of said resistor in process (i);

forming a connecting window of the butting contact portion of said resistor region in process (k);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (l);

ion-implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (m);

forming connecting windows for the resistor and the capacitor regions in process (n);

connecting to the conductive layer through said windows in process (o); and

depositing the protecting layer and exposing the pad for wire-welding in process (p).

13. A method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region located between the first and third substrate regions,

and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produce each gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form each base region of said first and second bipolar transistors and then activating these to ion-implanted regions;

(f) ion-implanting with the second conductivity-type in order to form a connecting region of the first substrate region, each collector connecting region of the third and fourth substrate regions, an emitter region of the second bipolar transistor, and a drain and a source region of the second MOSFET;

(g) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the

first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(h) after growing a third oxide layer on the whole substrate, performing a thermal process for the activation of the impurities ion-implanted by processes (f) and (g), and for raising the density of the third oxide layer surface;

(i) after depositing the second polycrystalline silicon layer on the whole substrate, etching a second polycrystalline silicon layer on the third substrate region in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor;

(j) forming a window for producing an emitter region of the first bipolar transistor on the third substrate region and ion-implanting with the second conductivity-type through said window;

(k) ion-implanting, with the second conductivity-type, into the second polycrystalline silicon of an emitter connecting region of the first bipolar transistor, growing a fourth oxide layer on the whole substrate, and then performing a thermal process in order to activate said ion-implanted impurities and raise the density of the fourth oxide layer so as to produce an emitter region of the first bipolar transistor;

(l) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate

regions of the first and second MOSFETs;

(m) connecting to a conductive layer through said windows; and

(n) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

14. A method according to Claim 13, further comprising the steps of:

forming the first oxide layer between said respective element regions with the exception of a region to thereon form a capacitor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to form a lower electrode of a capacitor in the capacitor region after process (b);

forming an oxide dielectric layer over the lower electrode of the capacitor in addition to forming the gate oxide layers of the first and the second MOSFETs in process (c);

forming an upper electrode of the capacitor in addition to forming the polycrystalline silicon gates of the first and the second MOSFETs in process (d);

forming a connecting region for the lower electrode of the capacitor after process (e);

forming a connecting window for the capacitor region in addition to forming said windows for every

regions in process (l);

connecting to the conductive layer through said windows in process (m); and

depositing a protecting layer on the whole substrate surface and then exposing the pad for wire-welding in said process (n).

15. A method according to Claim 14, further comprising the steps of:

forming the first oxide layer between said respective element regions and a resistor region with the exception of a region to form a substrate connecting region of the resistor region, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

forming the substrate connecting region of the resistor after process (e);

forming an ion-implantation region under the substrate connecting region of said resistor in process (f);

forming a connecting window of the butting contact portion of the resistor region in process (i);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (j);

ion-implanting with the second conductivity-type into the butting contact portion and the low resistance

portion of the resistor region in process (k);

forming a connecting window for the resistor region in process (l);

connecting to the conductive layer through said windows in process (m); and

depositing the protecting layer and exposing the pad for wire-welding in process (n).

16. A method according to Claim 15, further comprising the steps of:

forming the first oxide layer between said regions with the exception of the regions to form the capacitor region and the substrate connecting region of the resistor, and the first conductivity-type of channel stopper region below the first oxide layer in process (b);

ion-implanting in order to produce a lower electrode of the capacitor in the capacitor region after process (b);

growing an oxide dielectric layer over the lower electrode of the capacitor in process (c);

forming the upper electrode of said capacitor in process (d);

forming the lower electrode connecting region of said capacitor and the substrate connecting region of the resistor in process (h);

forming an ion-implantation region below a substrate connecting region of said resistor in process (i);

forming a connecting window of butting contact portion of said resistor region in process (i);

forming a high resistance portion, a butting contact portion and a low resistance portion of the resistor region in process (j);

ion-implanting, with the second conductivity-type, into the butting contact portion and the low resistance portion of the resistor region in process (k);

forming connecting windows for the resistor and the capacitor regions in process (l);

connecting to the conductive layer through said windows in process (m);

depositing the protecting layer and exposing the pad for wire-welding in process (n).

17. A method of making a BiCMOS semiconductor device including first and second MOSFETs and first and second bipolar transistors provided on a first conductivity-type silicon substrate, the method comprising the steps of:

(a) producing, by ion-implantation of a second conductivity-type on the substrate, a first substrate region on which to form the first MOSFET, and a third and fourth substrate region on which to form respective first and second bipolar transistors, wherein a second MOSFET is subsequently formed in a second substrate region

located between the first and third substrate regions, and then the ion-implanted regions are activated;

(b) forming a first oxide layer between said regions, in order to isolate respective transistor elements on said substrate and a first conductivity-type of channel stopper region below said first oxide layer;

(c) growing a second oxide layer on the whole substrate surface in order to form each gate oxide layer of said first and second MOSFETs;

(d) depositing a first polycrystalline silicon layer on said second oxide layer, doping, into the whole surface thereof, with the second conductivity-type, and then etching the first polycrystalline silicon layer so as to produceach gate of said first and second MOSFETs on respective first and the second substrate regions;

(e) ion-implanting with the first conductivity-type, in order to form base region of said first and second bipolar transistors and then activating these ion-implanted regions;

(f) ion-implanting with the first conductivity-type in order to form drain and source regions of the first MOSFET provided in the first substrate region, a connecting region of the second MOSFET provided in the second substrate region, a base connecting region of the first bipolar transistor provided in the third substrate region and a base connecting region of the second bipolar transistor provided in the fourth substrate region;

(g) depositing a second polycrystalline silicon layer on the whole substrate, and then etching the second

* C L M S *

polycrystalline silicon layer in order to produce a connecting portion for a polycrystalline silicon emitter region of the first bipolar transistor provided in the third substrate region;

(h) forming windows for each source and drain regions of the first and second MOSFETs, each emitter, base and collector regions of the first and second bipolar transistors and each connecting region of the substrate regions of the first and second MOSFETs;

(i) connecting to a conductive layer through said windows; and

(j) depositing a protective layer on the whole substrate surface and then exposing a pad for wire-welding.

18. A method of making a BiCMOS semiconductor device, the method being substantially as hereinbefore described with reference to the accompanying drawings.