

CLAIMS

1. A semiconductor device package, comprising:
 - a plurality of package contacts; and
 - a semiconductor die, including—
 - a plurality of first die bond pads having dedicated first pin assignments,
 - a plurality of second die bond pads having dedicated second pin assignments,
 - a plurality of duplicate die bond pads having the same dedicated second pin assignments as the second die bond pads, and
 - an integrated circuit operably coupled to the package contacts via the plurality of first die bond pads and either the second die bond pads or the duplicate die bond pads, but not both,
 - wherein the integrated circuit is configured to be programmed into one of (1) a first pad state in which the first and second die bond pads are enabled for use with the package contacts or (2) a second pad state in which the first and duplicate die bond pads are enabled for use with the package contacts.
2. The semiconductor device package of claim 1 wherein the integrated circuit is further configured to:
 - disable the duplicate die bond pads in the first pad state; or
 - disable the second die bond pads in the second pad state.
3. The semiconductor device package of claim 1 wherein the semiconductor die further includes a perimeter and first and second die edges at opposite sides of the perimeter, and wherein the first and second die bond pads are adjacent the first die edge, and wherein the duplicate die bond pads are adjacent the second die edge.
4. The semiconductor device package of claim 3, further comprising a package substrate carrying the semiconductor die, wherein:
 - the package substrate includes a plurality of intermediate bond pads wirebonded to corresponding ones of the first and second die bond pads, and a plurality of conductive traces electrically coupling the intermediate bond pads to the package contacts; and
 - the package contacts are formed on the package substrate beneath the semiconductor die.
5. The semiconductor device package of claim 4 wherein the first die bond pads are proximate to first and second die corner regions adjacent the first edge, the second die bond pads are positioned medially along the first edge between the first and second die corner regions, and the duplicate die

bond pads are proximate to third and fourth die corner regions adjacent the second die edge.

6. The semiconductor device package of claim 1, further comprising a casing at least partially encapsulating the semiconductor die, wherein the package contacts include metal leads extending through the package casing and wirebonded to corresponding ones of the first die bond pads and the duplicate die bond pads.

7. The semiconductor device package of claim 1 wherein the integrated circuit includes non-volatile memory, and wherein the non-volatile memory is configured to store at least one of a first value indicative of the first pad state and a second value indicative of the second pad state.

8. The semiconductor device package of claim 7 wherein the non-volatile memory is further configured to store a value indicative of a third pad state in which both the second die bond pads and the duplicate die bond pads are disabled for use.

9. The semiconductor device package of claim 1 wherein the integrated circuit includes a memory component and a plurality of data lines for accessing the memory component, and wherein each of the first, second, and duplicate pin assignments is associated with one of the data lines.

10. A semiconductor device, comprising:
a package casing;
a plurality of package contacts along at least one side of the package casing; and
a memory die at least partially encased in the package casing, wherein the memory die includes an active surface and first, second, and third groups of die bond pads positioned at different regions of the active surface, wherein—
the first and second groups of die bond pads are electrically coupled to corresponding ones of the package contacts,
the third group of die bond pads is electrically disconnected from the package contacts,
the first group of die bond pads has first pin assignments,
the second group of die bond pads has second pin assignments that are different than the first pin assignments,
the third group of die bond pads has third pin assignments that are the same as the second pin assignments, and
the memory die is configured to be programmed into (1) a first pad state in which the first and second groups of die bond pads are enabled for use and (2) a second pad state in which the first and

third groups of die bond pads are enabled for use.

11. The semiconductor device of claim 10 wherein:

the package contacts are arrayed in a ball grid array (BGA) configuration; and

the memory die is configured to be programmed into (1) the first pad state in which the first and second groups of die bond pads are enabled for use in the BGA configuration and (2) the second pad state in which the first and third groups of die bond pads are enabled for use in a configuration of package contacts other than the BGA configuration.

12. The semiconductor device of claim 10 wherein:

the package contacts are arrayed in a small outline integrated circuit (SOIC) configuration;

and

the memory die is configured to be programmed into (1) the first pad state in which the first and second groups of die bond pads are enabled for use in the SOIC configuration and (2) the second pad state in which the first and third groups of die bond pads are enabled for use in a configuration other than the SOIC configuration.

13. A semiconductor device comprising:

an active surface and first, second, and third groups of die bond pads positioned at different regions of the active surface, wherein—

the first group of die bond pads has first pin assignments,

the second group of die bond pads has second pin assignments that are different from the first pin assignments, and

the third group of die bond pads has third pin assignments that are the same as the second pin assignments,

wherein the semiconductor device is configured to selectively enable one of (1) the second group of bond pads and (2) the third group of bond pads.

14. The semiconductor device of claim 13 further comprising a semiconductor device package including a first group of package contacts coupled to the first group of bond pads, and a second group of package contacts coupled to the enabled one of (1) the second group of bond pads and (2) the third group of bond pads.

15. The semiconductor device of claim 14 wherein package contacts include metal leads extending through the package casing and wirebonded to the first and third group of die bond pads.

16. The semiconductor device of claim 14 wherein package contacts include metal bumps beneath the semiconductor die and electrically coupled to the first and third groups of die bond pads.