WHAT IS CLAIMED IS:

1. A nonvolatile memory (NVM) device comprising:

a data pin;

a control pin;

an on-die termination (ODT) pin; and

a plurality of NVM chips commonly connected to the data pin, the control pin, and the ODT pin,

wherein a first NVM chip among the NVM chips comprises an ODT circuit,

wherein the first NVM chip determines one of an ODT write mode and an ODT read mode based on a control signal received through the control pin and an ODT signal received through the ODT pin, uses the ODT circuit to perform an ODT on the data pin during the ODT write mode, and uses the ODT circuit to perform the ODT on the control pin during the ODT read mode,

wherein the control signal indicates whether one of a read operation and a write operation is to be performed, and

wherein the plurality of NVM chips commonly receives the ODT signal.

2. The NVM device of claim 1, wherein the ODT signal indicates whether the ODT is to be performed.

3. The NVM device of claim 1, wherein the ODT circuit is used to perform the ODT when data is read from or written to a second NVM chip among the NVM chips.

4. The NVM device of claim 1, wherein the ODT circuit is used to perform the ODT while the first NVM chip is deselected and a second NVM chip among the NVM chips is selected using a chip enable signal.

5. The NVM device of claim 1, wherein the NVM device further comprises a data strobe pin for receiving a data strobe signal, and the NVM chips are commonly connected to the data strobe pin.

6. The NVM device of claim 5, wherein the first NVM chip activates a write ODT enable signal during a preamble section of the data strobe signal before a toggling section of the data strobe signal when the ODT signal is activated and the control signal is inactivated, and uses the ODT circuit to perform the ODT on the data pin and the data strobe pin when the write ODT enable signal is activated.

7. The NVM device of claim 6, wherein the first NVM chip inactivates the write ODT enable signal during a postamble section of the data strobe signal after the toggling section when the ODT signal is inactivated.

8. The NVM device of claim 1, wherein the first NVM chip activates a read ODT enable signal during a preamble section of the control signal before a toggling section of the control signal when the ODT signal is activated and the control signal is activated, and uses the ODT circuit to perform the ODT on the control pin when the read ODT enable signal is activated.

9. The NVM device of claim 8, wherein the first NVM chip inactivates the read ODT enable signal during a postamble section of the control signal after the toggling section when the ODT signal is inactivated.

10. The NVM device of claim 1, wherein the ODT circuit comprises;

a first resistor connected in series between a power supply voltage and a first switch connected to the data pin; and

a second resistor connected in series between the power supply voltage and a second switch connected to the control pin,

wherein the first NVM chip turns on the first switch and turns off the second switch during the ODT write mode, and

wherein the first NVM chip turns off the first switch and turns on the second switch during the ODT read mode.

11. The NVM device of claim 1, wherein the first NVM chip comprises:

a first input circuit outputting a first internal signal based on the control signal;

a second input circuit outputting a second internal signal based on the ODT signal; and

a control circuit generating a write ODT enable signal and a read ODT enable signal based on the first and second internal signals,

wherein the write ODT enable signal is used to perform the ODT during the ODT write mode and the read ODT enable signal is used to perform the ODT during the ODT read mode.

12. The NVM device of claim 11, wherein the control circuit comprises:

an inverter receiving the first internal signal;

a delay circuit receiving the second internal signal;

a first flip-flop comprising a data pin receiving an output of the inverter, a clock terminal receiving an output of the delay circuit, and an output terminal outputting the ODT read enable signal; and

a second flip-flop comprising a data pin receiving the first internal signal, a clock terminal receiving an output of the delay circuit, and an output terminal outputting the ODT write enable signal.

13. The NVM device of claim 11, wherein the first input circuit comprises a buffer configured to output the first internal signal, wherein the control circuit activates the buffer when the ODT signal is activated, and inactivates the buffer after pre-defined delay.

14. The NVM device of claim 1, wherein the NVM device modifies an impedance of the ODT circuit based on an impedance signal received through the data pin.

15. The NVM device of claim 1, wherein the NVM device configures a pin to operate as the ODT pin in response to a received ODT setting command.

16. A nonvolatile memory (NVM) device comprising:

a data pin;

a control pin;

a first on-die termination (ODT) pin;

a second ODT pin; and

a plurality of NVM chips commonly connected to the data pin, the control pin, the first ODT pin and the second ODT pin,

wherein a first NVM chip among the NVM chips comprises an ODT circuit,

wherein the first NVM chip determines one of an ODT write mode and an ODT read mode based on a first ODT signal received through the first ODT pin and a second ODT signal received through the second ODT pin, uses the ODT circuit to perform an ODT on the data pin during the ODT write mode, and uses the ODT circuit to perform the ODT on the control pin during the ODT read mode,

wherein one of a write operation and a read operation is enabled based on a control signal applied to the control pin, and

wherein the plurality of NVM chips commonly receives the first ODT signal and the second ODT signal.

17. The NVM device of claim 16, wherein the NVM device further comprises a data strobe pin for receiving a data strobe signal, and the NVM chips are commonly connected to the data strobe pin.

18. The NVM device of claim 17, wherein the first NVM chip activates a write ODT enable signal during a preamble section of the data strobe signal before a toggling section of the data strobe signal when the first ODT signal is activated, and uses the ODT circuit to perform the ODT on the data pin and the data strobe pin when the write ODT enable signal is activated.

19. The NVM device of claim 16, wherein the first NVM chip activates a read ODT enable signal during a preamble section of the control signal before a toggling section of the control signal when the second ODT signal is activated, and uses the ODT circuit to perform the ODT on the control pin when the read ODT enable signal is activated.

20. A nonvolatile memory (NVM) device comprising:

a data pin;

a first control pin;

a second control pin; and

a plurality of NVM chips commonly connected to the data pin and the first control pin,

wherein a first NVM chip among the NVM chips comprises an ODT circuit,

wherein the first NVM chip determines one of an ODT write mode and an ODT read mode based on a first control signal received through the first control pin and a second control signal received through the second control pin, uses the ODT circuit to perform an ODT on the data pin during the ODT write mode, uses the ODT circuit to perform the ODT on the first control pin during the ODT read mode when the first control signal is a read enable signal, and uses the ODT circuit to perform the ODT on a read enable pin of the NVM device during the ODT read mode when the first and second control signals indicate whether the ODT is to be performed on the data pin or the read enable pin,

wherein one of a write operation and a read operation is enabled based on a read enable signal applied to the read enable pin.