CLAIMS

1. A metallized substrate comprising:

a base substrate having one or more vias terminating in the base substrate, extending between a first face and second face of the base substrate, or any combination thereof, the base substrate comprising a glass substrate or a silicon substrate; and

a via fill material within the one or more vias, the via fill material comprising:

1) a porous matrix material having a void space of about 30% to about 60% and comprising a plurality of electrically conductive particles; and

2) a conductive network at least partially filling the void space within the porous matrix material, the conductive network comprising a plurality of metal nanoparticles that have been consolidated together with one another.

2. The metallized substrate of claim 1, wherein the electrically conductive particles are bonded together with a cured silicate-reactive matrix material, wherein the silicate-reactive matrix material cures at a temperature within a range of room temperature to about 100°C, optionally, wherein the cured silicate-reactive matrix material comprises a cured liquid glass binder.

3. The metallized substrate of claim 2, wherein a mass ratio of the electrically conductive particles to the cured silicate-reactive matrix material in the via fill material ranges from about 6:1 to about 30:1.

4. The metallized substrate of claim 2 or claim 3, wherein the cured silicate-reactive matrix material is also chemically bonded to a wall surface of the one or more vias.

5. The metallized substrate of any of claims 1-4, wherein the electrically conductive particles comprise one or more particles selected from the group consisting of micron-size metal particles, chopped metal filaments, metal nanowires, carbon nanotubes, graphene, a graphite material, and any combination thereof.

6. The metallized substrate of any of claims 1-5, wherein the electrically conductive particles have a diameter no larger than about 1/10th a

diameter of the one or more vias, the electrically conductive particles are elongated and have a length no larger than about 3/4th of the diameter of the one or more vias, or any combination thereof.

7. The metallized substrate of any of claims 1-6, wherein the electrically conductive particles comprise at least micron-size copper particles.
8. The metallized substrate of claim 7, wherein the metal nanoparticles comprise copper nanoparticles.
9. The metallized substrate of any of claims 1-8, wherein the one or more vias have a diameter up to about 500 microns.
10. The metallized substrate of any of claims 1-9, further comprising:

one or more conductive traces defined upon at least one of the first face or the second face of the base substrate and in electrical communication with the via fill material.

11. The metallized substrate of claim 10, wherein the one or more conductive traces are located upon a seed layer adhered to at least one of the first face or the second face of the base substrate, the seed layer being electrically conductive and comprising a cured silicate-reactive matrix material and a second plurality of electrically conductive particles mixed with the cured silicate-reactive matrix material, and wherein the one or more conductive traces directly contact the via fill material or indirectly contact the via fill material by way of a bonding pad.
12. The metallized substrate of claim 10, wherein the seed layer has a thickness ranging from about 1 micron to about 30 microns.
13. The metallized substrate of claim 10, wherein the second plurality of electrically conductive particles in the seed layer comprises micron-size metal particles, metal nanoparticles, or any combination thereof.
14. A printed circuit board comprising the metallized substrate of any of claims 1-13 or a plurality of the metallized substrates of any of claims 1-13 that are stacked upon one another.
15. The printed circuit board of claim 14, wherein the electrically conductive particles are bonded together with a cured silicate-reactive matrix material, wherein the silicate-reactive matrix material cures at a temperature within a range of room temperature to about 100°C.
16. The printed circuit board of claim 14 or claim 15, wherein one or more conductive traces are defined upon at least one of the first face or the second face of the base substrate and in electrical communication with

the via fill material.

17. The printed circuit board of claim 16, wherein the one or more conductive traces are located upon a seed layer adhered to at least one of the first face or the second face of the base substrate, the seed layer being electrically conductive and comprising a cured silicate-reactive matrix material and a second plurality of electrically conductive particles mixed with the cured silicate-reactive matrix material.

18. An interposer comprising the metallized substrate of any of claims 1-13.

19. A process comprising:

providing a base substrate having one or more vias defined therein, the one or more vias terminating in the base substrate, extending between a first face and a second face of the base substrate, or any combination thereof, and the base substrate comprising a glass substrate or a silicon substrate;

depositing a via fill precursor comprising a plurality of electrically conductive particles within the one or more vias;

curing the via fill precursor to form a porous matrix material having a void space of about 30% to about 60%;

introducing a metal nanoparticle composition into at least a portion of the void space; and

at least partially consolidating metal nanoparticles of the metal nanoparticle composition with one another in the void space to form a conductive network at least partially filling the void space.

20. The method of claim 19, wherein the via fill precursor further comprises a silicate-reactive matrix material, the silicate-reactive matrix material forming a cured silicate-reactive matrix material after curing at a temperature within a range of about room temperature to about 100°C and bonding the electrically conductive particles together, optionally, wherein the silicate-reactive matrix material comprises a liquid glass binder.

21. The process of claim 19 or claim 20, wherein the electrically conductive particles comprise one or more particles selected from the group consisting of micron-size metal particles, chopped metal filaments, metal nanowires, carbon nanotubes, graphene, and any combination thereof.

22. The process of any of claims 19-21, wherein the metal nanoparticle

composition is introduced into the one or more vias in at least a portion of the void space by pressure infiltration, vacuum infiltration, or any combination thereof.

23. The process of any of claims 19-22, wherein the electrically conductive particles have a diameter no larger than about $1/10^{th}$ a diameter of the one or more vias, the electrically conductive particles are elongated and have a length no larger than about $3/4^{th}$ of the diameter of the one or more vias, or any combination thereof.

24. The process of any of claims 19-23, wherein the electrically conductive particles comprise at least micron-size copper particles.

25. The process of claim 24, wherein the metal nanoparticles comprise copper nanoparticles.

26. The process of any of claims 19-25, wherein the one or more vias have a diameter up to about 500 microns.

27. The process of any of claims 19-26, further comprising:

depositing a seed layer upon at least a portion of the base substrate, the seed layer comprising a silicate-reactive matrix material and a second plurality of electrically conductive particles;

curing the silicate-reactive matrix material to form a cured silicate-reactive matrix material;

optionally, mechanically polishing the seed layer; and

forming one or more conductive traces upon at least a portion of the seed layer, the one or more conductive traces being in electrical communication with the via fill material.

28. The process of any of claims 19-27, wherein the via fill precursor and the metal nanoparticle composition are combined together prior to being deposited and introduced into the one or more vias, or alternatively, wherein the via fill precursor and the metal nanoparticle composition are deposited and introduced separately into the one or more vias.