

Claims

What is claimed is:

- 5 1. A method of making a multi-die patch, the method comprising:
forming a first patterned conductive layer defining multiple contact pads
on a first carrier structure;
placing a first die on a first plurality of contact pads of the multiple
contact pads;
10 placing a second die on a second plurality of contact pads of the multiple
contact pads;
embedding the first die and the second die in a dielectric disposed on the
patterned conductive layer;
attaching a second carrier structure to the dielectric on a surface of the
15 dielectric opposite the first carrier;
removing the first carrier structure;
forming routing traces, the routing traces configured to electrically
couple the first and second die with one or more surface die;
forming first terminals connected with a first plurality of routing traces of
20 the routing traces, the first terminals exposed at a first side of the
dielectric; and
forming second terminals connected with a second plurality of routing
traces of the routing traces, the second terminals exposed at a
second side of the dielectric, the second side opposite the first
25 side.
2. The method of claim 1, wherein a thickness of the first die is different
than the thickness of the second die.
- 30 3. The method of claim 1, wherein the forming second terminals includes
removing the second carrier structure.

4. The method of claim 3, wherein removing the second carrier structure includes laser ablating an adhesive layer of the second carrier structure.
5. The method of claim 3, wherein removing the second carrier structure includes coupling a stiffener to the first side before removing the second carrier structure.
6. The method of claim 1, wherein the forming a patterned conductive layer includes:
10 depositing a copper layer on a first carrier; and
etching the multiple contact pads in the first copper layer.
7. The method of claim 6, including:
laminating a first portion of the dielectric to the patterned conductive
15 layer; and
polishing the first portion of the dielectric.
8. The method of claim 1, including forming a plurality of vertical contacts extending from a third plurality of contact pads of the multiple contact pads to
20 the second side.
9. The method of claim 8, wherein the embedding the first die and the second die in a dielectric includes embedding the vertical contacts in the dielectric.
25
10. The method of claim 9, wherein the embedding the first die and the second die in a dielectric includes planarizing the dielectric to expose the vertical contacts.
- 30 11. The method of claim 10, wherein the embedding the first die and the second die in a dielectric includes sputtering a protective layer over exposed portions of the vertical contacts.

12. The method of claim 1, wherein the first carrier structure includes a glass carrier.

13. The method of claim 1, wherein the second carrier structure includes a
5 glass carrier.

14. The method of claim 1, wherein the forming first terminals includes replacing at least a portion of the first patterned conductive layer with a second patterned conductive layer.

10

15. The method of claim 14, wherein the forming first terminals includes:
attaching a solder resist material to the second patterned conductive
layer;

etching vias in the solder resist layer; and

15 filling the vias with conductive material to form the first terminals.

16. The method of claim 1, wherein the forming first terminals includes etching at least a portion of the first patterned conductive layer after the first carrier structure is removed.

20

17. The method of claim 16, wherein the forming first terminals includes etching an attachment material from contacts of at least one of the first embedded die or the second embedded die.

25 18. The method of claim 1, wherein at least a portion of the first terminals to the first and second embedded dies are arranged in a first pitch relative to one another, and wherein at least a portion of the second terminals are arranged at a second pitch relative to one another, and wherein the first pitch is narrower than the second pitch.

30

19. A patch configured to electrically interconnect a first surface die with a second surface die and to interconnect at least one of the first surface die or the second surface die with an interposer or other device, the patch comprising:

a dielectric;
first terminals exposed on a first side of the dielectric;
second terminals disposed in the dielectric and exposed on a second side
of the dielectric, the second terminals configured to couple with
5 the interposer, the second side opposite the first side;
a first embedded die embedded in the dielectric and coupled to a first
plurality of the first terminals; and
a second embedded die embedded in the dielectric and coupled to a
second plurality of the first terminals; and
10 wherein a thickness of the first embedded die is different than a thickness
of the second embedded die.

20. The patch of claim 19, including traverse routing traces configured to
electrically couple at least one of the first terminals with a terminal of at least
15 one of the first embedded die or the second embedded die.

21. The patch of claim 19, wherein the first embedded die is a bridge die.

22. The patch of claim 19, wherein the first embedded die is an active die.
20

23. The patch of claim 19, wherein the second embedded die is a bridge die.

24. The patch of claim 19, wherein the second embedded die is an active die.

25 25. The patch of any of claims 19-24, wherein at least one of the first
embedded die or the second embedded die includes one or more through
silicon vias.

30