ABSTRACT

METHOD OF SHALLOW TRENCH ISOLATION

The invention is an improved process for forming isolations of uniform thickness in narrow and wide trenches. The process begins by forming a pad layer on a semiconductor substrate. A first barrier layer is formed on the pad layer. The first barrier layer and pad layer are patterned forming openings, thereby exposing the substrate surface. The substrate is then etched through the openings to form shallow trenches in the substrate. The trenches generally falling into two ranges of width: narrow trenches having widths in the range between 0.3 μm and 1.0 μm; and wide trenches having widths greater than 1.0 μm. A thin oxide film is grown on the sidewalls and bottoms of the trenches. A gap-fill dielectric layer is formed on the thin oxide film. A polysilicon layer is grown on the gap-fill dielectric layer. The polysilicon layer acts as a stop during CMP, providing additional protection of the gap-fill dielectric layer in the wide trenches. A planarizing material layer is formed on the polysilicon layer. The planarizing material layer, polysilicon layer and gap-fill dielectric layer are planarized to the level of the first barrier layer using chemical mechanical polishing (CMP). The residual planarizing material is then stripped. The polysilicon layer is oxidized forming **a novel second dielectric oxide layer** in an oxidizing atmosphere. The dielectric layer is densified, preferably in the same oxidizing atmosphere, forming an isolation layer with uniform thickness in the narrow trenches and the wide trenches. The stress developed during conversion of the polysilicon layer to a novel second dielectric oxide layer compensates for the stress due to densification of the dielectric layer.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)