DIELECTRIC DEPOSITION AND ETCH BACK PROCESSES FOR BOTTOM UP GAPFILL

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/805,573, filed June 22, 2006, the entire contents of which are herein incorporated by reference for all purposes. This application is also related to U.S. Pat. App. Ser. No. 11/753,918, filed May 25, 2007, and titled "A METHOD FOR DEPOSITING AND CURING LOW-K FILMS FOR GAPFILL AND CONFORMAL FILM APPLICATIONS"; and U.S. Pat. App. Ser. No. 11/753,968, filed May 25, 2007, and titled "A NOVEL DEPOSITION-PLASMA CURE CYCLE PROCESS TO ENHANCE FILM QUALITY OF SILICON DIOXIDE", of which the entire contents of both applications are herein incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

[0002] One of the persistent challenges faced in the development of semiconductor technology is the desire to increase the density of circuit elements and interconnections on substrates without introducing spurious interactions between them. Unwanted interactions are typically prevented by providing gaps or trenches that are filled with electrically insulative material to isolate the elements both physically and electrically. As circuit densities increase, however, the widths of these gaps decrease, increase their aspect ratios and making it progressively more difficult to fill the gaps without leaving voids. The formation of voids when the gap is not filled completely is undesirable because they may adversely affect operation of the completed device, such as by trapping impurities within the insulative material.

[0003] Common techniques that are used in such gapfill applications are chemical-vapor deposition ("CVD") techniques. Conventional thermal CVD processes supply reactive gases to the substrate surface where heat-induced chemical reactions take place to produce a desired film. Plasma-enhanced CVD ("PECVD") techniques promote excitation and/or dissociation of the reactant gases by the application of radio-frequency ("RF") energy to a

reaction zone near the substrate surface, thereby creating a plasma. The high reactivity of the species in the plasma reduces the energy required for a chemical reaction to take place, and thus lowers the temperature required for such CVD processes when compared with conventional thermal CVD processes. These advantages may be further exploited by high-density-plasma ("HDP") CVD techniques, in which a dense plasma is formed at low vacuum pressures so that the plasma species are even more reactive. While each of these techniques falls broadly under the umbrella of "CVD techniques," each of them has characteristic properties that make them more or less suitable for certain specific applications.

[0004] In some instances where gaps have a large aspect ratio and narrow width, gaps have been filled with thermal CVD techniques using a "dep/etch/dep" process by sequentially depositing material, etching some of it back, and depositing additional material. The etching step acts to reshape the partially filled gap, opening it so that more material can be deposited before it closes up and leaves an interior gap. Such dep/etch/dep processes have also been used with PECVD techniques, but some thermal and PECVD techniques are still unable to fill gaps having very large aspect ratios even by cycling deposition and etching steps.

[0005] Dep/etch/dep processes have also been shown to improve gapfill in HDP-CVD processes. Originally, the application of dep/etch/dep processes to HDP-CVD was considered counterintuitive because, unlike PECVD processes, the high density of ionic species in the plasma during HDP-CVD processes already causes there to be sputtering of a film while it is being deposited. This simultaneous sputtering and deposition of material during a deposition process tends to keep the gap open during deposition, and was therefore believed to render a separate intermediate etching step superfluous. Nevertheless, in U.S. Pat. No. 6,194,038, filed March 20, 1998 by Kent Rossman, the unexpected result was demonstrated that gapfill could be improved even further by using a dep/etch/dep process under certain HDP-CVD process conditions. This result was later confirmed in U.S. Pat. No. 6,030,181, filed May 5, 1998 by George D. Papasouliotis *et al.*

[0006] However, even for processes that combine HDP-CVD and dep/etch/dep for dielectric gapfills, there are still limits on the size and aspect ratios of the gaps that can be filled. For example, small gaps with high aspect ratios may need to undergo an impractical number dep-etch cycles to keep the top portion of the gap from overfilling with dielectric material. The increased frequency and duration of the etch cycles presents a possibility of damaging the structures that define the gaps to be filled. This possibility exists when

insufficient material is deposited during the prior deposition and/or when too much of the deposited material is removed during the etching step. Optimization of a recipe is hindered by the fact that individual chamber characteristics and/or individual wafer characteristics may affect the deposition and etching. As the trend towards more densely packed devices continues, it will be desirable to find new methods of depositing dielectric materials into the gaps that can accommodate their increasing aspect ratios.

BRIEF SUMMARY OF THE INVENTION

[0007] Embodiments of the invention include methods to reduce film cracking in a dielectric layer. The methods may include the steps of depositing a first dielectric film on a substrate and removing a top portion of the first dielectric film by performing an etch on the film. The methods may also include depositing a second dielectric film over the etched first film, and removing a top portion of the second dielectric film. In addition, the methods may include annealing the first and second dielectric films to form the dielectric layer, where the removal of the top portions from the first and the second dielectric films reduces a stress level in the dielectric layer.

[0008] Embodiments also include methods filling a trench with a dielectric material. The methods may include filling the trench with a film of the dielectric material, where the dielectric film may be formed by combining a first fluid stream comprising atomic oxygen with a second fluid stream comprising a silicon-containing precursor, and reacting the atomic oxygen and the silicon-containing precursor to form the dielectric film in the trench. The methods may also include removing a top portion of the dielectric film by etching the film, and annealing the etched film.

[0009] Embodiments still further include additional methods to reduce film cracking in a dielectric layer. The methods may include depositing a first dielectric film on a substrate and performing a first anneal on the first film. The methods may also include removing a top portion of the annealed first film by performing a first etch on the first film, and depositing a second dielectric film over the etched first film. In addition, the methods may include removing a top portion of the second dielectric film by performing a second etch on the second film, and performing a second anneal of the first and second dielectric films and forming the dielectric layer. The removal of the top portions from the first and the second dielectric films reduces a stress level in the dielectric layer.

[0010] Embodiments may yet still further include multistep deposition methods for filling a gap on a semiconductor substrate with dielectric material. The methods may include depositing a first dielectric film in a bottom portion of the gap, and annealing the first dielectric film in a first anneal. The methods may further include depositing a second dielectric film on the annealed first dielectric film, and annealing the second dielectric film in a second anneal.

[0011] Additional embodiments and features are set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the specification or may be learned by the practice of the invention. The features and advantages of the invention may be realized and attained by means of the instrumentalities, combinations, and methods described in the specification.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figs. 1A-C show cross-sectional views of a gap pattern in a substrate that is filled with dielectric material according to embodiments of the invention;

[0013] Figs. 2A&B are flowcharts showing methods of depositing dielectric material on a substrate according to embodiments of the invention;

[0014] Fig. 3 is a flowchart illustrating methods of depositing dielectric material that includes using an atomic oxygen precursor to deposit the material according to embodiments of the invention;

[0015] Fig. 4 is a flowchart that shows methods of depositing and heating dielectric material according to embodiments of the invention;

[0016] Figs. 5A&B are additional flowcharts showing methods of depositing and annealing dielectric material according to embodiments of the invention;

[0017] Figs. 6A-D show cross-sectional views of substrate gaps that are filled with dielectric material according to embodiments of the invention;

[0018] Figs. 7A-C show additional cross-sectional views of substrate gaps that are filled with dielectric material according to embodiments of the invention;

[0019] Figs. 8A&B show electron micrographs of dielectric materials deposited in substrate gaps and along a substrate step according to embodiments of the invention; and

[0020] Figs. 9A&B show electron micrographs of comparative dielectric depositions in substrate gaps and along a substrate step.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Embodiments of the invention include methods and systems for depositing dielectric materials in gaps and trenches within a surface of a substrate. The dielectric materials include silicon oxide films, which have wide application in the art, but the invention is not limited to any particular film composition, as will be evident from the description. Dielectric films deposited according to the techniques of the invention have excellent gapfill properties and can fill high-aspect-ratio gaps encountered in, for example, shallow trench isolation (STI) structures. Dielectric materials deposited by the methods and systems of the invention are particularly useful in filling gaps in 100-nm or smaller technology (e.g., 65 nm, 45 nm technology, etc.).

[0022] Dielectric depositions may include the formation of flowable dielectrics on the substrate that tend to collect in the bottom portion of a substrate gap or trench during the deposition. Because the flowable dielectric tends to migrate from the top to bottom portions of a gap, the congestion of dielectric material around the top of the gap is reduced, which reduces the occurrence of voids around the center of the gapfill.

[0023] Following a partial or complete fill of the gap, the flowable dielectric may be treated (*e.g.*, cured, baked, annealed, etched, *etc.*) to harden the dielectric. These treatments often reduce the amount of hydroxyl groups and water vapor in the flowable dielectric, and physically reduce the dimensions of the deposited film, thereby increasing its density. However, when the film shrinks, it is common for cracks (*e.g.*, microcracks) to form that can adversely impact the dielectric qualities, barrier qualities, support qualities, *etc.*, of the deposited dielectric. The size and number of these cracks typically increase with an increased thickness of the deposited dielectric film.

[0024] Figs. 1A-C show cross-sections of a gap pattern formed in a substrate 102 as a flowable dielectric is being deposited and treated in the substrate gaps 104a-d. Fig. 1A shows a substrate 102 with a pattern of gaps 104a-d that includes narrow gaps 104a-c and a wide gap 104d. The gaps 104a-c may have an aspect ratio of about 3:1 or more, about 5:1 or more, about 8:1 or more, about 10:1 or more, about 12:1 or more, *etc.* The substrate may be made of a semiconductor material (*e.g.*, Si, doped Si, GaAs, *etc.*) on which circuit elements (e.g.,

transistors, contacts, *etc.*) are formed into an integrated circuit. The substrate may be a semiconductor substrate wafer (*e.g.*, a 100mm, 150mm, 200mm, 300mm, 400mm, *etc.*, wafer). The substrate 102 may also include one or more additional layers, such as a dielectric layer (*e.g.*, a contact layer, a PMD layer, a IMD layer, *etc.*) in which the gaps 104a-d have been formed.

[0025] Fig. 1B shows the substrate 102 following a deposition of a flowable dielectric material 106. The flowable dielectric may be a silicon oxide type dielectric formed from the reaction of oxygen-containing and silicon-containing precursors. For example, the oxide dielectric may be formed from the reaction of remotely generated radical atomic oxygen (*i.e.*, the oxygen-containing precursor) and an organo-silicon precursor such as tetramethylorthosilicate (i.e., the silicon-containing precursor). Additional details and examples of methods of depositing flowable dielectric compositions may be found in co-assigned U.S. Pat. App. Ser. No. 11/549,930, filed October 16, 2006, and titled "FORMATION OF HIGH QUALITY DIELECTRIC FILMS OF SILICON DIOXIDE FOR STI: USAGE OF DIFFERENT SILOXANE-BASED PRECURSORS FOR HARP II - REMOTE PLASMA ENHANCED DEPOSITION PROCESSES"; and U.S. Pat. App. Ser. No. 11/754,440, filed May 29, 2007, and titled "CHEMICAL VAPOR DEPOSITION OF HIGH QUALITY FLOW-LIKE SILICON DIOXIDE USING A SILICON CONTAINING PRECURSOR AND ATOMIC OXYGEN" of which the entire contents of both applications are herein incorporated by reference for all purposes.

[0026] In the example shown, the flowable dielectric 106 partially fills the gaps 104a-d. The flowability of the dielectric may cause a migration from the top to the bottom portions of the gaps 104a-d, which increases the thickness of the film at the bottom portion of the gaps. The rate of the dielectric film migration depends on the film's viscosity as well as process parameters, such as the deposition temperature.

[0027] Fig. 1C shows size changes in the dielectric thickness of one of the partially filled gaps 104c during a post-deposition treatment of the dielectric material. As indicated by the arrows, the treatment reduces the thickness of the deposited dielectric material 106 along the bottom and sidewalls of the gap 104c, as well as the material 106 over the top of the gap. The net effect of this shrinkage is to widen the cavity formed in the gap 104c by the sidewalls and bottom portions of the treated dielectric material. As note above, the change in physical dimensions of the treated dielectric can also cause the film to crack.

[0028] The film cracking may be reduced or eliminated by etching the film before or during a treatment step that reduces the size and increases the density of the film. For example, and etch may be preformed on the newly deposited film that removes a top portion of the film. This etch may reduce the stresses on the film that can lead to cracking during a subsequent densification step. Following the etch, additional dielectric material may be deposited before or after the treatment of the etched dielectric film. Another etch may be performed on the additional dielectric material.

[0029] Figs. 2A&B are flowcharts showing an exemplary method 200 of depositing and etching dielectric material from a substrate according to embodiments of the invention. The method 200 shown in Fig. 2A includes depositing a first film 202 on the substrate. The film may be a flowable dielectric film deposited on a substrate having one or more gaps and/or trenches that are formed in the substrate.

[0030] For example, the deposited first film may include a silicon oxide dielectric formed from an organo-silicon precursor and oxygen-containing precursor. The organo-silicon precursor may include one or more of dimethylsilane, trimethylsilane, tetramethylsilane, diethylsilane, trimethoxysilane (TriMOS), tetramethylorthosilicate (TMOS), triethoxysilane (TriEOS), tetraethylorthosilicate (TEOS), octamethyltrisiloxane (OMTS), octamethylcyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TOMCATS), DMDMOS, DEMS, methyl triethoxysilane (MTES), phenyldimethylsilane, and/or phenylsilane. The oxygen-containing precursor may be atomic oxygen that is generated remotely from oxygen containing species such as molecular oxygen (O_2), ozone (O3), nitrogen dioxide (NO_2), nitrous oxide (N_2O), peroxide (e.g., H_2O_2) and water vapor (H_2O), among other oxygen containing species. Additional gases may also be present with the precursors, such as carrier gases (*e.g.*, hydrogen, helium, nitrogen (N2), argon, etc.) that help transport the precursors to a deposition chamber, and water vapor, peroxide and/or other hydroxyl-containing species introduced into the deposition chamber.

[0031] In some examples of method 200, the deposited first film may completely fill the gaps, and may even continue to a final thickness above the gaps. In additional examples, the first film may partially fill the gaps (*e.g.*, fill the bottom 10%, 20%, 30%, 40%, 50%, 60%, 70, 80%, or 90%, *etc.*, of the gap).

[0032] Following the deposition 202, a top portion of the first dielectric film may be removed 204. The removal may be done by etching the freshly deposited film. For example,

the film may be chemically dry etched with an activated etchant such as atomic fluorine. The activated fluorine may be generated from one or more fluorine containing precursors (such as NF3 and/or an organo-fluorine compound) that is dissociated in a plasma. Etchants may also include oxygen, ozone, and/or hydrogen gas. In additional examples, the film may be plasma etched by exposure to a plasma of helium, argon, nitrogen, *etc.* generated by, for example, a remote plasma system or microwave applicator located outside the reaction chamber, and/or and ICP or CCP generator that generates the plasma inside the reaction chamber.

[0033] In some examples, the removed top portion of the film may constitute about 10%, 20%, 30%, 40%, 50%, 60%, etc., of the thickness of the film. When the first film is initially deposited at or above the tops of the gaps/trenches, the removal step 204 may remove enough material to bring dielectric level below the tops of the gaps/trenches. In additional instances, the removal step 204 may remove some of the dielectric above the tops, but not enough to bring the dielectric below the tops of the gaps/trenches. When the first film is initially deposited below the tops of the gaps/trenches, the removal step 204 may further reduce the amount of the first film in the trenches.

[0034] During or following the removal 204, the first film may, in some embodiments, be treated to harden and increase the density of the film. The treatments may include baking (*i.e.*, thermal annealing), irradiative annealing, plasma curing, E-beam curing, and/or UV curing the film, among other treatments. For example, the film may be baked (i.e., thermally annealed) at a temperature of up to about 600°C (e.g., about 300°C to about 400°C) for a period of time of up to about an hour (*e.g.*, about 1 minute to about 1 hour). In irradiative annealing, the film may be exposed to thermal radiation (*e.g.*, infrared radiation) from, for example, heat lamps that raise the temperature of the film. An example of irradiative annealing is rapid thermal annealling (RTA). Plasma curing and E-beam curing may be done by exposing the film to a plasma and electron-beam, respectively. The plasma may be a induced-coupled plasma (ICP) or capacitively-coupled plasma (CCP) that is generated inside the chamber containing the substrate. UV curing may be done by exposing the film to radiation having a significant UV frequency component. The radiation may be generated by, for example, an incandescent light source and/or a laser.

[0035] After the removal of a top portion of the first dielectric film 204, and in some embodiments a treatment of the first dielectric film, a second dielectric film may be deposited 206 on a remaining portion of the first film. The second dielectric film may be deposited

with using the same precursors and deposition conditions as the first dielectric film. For example, the first and second dielectric films may be silicon oxide films deposited using the same organo-silicon and oxygen-containing precursors. In additional embodiments, the second film may use different precursors or process conditions than the first film, and may be a different kind of dielectric than the first film (*e.g.*, a silicon nitride or silicon oxy-nitride dielectric instead of a silicon oxide dielectric).

[0036] The second dielectric film may also be a flowable dielectric. When the remaining portion of the first film is below the tops of the gaps/trenches, the second film may fill the rest of the gaps/trenches, and may continue to fill a space above the tops. In additional examples where the first film is below the tops, the second film may fill a volume that is less than the total remaining volume in the gaps/trenches. In these examples, one or more additional dielectric depositions may be done to completely fill the gaps/trenches.

[0037] Similar to the first dielectric film, a top portion of the second dielectric film may be removed 208 following the initial deposition. The removal step 208 may remove the same portion of the film as the first portion, or it may remove a greater or lesser percentage of the film than the first removal step 204. In some instances, the second removal step 208 may be stopped before the second dielectric film dips below the top of the gaps/trenches, while in other instances removal step 208 leaves the remaining second dielectric film below the tops of the gaps/trenches.

[0038] The remaining portions of the first and second dielectric films may be annealed 210. The anneal 210 may be a thermal anneal (*i.e.*, baking), a plasma anneal, a ultraviolet light anneal, an IR irradiative anneal (*e.g.*, RTA), an e-beam anneal, and/or a microwave anneal, among other types of anneals. For example, the anneal 210 may be a thermal anneal that includes adjusting the temperature of the substrate to about 300°C to about 1000°C (e.g., about 650°C to about 950°C) for a period of about 1 minute to about 1 hour. The anneal atmosphere may be, for example, and inert gas atmosphere (*e.g.*, N_2, He, Ne, Ar, H_2, *etc.*), and/or an oxygen containing atmosphere NO_2, N_2O, H_2O, H_2O_2, O_2, O_3, *etc.*, among other types of atmospheres. The pressure of the anneal atmosphere may be from about 0.1 Torr to about 100 Torr (*e.g.*, about 1 to 2 Torr). The anneal 210 normally increases the density and reduces the etch rate (*e.g.*, reduces the WERR) of the annealed dielectric material.

[0039] Fig. 2B shows a method 250 of depositing and etching one or more layers of dielectric material in a substrate gap or trench according to embodiments of the invention.

The method 250 may include depositing a dielectric layer into the substrate gap/trench 252 and removing a top portion of the deposited dielectric layer 254. A determination is then made whether the deposited and etched dielectric material fills the trench 256 (i.e., whether the dielectric film is at or above the top of the gap). If the dielectric material has not entirely filled the gap, then an additional dielectric layer is deposited and etched in the gap, and another determination is made about whether the gap is completely filled.

[0040] When the gap has been completely filled with dielectric after one, two, three, etc. deposition 252 and removal 254 cycles, the layer (or layers) of dielectric may be annealed 258. As noted above, the anneal 258 may be a thermal anneal (*i.e.*, baking), a plasma anneal, a ultraviolet light anneal, an IR irradiative anneal (*e.g.*, RTA), an e-beam anneal, and/or a microwave anneal, among other types of anneals.

[0041] Referring now to Fig. 3, flowchart illustrating an exemplary method 300 of depositing dielectric material that includes using an atomic oxygen precursor to deposit the material according to embodiments of the invention is shown. The method 300 may include combing an atomic oxygen precursor with a silicon precursor 302 and reacting the precursors 304 to deposit a dielectric film in the gap or trench on a semiconductor substrate. The atomic oxygen may be generated in-situ in the deposition chamber, or remotely generated and transported to the chamber. For example, a remote plasma generation system may be used to dissociate an oxygen-containing precursor (*e.g.*, O2, O3, N2O, NO2, *etc.*) and form the atomic oxygen species, which is then transported to the deposition chamber to mix and react with other precursors (*e.g.*, silicon-containing precursors) and deposit the dielectric material 306.

[0042] Following the deposition 306, a top portion of the dielectric film may be removed in a etch process 308. For example, when the dielectric is primarily silicon dioxide (SiO_x), a top portion of the oxide may be removed by exposing the deposited film to activated fluorine (*e.g.*, about 1 second to about 1 minute of exposure) generated by the dissociation (e.g., plasma dissociation) of a fluorine precursor such as NF_3 that is transported to the substrate (*e.g.*, NF_3 flows into the substrate at about 1500 sccm with a total chamber pressure of about 1 to 2 Torr). The activated fluorine reacts with the silicon oxide to form silicon fluoride compounds (*e.g.*, SiF_4) that are volatile and get removed from the deposited dielectric.

[0043] The remaining portion of the dielectric after removal step 308 may be annealed 310 to increase the density and reduce the etch rate of the film. The anneal 310 may be a thermal

anneal (*i.e.*, baking), a plasma anneal, a ultraviolet light anneal, an IR irradiative anneal (*e.g.*, RTA), an e-beam anneal, and/or a microwave anneal, among other types of anneals.

[0044] Fig. 4 shows a flowchart illustrating a method 400 of depositing and heating dielectric material according to embodiments of the invention. The method 400 includes a multistep heating process where a first deposited dielectric film is heated in three stages at three different temperatures before a top portion of the film is removed. The method 400 may start with depositing the dielectric film 402 on a substrate that may have one or more gaps and/or trenches. The film my partially or completely fill these gaps.

[0045] Following the deposition 402, the film may be heated to a first temperature 404 (*e.g.*, up to about 50°C) for a first period of time (*e.g.*, about 1 hour). Then the film may be adjusted to a second temperature 406 (e.g., about 50°C to about 100°C) for a second period of time (e.g., about 30 minutes). The film may then further be adjusted to a third temperature 408 (*e.g.*, about 100°C to about 600°C) for a third period of time (*e.g.*, about 30 minutes to about 1 hour). Additional heating steps (not shown) may also occur.

[0046] A top portion of the first dielectric may removed 410 after the multistep heating. This removal may be done by a chemical wet etch or dry etch process. Then, a second dielectric film may be deposited 412 on the remaining portion of the first film and another top portion of the second film may be removed 414.

[0047] The remaining portions of the first and second dielectric films may then be annealed 416 to increase the density of the films. The anneal 416 may be done in a dry, non-reactive atmosphere (*e.g.*, N_2, He, *etc.*) at a temperature of about 800°C or more (*e.g.*, about 850°C, about 900°C, about 950°C, about 1000°C, *etc.*).

[0048] Referring now to Figs. 5A & 5B additional flowcharts showing methods 500 and 550 of depositing and annealing dielectric material according to embodiments of the invention are shown. Fig. 5A shows a method 500 that includes alternating deposition and annealing cycles that may be done to completely fill a gap or trench formed in a substrate, or constitute the a partial fill. The method 500 may include depositing a first film 502 in a gap and/or trench, and annealing the film 504. A second dielectric film may then be deposited 506 over the first film and the second film may then be annealed 508. The first anneal 504 may be done at a lower temperature (e.g., up to about 600°C) than the second anneal 508 (e.g., up to a second temperature of about 1000°C). The method 500 may also include

removing a top portion of the first film before or after the anneal 504, and removing a top portion of the second film before or after the anneal 508.

[0049] Fig. 5B shows another method 550 of one or more alternating dielectric deposition and anneal cycles that may continue until a gap and/or trench is completely filled with dielectric material. The method 550 may include depositing a dielectric layer 552 in a trench formed in a substrate and annealing the dielectric layer 554. Following the first deposition and annealing cycle, a determination may be made about whether the trench is completely filled by the dielectric 556. If the trench has been completely filled, then the trench filling is complete 558 and no more dep-anneal cycles are run. If the trench is not completely filled, then at least one more deposition 552 and anneal 554 cycle is run to further fill the trench with dielectric material.

[0050] Figs. 6A-D show cross-sectional views of substrate gaps that are successively filled with two layers of dielectric material according to embodiments of the invention. Fig. 6A shows a portion of a substrate 602 in which gaps 604a-c and trench 606 have been formed. As noted above, the substrate 602 may be made from a semiconductor material such a silicon, and may be a circular silicon substrate wafer having a diameter of about 100mm, 150mm, 200mm, 300mm, 400mm, *etc.* A first dielectric film 608 partially fills the gaps 604a-c and trench 606. The dielectric film 608 may be a flowable dielectric of silicon oxide, nitride, carbon-containing oxide, or oxy-nitride, among other dielectric materials.

[0051] Fig. 6B shows the remaining first dielectric film 608 in the gaps 604a-c and trench 606 following the removal of a top portion of the film. In the example shown, the removal step etched back all the film 608 above the top of the gaps and trench, and recessed the film in the gaps and trench. Following the removal of the top portion, a treatment step may be performed on the remaining film 608 to increase its density and/or hardness before depositing a subsequent layer.

[0052] Fig. 6C shows the deposition of a second dielectric layer 610 on the remaining portion of the first dielectric layer 608. The second dielectric layer 610 completely fills the gaps 604a-c and trench 606 with dielectric, and further extends above the tops of the gaps and trench. The second dielectric layer 610 may also be made from a flowable dielectric material, and may have the same composition as the first dielectric layer 608.

[0053] A top portion of the second dielectric film 608 may be removed to form a planarized dielectric gapfill in the gaps 604a-c and trench 606, as shown in Fig. 6D. The removal of the

top portion of the second film 610 may be done using the same process used to remove the top portion of the first film 608. An anneal may be performed on the first and second deposited films before or after the removal of the top portion of the second film 610. The anneal may be a thermal anneal (*i.e.*, baking), a plasma anneal, a ultraviolet light anneal, an IR irradiative anneal (*e.g.*, RTA), an e-beam anneal, and/or a microwave anneal, among other types of anneals.

[0054] Referring now to Figs. 7A-C, cross-sectional views of substrate gaps on which a first and second dielectric film are deposited according to embodiments of the invention is shown. In Fig. 7A, a first dielectric film 704 is shown completely filling the gaps 706a-c and trench 708 which are formed in substrate 702. A top portion of the first dielectric is then removed as shown in Fig. 7B. The remaining dielectric 704 may be treated (e.g., annealed) before a second layer of dielectric 710 is deposited on the substrate 702.

[0055] The second layer 710 may be a flowable dielectric deposited under the same conditions as the first dielectric layer 704, or it may be deposited by a different deposition method. For example, the second layer 710 may be deposited by a conventional sub-atmospheric chemical vapor deposition process (SACVD), such as HARP, a high-density plasma chemical vapor deposition process (HDP-CVD), or a plasma-enhanced chemical vapor deposition process (PECVD), among other types of processes used to deposit dielectric material. The first and second dielectric layers may then be annealed before or after subsequent processing steps, such as planarizing the top of the dielectric with an etch and/or chemical-mechanical polishing technique.

EXPERIMENTAL

[0056] Figs. 8A&B are electron micrograph images of substrate gaps and a substrate steps following the deposition and etch of a dielectric material according to embodiments of the invention. Fig. 8A shows a series of gaps into which a flowable dielectric film of silicon oxide has been deposited. Fig. 8B shows a step formed in the substrate that is covered with the same flowable oxide film. As both figures show, etching the deposited dielectric before annealing the film eliminates cracking in the final annealed film.

[0057] The silicon oxide film was formed by the reaction of atomic oxygen and TMOS. The atomic oxygen was generated from a source of molecular oxygen (O2) and provided to the deposition chamber containing the substrate at a flow rate of about 1400 sccm. The TMOS was provided to the deposition chamber at rate of about 1850 mgm, and the

deposition chamber pressure was held at about 1.5 Torr during the deposition. This was a low-temperature oxide deposition with the substrate wafer held at a temperature of about 50°C.

[0058] Following the deposition, the silicon oxide was etched in a dry chemical etch process using activated fluorine. The precursor to the activated fluorine was NF_3, which flowed at a rate of 1500 sccm into the chamber holding the substrate. As the total chamber pressure was maintained at about 1.6 Torr, the NF_3 was plasma dissociated and the substrate was exposed to the activated fluorine for about 10 seconds. Then the etched substrate was annealed at about 400°C in an atmosphere that included ozone.

[0059] Figs. 9A&B show comparative electron micrographs of similar substrate gaps (Fig. 9A) and a step (Fig. 9B) with the same silicon oxide dielectric as that was used in Figs. 8A&B. However, in this comparative example the deposited dielectric was not etched before being annealed. As Fig. 9A shows, cracking of the dielectric material occurred in the gaps.

[0060] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Each smaller range between any stated value or intervening value in a stated range and any other stated or intervening value in that stated range is encompassed within the invention. The upper and lower limits of these smaller ranges may independently be included or excluded in the range, and each range where either, neither or both limits are included in the smaller ranges is also encompassed within the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included in the invention.

[0061] As used herein and in the appended claims, the singular forms "a", "and", and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a process" may includes a plurality of such processes and reference to "the precursor" may include reference to one or more precursors and equivalents thereof known to those skilled in the art, and so forth.

[0062] Also, the words "comprise," "comprising," "include," "including," and "includes" when used in this specification and in the following claims are intended to specify the presence of stated features, integers, components, or steps, but they do not preclude the presence or addition of one or more other features, integers, components, steps, or groups.

WHAT IS CLAIMED IS:

1. A method to reduce film cracking in a dielectric layer, the method comprising:

depositing a first dielectric film on a substrate;

removing a top portion of the first dielectric film by performing an etch on the film;

depositing a second dielectric film over the etched first film;

removing a top portion of the second dielectric film; and

annealing the first and second dielectric films to form the dielectric layer, wherein the removal of the top portions from the first and the second dielectric films reduces a stress level in the dielectric layer.

2. The method of claim 1, wherein the depositing of the first and the second dielectric films comprises:

mixing an organo-silicon precursor and atomic oxygen in a deposition chamber; and

reacting the precursors to form a silicon dioxde layer on the substrate.

3. The method of claim 2, wherein the atomic oxygen is generated outside the deposition chamber.

4. The method of claim 2, wherein the atomic oxygen is formed by:

forming a plasma from a gas mixture comprising argon; and

introducing an oxygen precursor to the plasma, wherein the oxygen precursor dissociates to form the atomic oxygen.

5. The method of claim 4, wherein the oxygen precursor is selected from the group consisting of molecular oxygen, ozone, nitrogen dioxide (NO_2), nitrous oxide (N_2O), and water.

6. The method of claim 2, wherein the atomic oxygen is formed by:

introducing an oxygen precursor into a photodissociation chamber; and

exposing the oxygen precursor to ultraviolet light, wherein the ultraviolet light dissociates the oxygen precursor to form atomic oxygen.

7. The method of claim 2, wherein the organo-silicon precursor comprises dimethylsilane, trimethylsilane, tetramethylsilane, diethylsilane, trimethoxysilane (TriMOS), tetramethylorthosilicate (TMOS), triethoxysilane (TriEOS), tetraethylorthosilicate (TEOS), octamethyltrisiloxane (OMTS), octamethylcyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TOMCATS), DMDMOS, DEMS, methyl triethoxysilane (MTES), phenyldimethylsilane, or phenylsilane.

8. The method of claim 1, wherein the etch of the first dielectric film is performed as a wet etch or a dry etch.

9. The method of claim 1, wherein the etch of the first dielectric film is a dry etch performed by exposing the film to a etch gas comprising a fluorine compound.

10. The method of claim 9, wherein the etch gas comprises nitrogen tri-fluoride or an organo-fluorine compound.

11. The method of claim 10, wherein the organo-fluorine compound comprises CF_4, C_2F_6, or C_3F_8.

12. The method of claim 1, wherein the etch of the first dielectric film is a wet etch performed by exposing the film to an acidic solution.

13. The method of claim 12, wherein the acidic solution comprises hydrofluoric acid, hydrochloric acid, phosphoric acid, nitric acid, or sulfuric acid.

14. The method of claim 12, wherein the acidic solution further comprises hydrogen peroxide.

15. The method of claim 1, wherein the etch of the first dielectric film is a wet etch performed by exposing the film to an basic solution.

16. The method of claim 15, wherein the basic solution comprises ammonium hydroxide.

17. The method of claim 16, wherein the basic solution further comprises hydrogen peroxide.

18. The method of claim 8, wherein the etch is a wet etch, and wherein the deposition of the first film and the wet etch of said first film are performed in the same process chamber.

19. The method of claim 8, wherein the etch is a wet etch performed in a different chamber then that used for the deposition of the first dielectric film.

20. The method of claim 1, wherein the first dielectric film has an initial depth of about 1 nm to about 100 nm.

21. The method of claim 1, wherein the method comprises annealing the first dielectric film before the removal of the top portion of the first film.

22. The method of claim 1, wherein the method comprises annealing the first dielectric film before depositing the second dielectric film.

23. A method filling a trench with a dielectric material, the method comprising:

filling the trench with a film of the dielectric material, wherein the dielectric film is formed by:

combining a first fluid stream comprising atomic oxygen with a second fluid stream comprising a silicon-containing precursor, and

reacting the atomic oxygen and the silicon-containing precursor to form the dielectric film in the trench;

removing a top portion of the dielectric film by etching the film; and

annealing the etched film.

24. The method of claim 23, wherein the initially deposited dielectric film extends over a top of the trench.

25. The method of claim 24, wherein the dielectric film is etched back below the top of the trench.

26. The method of claim 25, wherein a capping layer is deposited on the etched back dielectric film.

27. The method of claim 26, wherein the capping layer comprises the same dielectric material as the dielectric film.

28. The method of claim 23, wherein the etching of the film is performed as a wet etch or a dry etch.

29. The method of claim 23, wherein the etching of the film is a dry etch performed by exposing the film to a etch gas comprising a fluorine compound.

30. A method to reduce film cracking in a dielectric layer, the method comprising:

depositing a first dielectric film on a substrate;

performing a first anneal on the first film;

removing a top portion of the annealed first film by performing a first etch on the first film;

depositing a second dielectric film over the etched first film;

removing a top portion of the second dielectric film by performing a second etch on the second film; and

performing a second anneal of the first and second dielectric films and forming the dielectric layer, wherein the removal of the top portions from the first and the second dielectric films reduces a stress level in the dielectric layer.

31. The method of claim 30, wherein the first anneal comprises heating the first film to a temperature up to about 600°C.

32. The method of claim 30, wherein the first anneal is a multistage anneal that comprises the stages of:

heating the first film at a first temperature of up to about 50°C for a first period of time;

heating the first film at a second temperature of about 50°C to about 100°C for a second period of time; and

heating the first film at a third temperature of more than 100°C to about 600°C for a third period of time.

33. The method of claim 32, wherein the first period of time comprises about 1 hour, and the second period of time comprises about 30 minutes.

34. The method of claim 32, wherein the third period of time comprises about 30 minutes to about 1 hour.

35. The method of claim 30, wherein the first anneal comprises irradiating the first film with UV light.

36. The method of claim 30, wherein the first anneal comprises exposing the first film to an inert plasma.

37. The method of claim 30, wherein the first anneal comprises exposing the first film to an electron beam.

38. The method of claim 30, wherein the second anneal comprises heating the first and second layers in a dry, non-reactive gas atmosphere to a temperature of about 800°C or more.

39. The method of claim 38, wherein the dry, non-reactive gas atmosphere comprises nitrogen (N_2).

40. The method of claim 30, wherein the first etch is performed as a wet etch or a dry etch.

41. The method of claim 30, wherein the second etch is performed as a wet etch or a dry etch.

42. The method of claim 30, wherein the method further comprises depositing a third dielectric film over the first and second films; and
removing a top portion of the third dielectric film.

43. The method of claim 42, wherein the method further comprises annealing the first second and third dielectric films to form the dielectric layer, wherein the removal of the top portions of the first, second and third dielectric films reduced the stress level in the dielectric layer.

44. A multistep deposition method for filling a gap on a semiconductor substrate with dielectric material, the method comprising:

depositing a first dielectric film in a bottom portion of the gap;

annealing the first dielectric film in a first anneal;

depositing a second dielectric film on the annealed first dielectric film; and

annealing the second dielectric film in a second anneal.

45. The multistep deposition of claim 44, wherein the method comprises:

depositing a third dielectric film on the annealed second dielectric film; and

annealing the third dielectric film in a third anneal.

46. The multistep deposition of claim 44, wherein the first anneal comprises a thermal anneal, an e-beam anneal, an ultra-violet light anneal, or a plasma anneal.

47. The multistep deposition of claim 44, wherein the second anneal comprises a thermal anneal, an e-beam anneal, an ultra-violet light anneal, or a plasma anneal.

48. The multistep deposition of claim 44, wherein the first anneal is performed at a lower temperature than the second anneal.

49. The multistep deposition of claim 48, wherein the first anneal is performed at a first temperature up to about 600°C and the second anneal is performed at a second temperature up to about 1000°C.

50. The multistep deposition of claim 44, wherein the method comprises performing a first etch of the annealed first dielectric film before the depositing of the second dielectric film.

51. The multistep deposition of claim 50, wherein the etch removes a top portion of the first dielectric film.

52. The multistep deposition of claim 50, wherein the etch comprises a wet etch or a dry etch.

53. The multistep deposition of claim 50, wherein the etch comprises exposing the film to a etch gas comprising a fluorine compound.

54. The multistep deposition of claim 44, wherein the method comprises performing a second etch of the second dielectric film.