

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Pulse Storage Circuit

We, HAYAKAWA DENKIKOGYO KABUSHIKI KAISHA, a Japanese Company, of 22—22 Nagaïke-cho, Abeno-ku, Osaka-shi, Osaka-fu, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to pulse storage circuits, especially pulse storage circuits including MOS type field effect transistors providing storage action.

Recently integration of semiconductor circuits has been intensely studied and improved, especially in the field of electronic computers. Various investigations have been made concerning a pulse storage circuit as a least memory unit of an electronic computer.

A number of forms of pulse storage circuits of the static type using MOS field effect transistors have been developed, but they leave various problems unsolved.

A MOS field effect transistor, when used as an amplification element, has a gate internal capacitance as a result of its structure, and pulse storage operation is effected by utilizing this storage effect.

By way of example, when a delay type pulse storage circuit is constituted by at least two such amplification elements having storage time, the amplification elements are connected in cascade and a feedback path is provided between the amplification element of the second stage and the amplification element of the first stage to form one circulation loop. Moreover, switches which are concurrently controlled by a single synchronizing control signal (clock signal) are respectively inserted in a forward path from the first stage to the second stage and a feedback path from the second stage to the first stage.

In practical operation, however, since the state of the second stage (conduction or non-

conduction) changes and the input information is newly stored in the amplification element of the first stage and the forward path and the feedback path between the first stage and the second stage is then concurrently closed by introducing the synchronizing signal, operation may become unstable and correct storage of information may become impossible.

For example, supposing the transistors are of the P-channel type and, when a negative potential is previously stored in a gate capacitance of the transistor of the second stage and the drain terminal of the second-stage is at zero potential, input information is supplied and a negative potential is newly stored in the gate capacitance of the first stage, then the transistor of the first-stage is conductive and its drain terminal is in zero potential state at this time.

The drain potential of the first-stage in this state tends to write new information in the second-stage but the zero potential which exists previously tends to cancel the negative potential in the gate capacitance of the first stage and has the disadvantage of erasing the new information. Therefore, it is necessary to make the time constant of the feedback path such as to prevent this disadvantage. For this purpose, use of MOS field effect transistors having analog quantities, e.g. different mutual conductances or gate capacitances can be considered but stable operation cannot be expected when there is fluctuation. Moreover, it is difficult to manufacture such elements having different characteristics on the same semiconductor wafer.

Accordingly, an object of this invention is to provide a pulse storage circuit which solves the abovementioned problems and provides a stable memory operation.

According to the invention there is provided a pulse storage circuit comprising at least one first stage MOS type field effect

[Price 5s. 0d.]

transistor and at least one second stage MOS type field effect transistor, said field effect transistors each having input and output terminals and a gate internal capacitance in which an electric charge corresponding to the information pulse is temporarily stored, first switching means connecting a forward path from the output of the first stage to the input of the second stage for controlling a transmission of stored information in the gate internal capacitance of the first stage to the second stage, second switching means connecting a feedback path from the output of second stage to the input of the first stage means for applying a stored information pulse to the input of the first stage, and means capable of generating at least two synchronizing control pulses with the phase of one pulse shifted relative to other pulse and operable to actuate said second switching means after the application of said information pulse and then actuate said first switching means upon the elapse of a time period after actuation of the first switching means. Thus, it is unnecessary to use elements having different mutual conductances or gate capacitances in combination and more stable operation can be obtained as compared with that combination.

In order that the invention may be clearly understood and readily carried into effect apparatus in accordance therewith will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a circuit diagram of a pulse storage circuit;

Figure 2 is a waveform diagram at various stages in the operation of the circuit of Figure 1, and

Figure 3 is a circuit diagram of another embodiment of the invention.

Throughout the drawings, like reference characters are used for like elements.

Figure 1 represents an embodiment of synchronous static pulse storage circuit of the delay type according to this invention. All of the respective circuit elements are constituted of MOS field effect transistors of P-channel type but some of them do not exhibit a transistor effect.

Each of two field effect transistors 1 and 2 has inherent floating capacitance between the gate electrode and the substrate, and by storing an electric charge corresponding to information pulse it temporarily memorizes information. Each gate electrode becomes an input portion, the source electrode is grounded and the drain electrode is connected to V_{DD} power source through a load resistor which will be explained later. The drain electrode of the first stage transistor 1 is connected to the gate electrode of the second stage transistor 2 to form a cascade connection, and the memory charge of the first stage is trans-

ferred while being inverted to the gate internal capacitance of the second stage. The drain end of the second stage transistor 2 is connected to the gate end of the first stage transistor 1 to form an information feedback path, and thus it is so arranged that an information can be circularly memorized by the two transistors 1 and 2. Field effect transistors 3, 4 and 5 are controlled according to presence and absence of synchronizing control signals having different phases and operate as switching elements, respectively.

Synchronizing control signals ϕ_1 , ϕ_2 and ϕ_3 are respectively supplied to the gate electrodes of the transistors 3, 4 and 5 and the source and drain electrodes of the transistors 3, 4 and 5 are inserted in circuit to be controlled by switching. Field effect transistors 6 and 7 respectively connected to the drain electrodes of the transistors 1 and 2 operate as load resistors of said transistors 1 and 2.

The upper half of Figure 2 represents waveforms of pulse trains to be supplied to the above circuit. The synchronizing control signals ϕ_1 , ϕ_2 and ϕ_3 are to be supplied to the switching elements 3, 4 and 5 respectively. The synchronizing control signals ϕ_2 and ϕ_3 are shifted by a small amount with respect to the reference synchronizing signal ϕ_1 .

Operations of the above circuit arrangements based on adoption of the above synchronizing control signals are as follows.

When an input signal is supplied to the switching transistor 3 and the synchronizing control signal ϕ_1 is applied thereto, the memory transistors 1 is driven in synchronization with the synchronizing control signal ϕ_1 , and information is stored in the gate capacitance of the memory transistor 1 of the first-stage. The synchronizing control signal ϕ_2 is then supplied to the switching transistor 4 to render said switching transistor 4 conductive. Then the memory transistor 2 of the second-stage is driven in synchronization with the synchronizing control signal ϕ_2 and the information is transferred to the gate capacitance of the memory transistor 2 of the second-stage. In the prior art, at the instant that this state is going to occur, a forward path from the first-stage to the second-stage and a feedback path from the second-stage to the first-stage are provided. In this circuit since the synchronizing control signal ϕ_3 is not yet introduced into the switching transistor 5 the feedback path to the first stage remains open, and there is no interference by the second stage transistor 2 to the first stage. Then, when the synchronizing control signal ϕ_3 is introduced the feedback path from the second stage to the first stage is closed, and the memory charge of the second stage is transferred to the gate internal capacitance of the first stage. Later, if a new information pulse is applied at the time of introduction of the synchronizing control signal ϕ_1 , storage

corresponding to the input information is maintained irrespective of the previous memory content of the first stage. In the case of no new input information, however, the memory content is again transferred to the gate internal capacitance of the second stage due to an introduction of the synchronizing control signal ϕ_2 , and by repetition of this operation one bit information is memorized virtually statically.

Further, there is present during the cut off time of the synchronizing control pulse a path from the gate electrode to the ground through the source electrode and at the time of open path through the switching transistor to the ground a discharge path with respect to the gate internal capacitance, but both exhibit a high impedance and, therefore, the information will not disappear.

The lower half of Figure 2 represents voltage waveforms at points A, B, C and D in the above circuit. As shown in the drawing, an output delayed by one period (of the synchronizing control signal ϕ_2) with respect to the input signal is obtained at the point D. As shown in the right-hand side of said drawing, at the time of absence of the synchronizing control signal ϕ_1 , it continues to store the input signal just ahead of it, cyclically. In the case of using this circuit in a register of an electronic computer, it serves as a memory unit of one bit and the switch 3 controls information transmission between bit and bit, the synchronizing control signal ϕ_1 being omitted.

As described above, a method of utilizing the synchronizing signal ϕ_1 in place of the synchronizing signals ϕ_2 and ϕ_3 in the memory transistor 1 of the first-stage after the memory transistor 2 of the second-stage responds perfectly can be also considered but it is undesirable when there are variations as abovementioned since, in this case, the memory transistors 1 and 2 must be handled in the analog mode by having different gate capacitances or mutual conductances.

The operation function table of the abovementioned circuit arrangement is as the under, wherein D^n is an input, Q^{n+1} is an output, and n is a bit time.

D^n	Q^{n+1}
0	0
1	1

Figure 3 is a structural diagram of a pulse storage circuit of the JK-type constituted by utilizing the above delay type pulse storage circuit as it is. JK type has the following operation function table, in which J, K are inputs, Q^{n+1} is an output, and n is a bit time.

J	K	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	Q^n

As can be understood from the above table, it is when the condition of KQ is established that the output state 1 of the memory circuit is changed to 0, and it is when the condition

of JQ is met that the output state 0 is changed to 1. Accordingly, such special consideration as the above is required at the time of application of the aforementioned circuit. Therefore, gate elements 8 and 9 which conduct under the condition KQ through the switching transistor 3 and gate elements 10 and 11 which conduct under the condition of

JQ through the switching transistor 3 are connected to the input side of the first stage transistor 1.

Since the pulse storage circuit of this invention performs information storage by use of three synchronizing control signals having different phases and by closing the feedback path to the memory transistor of the first-stage after perfect response of the last memory transistor, as described above, extremely stable operation can be obtained as compared with a combination of elements having different mutual conductances or gate capacitances. As it can be used as both a static type and a dynamic type according to presence and absence of the synchronizing control signal ϕ_1 , moreover, it can control easily shift and storage states. Especially, the circuit of this invention contributes to integration of semiconductors in an electronic computer and has a large industrial worth.

WHAT WE CLAIM IS:—

1. A pulse storage circuit comprising at least one first stage MOS type field effect transistor and at least one second stage MOS type field effect transistor, said field effect transistors each having input and output terminals and a gate internal capacitance in which an electric charge corresponding to the information pulse is temporarily stored, first switching means connecting a forward path from the output of the first stage to the input of the second stage for controlling a transmission of stored information in the gate internal capacitance of the first stage to the second stage, second switching means connecting a feedback path from the output of second stage to the input of the first stage means for applying a stored information pulse to the input of the first stage, and means capable of generating at least two synchronizing control pulses with the phase of one pulse shifted relative to other pulse and oper-

corresponding to the input information is maintained irrespective of the previous memory content of the first stage. In the case of no new input information, however, the memory content is again transferred to the gate internal capacitance of the second stage due to an introduction of the synchronizing control signal ϕ_2 , and by repetition of this operation one bit information is memorized virtually statically.

Further, there is present during the cut off time of the synchronizing control pulse a path from the gate electrode to the ground through the source electrode and at the time of open path through the switching transistor to the ground a discharge path with respect to the gate internal capacitance, but both exhibit a high impedance and, therefore, the information will not disappear.

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As described above, a method of utilizing the synchronizing signal ϕ_1 in place of the synchronizing signals ϕ_2 and ϕ_3 in the memory transistor 1 of the first-stage after the memory transistor 2 of the second-stage responds perfectly can be also considered but it is undesirable when there are variations as abovementioned since, in this case, the memory transistors 1 and 2 must be handled in the analog mode by having different gate capacitances or mutual conductances.

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1	0	1
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able to actuate said second switching means after the application of said information pulse and then actuate said first switching means upon the elapse of a time period after actuation of the first switching means.

5 2. A pulse storage circuit as claimed in Claim 1, wherein input switching means is connected to the input of said first stage and said input switching means, first switching
10 means and second switching means are sequentially actuated by the introduction of three synchronizing control pulses with the phase of each pulse shifted with respect to the other two.

15 3. A pulse storage circuit as claimed in Claim 2, wherein said input, first and second switching means are MOS type field effect transistors and said three synchronizing control pulses are applied to the gates of the
20 last said transistors.

25 4. A pulse storage circuit as claimed in Claim 3, wherein said first and second stage transistors have gate, source and drain terminals and the drain electrode of each such transistor is connected to a voltage supply through a respective field effect transistor functioning as a load impedance.

5. A pulse storage circuit as claimed in any one of Claims 2 to 4, further including gate elements connected to the input switching means and feed-back paths connected from the output of the second stage to said gate elements to constitute a so-called JK type circuit.

6. A pulse storage circuit as claimed in Claim 5 wherein said gate elements comprise field effect transistors.

7. A pulse storage circuit as claimed in any preceding Claim formed as an integrated circuit.

8. A pulse storage circuit substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.

9. A pulse storage circuit substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

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