CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor processing apparatus, configured to process a wafer, the semiconductor processing apparatus comprising:

a vacuum interlock chamber;

a plurality of apparatus bodies, the apparatus body including a transfer platform, and at least two reaction chambers being arranged along a circumferential direction of the transfer platform; and

a temporary storage channel, any two neighboring of the apparatus bodies being communicated through the temporary storage channel, and the temporary storage channel being configured to temporarily store the wafer;

wherein the transfer platform transfers the wafer between the vacuum interlock chamber and the reaction chamber, between the temporary storage channel and the vacuum interlock chamber, and between the temporary storage channel and the reaction chamber;

wherein the plurality of apparatus bodies include:

a first apparatus body connected to the vacuum interlock chamber, a shape of the transfer platform of the first apparatus body being a regular quadrilateral; and

a second apparatus body, a shape of the transfer platform of the second apparatus body being a regular pentagon.

2. The semiconductor processing apparatus according to claim 1, wherein a temporary storage table is arranged in the vacuum interlock chamber, and the temporary storage table is configured to temporarily store the wafer; and

one side of the vacuum interlock chamber is connected to the first apparatus body, a first gate valve is arranged at connection of the vacuum interlock chamber and the first

apparatus body, the other side of the vacuum interlock chamber is connected to an external apparatus, and a second gate valve is arranged at connection of the vacuum interlock chamber and the external apparatus.

3. The semiconductor processing apparatus according to claim 2, wherein a number of the temporary storage table is multiple.

4. The semiconductor processing apparatus according to claim 1, wherein a shape of the transfer platform is a quadrilateral, a pentagon, or a hexagon.

5. The semiconductor processing apparatus according to claim 4, wherein the shape of the transfer platform is a regular quadrilateral, a regular pentagon, or a regular hexagon.

6. The semiconductor processing apparatus according to claim 4, wherein at least two reaction chambers are arranged on at least one side of the transfer platform.

7. The semiconductor processing apparatus according to claim 4 or 5 or 6, wherein the shape of the transfer platform is the quadrilateral or the hexagon;

the vacuum interlock chamber and the temporary storage channel are connected to the transfer platform at positions corresponding to two opposite sides of the transfer platform, respectively.

8. The semiconductor processing apparatus according to claim 1, wherein the apparatus body further includes a conveying mechanism, and the conveying mechanism is arranged on the transfer platform.

9. The semiconductor processing apparatus according to claim 8, wherein the conveying mechanism is a manipulator, and the manipulator includes at least two wafer grabbing devices.

10. The semiconductor processing apparatus according to claim 1, wherein the temporary storage channel includes a plurality of wafer placement tables, and the wafer placement tables are configured to temporarily store wafers.

11. The semiconductor processing apparatus according to claim 1, wherein the reaction chamber includes an atomic layer deposition (ALD) process chamber or a chemical vapor deposition (CVD) process chamber.