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DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Signal Translating Circuits Using Field-Effect Transistors.

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to signal translating circuits, using field-effect transistors.

One type of field-effect transistor, known as an insulated gate field-effect transistor, has source, drain and gate electrodes formed on a semi-conductor substrate. The gate electrode is disposed on a layer of insulating material over-lying a conducting channel between the source and drain electrodes.

Ordinarily signal translating circuits utilizing the insulated gate field-effect transistor include an input circuit coupled between the source and gate electrodes so that the current in the conducting channel is modulated in accordance with the electrical field produced by the input signal voltage. The amplified signal is developed in an output circuit coupled between the source and drain electrodes.

We have ascertained that the insulated gate field-effect transistor can be advantageously employed in signal translating circuits.

In accordance with the present invention, we provide a signal translating circuit comprising an insulated gate field-effect transistor of the type referred to, an input circuit coupled between the source electrode and the substrate of the transistor, with said substrate either reverse biased relative to the source electrode to form therewith a

rectifying junction having a capacitance or forward biased relative to the source electrode to form therewith a bipolar transistor junction, a bias voltage applied to the gate electrode of the transistor to determine the operating characteristic of the transistor, and an output circuit connected between the source and drain electrodes of the transistor, the input circuit being either with or without a portion coupled between the gate and source electrodes.

Referring to the accompanying drawings:

FIGURE 1 is a diagrammatic view of a field-effect transistor;

FIGURE 2 is a section along lines 2—2 of FIGURE 1;

FIGURE 3 is a graph showing current vs. drain voltage curves for various values of gate-to-source voltages for the transistor of FIGURE 1;

FIGURE 4 is a schematic diagram of an example of an insulated gate field-effect transistor amplifier circuit embodying the invention;

FIGURE 5 is a graph of the transconductance vs. substrate bias voltage characteristic of the amplifier circuit of FIGURE 4;

FIGURE 6 is a schematic circuit diagram of another amplifier circuit embodying the invention;

FIGURE 7 is a graph showing the comparative transconductance characteristics of the amplifier circuit of FIGURE 6 with that of similar circuit wherein the substrate is grounded;

FIGURE 8 is a schematic diagram of a further amplifier circuit embodying the invention;

FIGURE 9 is a schematic circuit diagram of a mixer circuit embodying the invention;

FIGURE 10 is a schematic circuit dia-

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gram of a dual frequency amplifier embodying the invention;

FIGURE 11 is a schematic representation of the field-effect transistor shown in FIGURES 1 and 2;

FIGURE 12 is a schematic diagram of a still further insulated gate field-effect amplifier circuit embodying the invention;

FIGURE 13 is a graph of the drain voltage vs. drain current characteristic of the transistor shown in FIGURE 12 for different forms of gate bias voltage;

FIGURE 14 is a schematic circuit diagram of an amplifier circuit embodying the invention wherein different signals are applied to the gate and substrate electrodes; and

FIGURE 15 is a schematic circuit diagram of a self-oscillating frequency converter circuit embodying the invention.

Referring now to FIGURE 1, a field-effect transistor 10 which may be used with circuits embodying the invention includes a body 12 of semiconductor material. The body 12 may be either a single crystal or polycrystalline and may be of any of the semiconductor materials used to prepare transistors in the semiconductor art. For example the body 12 may be nearly intrinsic silicon, such as for example lightly doped P-type silicon of 500 to 1000 ohm cm. material.

In the manufacture of the transistor shown in FIGURE 1, heavily doped silicon is deposited over the surface of the silicon body 12. The silicon dioxide is doped with n-type impurities. By means of a photo-resist and acid etching, or other suitable technique the silicon dioxide is removed in the area where the gate electrode is to be formed, and around the outer edges of the silicon wafer as viewed on FIGURE 1. The deposited silicon dioxide is left undisturbed over those areas where the source-drain regions are to be formed.

The body 12 is then heated in a suitable atmosphere, such as in water vapour, so that exposed silicon areas are oxidized to form grown silicon dioxide layers indicated by the lightly stippled areas of FIGURE 1. During the heating process, impurities from the deposited silicon dioxide layer diffuse into silicon body 12 to form the source and drain regions. FIGURE 2, which is a cross section view taken along section line 2-2 of FIGURE 1, shows the source-drain regions labelled S and D respectively.

The remaining part of the body 12, that is the part or stratum thereof which is beneath the source and drain regions, is herein termed the substrate.

By means of another photo-resist and acid etching or like step the deposited silicon dioxide over part of the source-drain diffused

regions are removed. Electrodes are formed for the source, drain and gate regions by evaporation of a conductive material by means of an evaporation mask. The conductive material evaporated may be chromium or gold, for example, but other suitable metals may be used.

The finished wafer is shown in FIGURE 1, in which the stippled area between the outside boundary and the first dark zone 14 is grown silicon dioxide. The white area 16 is the metal electrode corresponding to the source electrode. Dark zones 14, 18 are deposited silicon dioxide zones overlying the diffused source region and the dark zone 20 is a deposited silicon dioxide zone overlying the diffused drain region. White areas 22 and 24 are the metallic electrodes which correspond to the gate and drain electrodes respectively. The stippled zone 28 is a layer of grown silicon dioxide on a portion of which the gate electrode 22 is placed and which insulates the gate electrodes 22 from the substrate silicon body 12 and from the source and drain electrodes as shown in FIGURE 2. The silicon wafer is mounted on a conductive base or header 26 as shown in FIGURE 2. The layer of grown silicon dioxide 28 on which the gate electrode 22 is mounted, overlies an inversion layer or conducting channel C, shown in dotted lines, connecting the source and drain regions. The gate electrode 22 is displaced towards the source region S so that the distance between the source region S and the gate electrode 22 is smaller than the distance of the gate electrode 22 and the drain region D. If desired the gate electrode may slightly overlap the deposited silicon dioxide layer 18 above the source electrode. It will be noted that the transistor is symmetrical, other than for the offset gate electrode, and that either of the electrodes D and S operate as the drain and the source electrodes as a function of the polarity of the bias potential applied therebetween; i.e. the electrode to which a positive bias potential is applied therebetween; i.e. the electrode to which a positive bias potential is applied relative to the bias potential applied to the other electrode operates as a drain electrode and the other electrode operates as a source electrode.

The input resistance of the transistor described above is very high, measuring approximately 10^{14} ohms at d-c.

FIGURE 3 is a family of curves 30-39 illustrating the drain current versus drain voltage characteristic of the transistor of FIGURE 1 for different values of gate-to-source voltage. Drain current in milliamperes is plotted along the ordinate, against drain voltage along the abscissa. A feature of an insulated gate field-effect tran-

sistor is that the zero bias characteristic can be at any of the curves 30—39. In FIGURE 2 the curve 37 corresponds to the zero bias gate-to-source voltage. Curves 38 and 39 represent positive gate voltages relative to the source and the curves 30—36 represent negative gate voltages relative to the source. The gate voltages are indicated at the right of the FIGURE.

The location of the zero bias curve is selected during the manufacture of the transistor, i.e. by controlling the time and/or temperature of the step of the process when the silicon dioxide layer 28 shown in FIGURES 1 and 2 is grown.

The amplifier circuit of FIGURE 4 utilizes an insulated gate field-effect transistor 40 similar to the one described in connection with FIGURES 1 and 2. The transistor 40 has a source electrode 42 a drain electrode 44, a gate electrode 46 and a substrate electrode 48. The source electrode 42 and the gate electrode 46 are both connected to a point of reference potential, shown as ground. If desired the gate electrode may be biased to a desired potential, not shown, to control the translation characteristics of the circuit. The drain electrode 44 is connected through a resistor 56 to the positive terminal of a source of bias potential 60 which is shown as a battery. The negative terminal of the bias potential source 60 is connected to ground.

The substrate electrode 48 is coupled to a source 62 of signals to be amplified through a signal coupling capacitor 64. The bias potential on the substrate electrode 48 is set by a potential source 66, which is shown as a battery of adjustable voltage, and a resistor 68 which are connected in series between the substrate electrode and ground.

The source of potential 66 is poled to reversely bias, that is negatively bias, the substrate electrode 48 with respect to the source and drain electrodes 42 and 44 respectively. It will be noted with the transistor construction shown in FIGURES 1 and 2 that the source and drain regions S and D are of N-type material, whereas the substrate electrode 48 is of P-type material. The interface between the substrate electrode 48 and either of the source or drain electrodes comprises a P-N rectifying junction. As is known, to reversely bias such a P-N junction the negative terminal of a potential source is connected to the P region and the positive terminal of the source is connected to the N region. Naturally, if the substrate region is of N-type material relative to the source and drain regions, the potential supply source 66 will be poled to maintain the substrate electrode positive relative to the source and drain electrodes. In the circuit of FIGURE 4 it will be noted

that the substrate-source rectifying junction is reverse biased by an amount equal to the voltage exhibited by the potential source 66, whereas the substrate-drain rectifying junction is reverse biased by an amount equal to the sum of the potentials exhibited by the potential sources 60 and 66. The amplified output may be taken from across the resistance 56.

The transconductance of the amplifying circuit shown in FIGURE 4 as a function of the d-c voltage on the substrate electrode is shown in FIGURE 5. In FIGURE 5, transconductance in milliohms is plotted along the ordinate, according to a logarithmic scale. Substrate voltages are indicated along the abscissa. It will be noted that the transconductance of the circuit of FIGURE 4 is maximum for relatively small negative potentials applied to the substrate electrode 48, and decreases as the substrate is made more negative. It is thought this change in transconductance is due to a field-effect type action somewhat similar to that effected if potentials were applied to the gate electrode 46.

Advantage is taken of the substrate transconductance characteristic in the amplifier circuit of FIGURE 6. The circuit of FIGURE 6 includes an insulated gate field-effect transistor 70 of the type described in connection with FIGURE 2. The transistor includes a source electrode 72, a drain electrode 74, a gate electrode 76 and a substrate electrode 78. The source electrode is grounded and the drain electrode 74 is connected through a resistor 80 and an operating potential supply 82 to ground. The resistor 80 represents the impedance of any suitable load for the amplifier circuit.

Signals to be amplified from a source 84 are coupled through a signal coupling capacitor 86 to the gate electrode 76 and to the substrate electrode 78 through a direct current conductive connection 88. The gate and substrate electrodes 76 and 78 are biased to the desired operating potential by an adjustable source of operating potential 90 which is connected in series with a resistor 92 between the gate electrode 76 and ground. As is shown, the gate and substrate electrodes are biased negatively with respect to ground. It is to be understood that the circuit may be self-biased, if desired, by the use of a bypassed source resistor. Alternatively it will be understood that a single supply source with suitable voltage divider networks may supply the operating potentials for the source-drain and biasing circuits. The amplified output may be taken from across the resistance 80.

The transconductance vs. gate voltage characteristic for the circuit of FIGURE 6 is shown by the curve 94 in FIGURE 7. In FIGURE 7, transconductance in milli-

ohms is represented on a logarithmic scale along the ordinate, and gate voltage is represented along the abscissa.

This transconductance characteristic may be compared with that of a similar circuit where the substrate electrode 78 is disconnected from the gate electrode 76 and is grounded. The transconductance of such a modified circuit is shown by the curve 96 of FIGURE 7. It has been found that the maximum transconductance of the circuit of FIGURE 6 is increased as much as 50% as compared to circuits where the input signals are applied only to the gate electrodes. It will be noted from FIGURE 7 that the circuit of FIGURE 6 exhibits a characteristic 94 which tends to cut off more quickly than circuits where the substrate is grounded. The reason for this is that the depleting fields of the substrate and gate electrodes compliment each other to enable a sharper cutoff.

If desired, the cut off characteristic of an amplifier may be tailored to a predetermined characteristic by applying different biasing voltages to the gate and substrate electrodes as is shown in FIGURE 8. The circuit of FIGURE 8 is similar to that of FIGURE 6, and like components are given corresponding primed reference numerals. The main difference between the circuits of FIGURE 6 and FIGURE 8 is that the gate electrode 76¹ and the substrate electrode 78¹ are isolated for direct currents by a d-c blocking capacitor 98. In addition, different d-c bias voltages are applied to the gate electrode 76¹ and substrate electrode 78¹ through resistors 100 and 102 respectively. The initial biasing voltages on the gate and substrate electrodes may be set to provide an initial maximum transconductance characteristic. Various combinations of different biasing potentials could be applied respectively to the electrodes 76¹ and 78¹ to provide different or modified transconductance vs. control voltage characteristics with different curve configurations from those indicated by the curves 94 and 97 of FIGURE 7.

Since the gate and substrate electrodes each provide control over the transconductance of the insulated gate field-effect transistor, the device may find use as a signal mixer as shown in FIGURE 9. The transistor 110 which is of the type described in connection with FIGURES 1 and 2 has a source electrode 112 and a drain electrode 114, a gate electrode 116 and a substrate electrode 118. Signals from a first signal source, represented by the terminals 119, are applied to the gate electrode 116 through a signal coupling capacitor 120 and gate biasing resistor 122. Signals from a second source, represented by the terminals 121, are applied to the substrate electrode 118 through a

signal coupling capacitor 124 and a substrate bias resistor 126. The source electrode 112 is connected to a point of reference potential, such as ground, through a resistor 128, which may be bypassed for signal frequencies, if desired. The voltage across resistor 128 provides a self-biasing voltage which establishes the desired operating point for the gate and substrate electrodes 116 and 118 respectively, and maintains the source electrode at a positive potential relative to the gate and substrate electrodes. An output circuit represented by the resistor 130 couples the drain electrode 114 to the positive terminal of a source of operating potential 132. Signals develop across the resistor 130 are coupled to suitable utilization means (not shown) through a signal coupling capacitor 134.

The circuit of FIGURE 9 is useful as a signal mixer for combining the signals applied to the gate and substrate electrodes. If desired, the mixer may be of the type used in superheterodyne signal receivers wherein one of the signals comprises a source of signal modulated carrier waves and the other source of signals comprises waves from a local oscillation generator. The desired output frequency from the heterodyne process is selected by the use of an output circuit tuned to the desired frequency, which in superheterodyne receivers, is usually the difference between the local oscillator and signal modulated carrier wave frequencies. In like manner, the circuit may also be adapted for use as a product detector such as a synchronous detector or differential amplifier or the like.

Another embodiment of the invention is shown in FIGURE 10 which is an amplifier for two signals of different frequencies. A transistor device 140 which may be of the type shown and described in connection with FIGURES 1 and 2 includes a source electrode 142, a drain electrode 144, a gate electrode 146 and a substrate electrode 148. Signals from a first source of signals of a first frequency, represented by terminals 149, are coupled to a gate electrode 146 through a coupling capacitor 150 and a gate bias resistor 152. Signals from a second source of signals of a second and different frequency, represented by terminals 153, are coupled to the substrate electrode 148 through a signal coupling capacitor 154 and a substrate biasing resistor 156. The source electrode 142 is connected to ground through a resistor 158 which is bypassed by a capacitor 160 which is of low impedance to signals from both signal sources.

The drain electrode 144 is connected through the series connection of a first output circuit 162 and a second output circuit 163 to the positive terminal of a source of operating potential 166.

The output circuit 162 is tuned to the higher of the first and second frequencies of signals from the two signal sources and signals from the other of the two sources are developed across the resistor 164. Signals developed in the circuit 162 are bypassed around the resistor 164 by a capacitor 170, and around the battery 166 by the capacitor 172. The capacitor 170 exhibits low impedance to signals developed across the circuit 162, but high impedance to the signals from the other source which are developed across the resistor 164. The capacitor 172 is of low impedance to signals from both of the two sources. Signals developed across the tuned output circuit 162 are coupled by a winding 168 to a utilization circuit (not shown). Signals developed across the resistor 164 are coupled through a coupling capacitor 174 to a utilization circuit (not shown).

By way of example, the amplifier circuit shown in FIGURE 10 may comprise an amplifier circuit of the type commonly used in broadcast radio receivers. The signals which are applied to the gate electrode, for example, comprise a signal modulated intermediate frequency wave which is translated by the amplifier stage and coupled by way of the winding 168 to suitable signal detection means where the audio modulation components of the wave are derived. The audio frequency signal may then be applied to the substrate electrode 148, with the translated audio frequency signal being developed across the resistor 164. The audio frequency signals may then be coupled through the capacitor 174 to further audio amplifier stages. If two relatively high frequency signals of different frequencies are to be amplified such as for example intermediate frequency or radio frequency signals of different frequencies such as are encountered in AM-FM broadcast receivers, the resistor 164 and capacitor 170 may be replaced by a suitably tuned circuit which responds to one of the two intermediate frequencies.

In connection with FIGURES 9 and 10 it is to be understood that different bias voltages may be used on the gate and substrate electrodes. One of these bias voltages, for example may be derived by a source biasing resistor which maintains the source electrode positive with respect to the gate and substrate electrode. The other of the voltages may be obtained from a suitable operating potential supply such as a voltage divider network across the amplifier power supply.

In the circuits of FIGURES 4, 6, and 8-10 the substrate electrode is reversely biased relative to the source electrode so that the translation of signals applied to the substrate electrode is by a field-effect type of action.

The impedance looking into the substrate electrode when it is reversely biased relative to the source electrode is very high thereby enabling efficient coupling to a high impedance signal source. Since the input impedance looking into the gate electrode is also very high, signals from a single high impedance source may be simultaneously applied to both the gate and the substrate electrodes as shown in FIGURES 6 and 8, or signals from separate high impedance sources may be applied to the source and substrate electrodes as is shown in FIGURES 9 and 10.

Circuits wherein the signals applied to the substrate electrode are translated by transistor action, as in junction transistors, or by a combination of transistor action and field-effect action, are shown in FIGURES 11-15.

FIGURE 11 is a schematic representation of the semiconductor device shown in FIGURES 1 and 2 wherein the gate electrode is represented by the reference character 240 and the interchangeable source and drain electrodes are indicated by the reference characters 242 and 244. The substrate electrode is indicated by the reference character 246. It will be noted with the transistor construction shown in FIGURES 1 and 2 that the source and drain regions S and D are of N-type material, whereas the substrate 246 is of P-type material. The interface between the substrate 246 and the drain and source electrodes comprises a pair of P-N rectifying junctions 248 and 250 respectively. If, as mentioned above, the substrate region is of N-type material relative to the source and drain regions, the poling of the rectifying junctions 248 and 250 will be reversed.

It has been found that, with proper circuit connections, transistor action can be obtained if the substrate electrode 246, the drain electrode 244 and the source electrode 242 are considered as the base, collector, and emitter electrodes respectively of a bipolar or junction transistor, of the NPN type. If the material of the substrate region is N-type relative to that of the source and drain regions the transistor effectively appears as a PNP type transistor. As mentioned hereinbefore, the discussion of the circuits shown in the drawings is restricted to the type of transistor described in connection with FIGURES 1 and 2 having a P-type substrate region. However, it is to be understood that by simple circuit modifications the principles of the invention may also be applied where the substrate is of N-type material.

The amplifier circuit of FIGURE 12 utilizes the insulated gate field-effect transistor 252 similar to the one described in connection with FIGURES 1 and 2. The

transistor 252 has a source electrode 254, a drain electrode 256, a gate electrode 258 and a substrate electrode 260. The source 254 is connected through a resistor 256, which is bypassed for signal frequencies by a capacitor 258, to a source of reference potential, shown as ground. The gate electrode 258 is grounded for signal frequencies by a capacitor 262, and a direct current (d-c) bias voltage is applied to the gate electrode 258, from a source (not shown). Although the potential applied to the gate electrode is shown to be negative, a positive biasing potential could be applied if desired. The drain electrode 56 is connected through a resistor 266 to the positive terminal of a source of bias potential 268 which is shown as a battery. The negative terminal of the battery 268 is connected to ground.

The substrate electrode 260 is coupled to a source 270 of signals, to be amplified through a signal coupling capacitor 272. The bias potential on the substrate electrode 260 is derived from a voltage divider comprising a pair of resistors 274 and 276 connected across the battery 268. For signal amplification the substrate electrode 260 is biased to the positive polarity relative to the source electrode so that the substrate electrode 260 and source electrode 254 act as a forward biased base-emitter junction of an NPN type junction transistor. It will be noted that the substrate electrode 260 is less positive than the drain electrode 256 so that these electrodes operate as a reversely biased base-collector junction. Amplified signals developed at the drain electrode 256 are coupled to suitable utilization means (not shown).

The drain voltage vs. drain current characteristics as a function of the substrate bias current is shown in FIGURE 13. In this FIGURE, drain-collector current in milliamperes is represented along the ordinate, and drain-collector voltage along the abscissa. The substrate current for each curve is indicated adjacent to each curve, at the right end thereof. The six curves at the top of the FIGURE are for a gate bias of 4 volts, and those below for a gate bias of 6 volts. It has been found that the gate electrode 258 may be used to control the source-drain substrate beta (β). In this case the term beta is equal to an incremental change in drain current divided by an incremental change in substrate current. Since the gate electrode controls the beta a control voltage such as an automatic gain control (AGC) voltage may be applied to the gate 258 to change the junction transistor gain without changing its operating point. This is of great importance since it enables a significant reduction in the cross-modulation and

other distortion characteristics of a gain controlled transistor amplifier.

From the curves of FIGURE 13 it will be seen that the more negative the voltage on the gate electrode the smaller the collector current for a given substrate-source current. The top six curves of FIGURE 13 are respectively for the same substrate currents as the bottom six curves. It will be noted that as the gate electrode is made more negative, the incremental change in drain current per incremental change in substrate-source current is reduced.

The channel conduction is modified by changes of the gate bias voltage and therefore the loading between the source and drain electrode changes. In the curves of FIGURE 13 the change of loading may be observed by the change in the slope of the curves. In other words the curves for a gate bias voltage of -4 exhibits a greater slope than the curves for a gate bias voltage of -6 volts. Since there is less channel resistance between the source and drain electrodes as the gate electrode voltage becomes more positive, the loading between the source and drain electrodes as seen by the NPN type transistor action is increased.

Advantage is taken of the transistor action exhibited by the substrate source and drain electrodes in the amplifier circuit of FIGURE 14 which shows a generalized form of a signal mixer stage. The transistor 280 which is of the type described in connection with FIGURES 1 and 2 has a source electrode 282, a drain electrode 284, a gate electrode 286 and a substrate electrode 288. Signals from a first signal source 290 are applied to the gate electrode 286 through a signal coupling capacitor 292 and a gate biasing resistor 294.

Signals from a second source 296 are applied to the substrate electrode 288 through a coupling capacitor 298 and a substrate bias resistor 300. The source electrode 282 is connected to a point of reference potential such as ground through a resistor 302 which is bypassed for signal frequencies by a capacitor 304. The voltage across the resistor 302 provides a self-biasing voltage which establishes the desired operating point for the gate electrode 286. An output circuit represented by the resistor 306 couples the drain electrode 284 to the positive terminal of a source of operating potential shown as a battery 308. A resistor 310 is coupled from the positive terminal in the battery 308 to the substrate electrode 288, which resistor in combination with the resistor 300 provides a voltage divider network to establish the operating point of the substrate electrode 288.

The circuit of FIGURE 14 is useful as a signal mixer for combining signals applied

Incremental

to the gate and substrate electrodes. If desired the mixer may be of the type used in superheterodyne signal receivers wherein one of the signals comprises a source of
 5 signal modulated carrier waves and the other source of signals comprises waves from a local oscillation generator. The desired output frequency signal from the heterodyne process can be selected by the
 10 use of an output circuit tuned to the desired frequency, which in superheterodyne receivers, is usually the difference between the local oscillator and signal modulated carrier wave frequencies. In like manner, the circuit may also be adapted for use as a product detector such as a synchronous detector or differential amplifier or the like.

The particular biasing voltage applied to the substrate electrode 288 is selected to be positive relative to the potential at the source electrode 282, thereby establishing a forward bias across the substrate-source rectifying junction. It will be seen that the drain electrode 284 is more positive than the substrate electrode 288 thereby providing a reverse bias across the substrate drain rectifying junction. The parameters of the circuit are such that the electrodes 282, 284 and 288 translate signals from the source
 25 296 by transistor action in the same manner as a bipolar or junction transistor circuit.

Another embodiment of the invention is shown in FIGURE 15 which is a self-oscillating frequency converter. An insulated gate field-effect transistor 312 which has a source electrode 314, a drain electrode 316, a gate electrode 318, and a substrate electrode 320 is of the general type shown and described in connection with FIGURES 1 and 2. Signal modulated carrier waves are derived from a suitable source 322 such as a signal selection circuit including a ferrite rod antenna winding 324 connected in parallel with a variable tuning capacitor 326 which tunes the signal selection circuit to the frequency of a desired carrier wave. The selected wave is applied to the gate electrode 318 through a coupling capacitor 328 and a gate bias resistor 330. The source electrode 314 is grounded and the drain electrode 316 is coupled through a tickler coil 332 and a parallel resonant circuit 334, tuned to the intermediate frequency of the receiver, to the positive terminal of the operating potential supply 336.
 55

The substrate electrode 320 is coupled through d-c blocking capacitor 338 to a tunable resonant circuit 340 which includes an inductor 342 and a variable tuning capacitor 344. A resistor 346 provides a d-c path from a substrate electrode 320 to ground.

The tunable circuit 340 determines the frequency of oscillation of the converter, and is tuned in tracking relation with the

signal selection circuit 322. Oscillation is sustained by regenerative feedback from the tickler coil 332 to the inductor 342 of the resonant circuit 340. The electrodes 316, 314 and 320 exhibit bipolar or junction transistor operation as the primary mechanism for sustaining oscillations in the circuit. Signal modulated carrier waves applied to the gate electrode 318 are combined by the nonlinear interaction in the circuit to produce heterodyne components, with the difference in frequency between the oscillator and signal modulated carrier wave corresponding to the intermediate frequency to which the circuit 334 is tuned.
 70 75 80

If desired the circuit of FIGURE 15 may be modified to feed the modulated carrier waves to the substrate electrode, and to connect the oscillator circuit between the source, gate and drain electrodes.
 85

In the circuits of FIGURES 12, 14 and 15, the substrate electrode is forward biased relative to the source electrode and reverse biased relative to the drain electrode so that the translation of signals is by transistor action. The impedance looking into the substrate electrode when it is forward biased relative to the source electrode is relatively low, thereby enabling efficient coupling to a low impedance source as is shown in FIGURE 12. If desired the gain of the circuit of FIGURE 12 may be controlled by controlling the bias applied to the gate electrode without altering the operating point of the source-substrate-drain circuit. Furthermore signals from high impedance and low impedance sources may be efficiently translated in mixers, product detectors, differential amplifiers and the like as shown in FIGURE 14 by coupling the high signal source to the gate electrode 286 and the low impedance signal source to the substrate electrode 288. Still further the gate electrode may be coupled to a high impedance source of signals of a first frequency and the substrate electrode to a low impedance source of a second and different frequency as is shown in FIGURE 10. In the latter case the substrate electrode is forward biased relative to the source electrode by a suitable bias source such as a voltage divider network across the battery 166.
 90 95 100 105 110 115

WHAT WE CLAIM IS:—

1. A signal translating circuit comprising an insulated gate field-effect transistor of the type referred to, an input circuit coupled between the source electrode and the substrate of the transistor, with said substrate either reverse biased relative to the source electrode to form therewith a rectifying junction having a capacitance or forward biased relative to the source electrode to form therewith a bipolar transistor junction,
 120 125

to the gate and substrate electrodes. If desired the mixer may be of the type used in superheterodyne signal receivers wherein one of the signals comprises a source of signal modulated carrier waves and the other source of signals comprises waves from a local oscillation generator. The desired output frequency signal from the heterodyne process can be selected by the use of an output circuit tuned to the desired frequency, which in superheterodyne receivers, is usually the difference between the local oscillator and signal modulated carrier wave frequencies. In like manner, the circuit may also be adapted for use as a product detector such as a synchronous detector or differential amplifier or the like.

The particular biasing voltage applied to the substrate electrode 288 is selected to be positive relative to the potential at the source electrode 282, thereby establishing a forward bias across the substrate-source rectifying junction. It will be seen that the drain electrode 284 is more positive than the substrate electrode 288 thereby providing a reverse bias across the substrate drain rectifying junction. The parameters of the circuit are such that the electrodes 282, 284 and 288 translate signals from the source 296 by transistor action in the same manner as a bipolar or junction transistor circuit.

Another embodiment of the invention is shown in FIGURE 15 which is a self-oscillating frequency converter. An insulated gate field-effect transistor 312 which has a source electrode 314, a drain electrode 316, a gate electrode 318, and a substrate electrode 320 is of the general type shown and described in connection with FIGURES 1 and 2. Signal modulated carrier waves are derived from a suitable source 322 such as a signal selection circuit including a ferrite rod antenna winding 324 connected in parallel with a variable tuning capacitor 326 which tunes the signal selection circuit to the frequency of a desired carrier wave. The selected wave is applied to the gate electrode 318 through a coupling capacitor 328 and a gate bias resistor 330. The source electrode 314 is grounded and the drain electrode 316 is coupled through a tickler coil 332 and a parallel resonant circuit 334, tuned to the intermediate frequency of the receiver, to the positive terminal of the operating potential supply 336.

The substrate electrode 320 is coupled through d-c blocking capacitor 338 to a tunable resonant circuit 340 which includes an inductor 342 and a variable tuning capacitor 344. A resistor 346 provides a d-c path from a substrate electrode 320 to ground.

The tunable circuit 340 determines the frequency of oscillation of the converter, and is tuned in tracking relation with the

signal selection circuit 322. Oscillation is sustained by regenerative feedback from the tickler coil 332 to the inductor 342 of the resonant circuit 340. The electrodes 316, 314 and 320 exhibit bipolar or junction transistor operation as the primary mechanism for sustaining oscillations in the circuit. Signal modulated carrier waves applied to the gate electrode 318 are combined by the nonlinear interaction in the circuit to produce heterodyne components, with the difference in frequency between the oscillator and signal modulated carrier wave corresponding to the intermediate frequency to which the circuit 334 is tuned.

If desired the circuit of FIGURE 15 may be modified to feed the modulated carrier waves to the substrate electrode, and to connect the oscillator circuit between the source, gate and drain electrodes.

In the circuits of FIGURES 12, 14 and 15, the substrate electrode is forward biased relative to the source electrode and reverse biased relative to the drain electrode so that the translation of signals is by transistor action. The impedance looking into the substrate electrode when it is forward biased relative to the source electrode is relatively low, thereby enabling efficient coupling to a low impedance source as is shown in FIGURE 12. If desired the gain of the circuit of FIGURE 12 may be controlled by controlling the bias applied to the gate electrode without altering the operating point of the source-substrate-drain circuit. Furthermore signals from high impedance and low impedance sources may be efficiently translated in mixers, product detectors, differential amplifiers and the like as shown in FIGURE 14 by coupling the high signal source to the gate electrode 286 and the low impedance signal source to the substrate electrode 288. Still further the gate electrode may be coupled to a high impedance source of signals of a first frequency and the substrate electrode to a low impedance source of a second and different frequency as is shown in FIGURE 10. In the latter case the substrate electrode is forward biased relative to the source electrode by a suitable bias source such as a voltage divider network across the battery 166.

WHAT WE CLAIM IS:—

1. A signal translating circuit comprising an insulated gate field-effect transistor of the type referred to, an input circuit coupled between the source electrode and the substrate of the transistor, with said substrate either reverse biased relative to the source electrode to form therewith a rectifying junction having a capacitance or forward biased relative to the source electrode to form therewith a bipolar transistor junction,



- a bias voltage applied to the gate electrode of the transistor to determine the operating characteristic of the transistor, and an output circuit connected between the source and drain electrodes of the transistor, the input circuit being either with or without a portion coupled between the gate and source electrodes.
2. A signal translating circuit according to Claim 1, wherein the gate electrode and the substrate are operated at the same bias potential when the substrate and source electrode are reverse biased.
3. A signal translating circuit according to Claim 1 or Claim 2, wherein the input circuit applies a first signal of one frequency between the source electrode and substrate and a second signal of a different frequency between the gate and source electrodes to provide an output signal corresponding to the combination of the first and second signals.
4. A signal translating circuit according to Claim 1, wherein said gate electrode is capacitively coupled to said substrate, said gate electrode is biased to exhibit a first bias voltage with respect to said source electrode, and said substrate is biased to exhibit a second and different bias voltage with respect to said source electrode.
5. A signal translating circuit according to Claim 1, including means connecting said gate electrode to a point of relatively fixed potential.
6. A signal translating circuit according to any preceding claim, wherein a second input circuit is coupled between said gate and source electrodes.
7. A signal translating circuit according to Claim 1, wherein said input circuit is arranged to apply signals of a first frequency, wherein a second input circuit is coupled between said gate and source electrodes and is arranged to apply signals of a second and different frequency, and wherein means providing first and second output circuits respectively for signals of said first and second frequencies is coupled to said drain electrode.
8. A signal translating circuit according to any preceding claim, wherein said output circuit includes a load impedance element and a source of direct voltage coupled between said source and drain electrodes.
9. A signal translating circuit according to Claim 1, wherein a source of signal modulated carrier waves is coupled between said gate and source electrodes, an oscillatory circuit is coupled between said substrate and source electrodes, a further circuit including a regenerative feedback means coupled to said oscillatory circuit to sustain oscillation is connected between said source and drain electrodes, and the output circuit is tuned to a frequency corresponding to the difference in frequency between the signals applied to said gate and substrate electrodes.
10. A signal translating circuit according to Claim 1, wherein said source and drain electrodes and said substrate operate as a junction transistor, and a source of gain controlling potential is coupled to said gate electrode to control the beta of said transistor.
11. A signal translating circuit substantially as herein described with reference to any one of FIGURES 4, 6, 8, 9, 10, 12, 14 and 15 of the accompanying drawings.

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