

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic timepieces, hereinafter referred to in the body of this specification as electronic watches and more specifically to electronic watches of the kind comprising a piezo-electric crystal oscillator as the time standard and a numeric time indicator actuated by signals derived from said oscillator.

The invention seeks to provide electronic watches of the kind referred to with improved, convenient, simple and quick operating means, suitable for use in small watches such as wrist watches, for correcting the numeric time indications given.

According to this invention an electronic timepiece comprises a piezo-electric crystal oscillator which produces a constant frequency output signal as a time standard, associated frequency dividers for producing from said constant frequency output signal a plurality of time signals each having a respective repetition frequency different from that of each of the others, said dividers comprising complementary MOS transistors in integrated circuit construction and there being provided for correcting the numeric indication of time given by said indicator, means on the input side of at least one divider or on the input side of each of a plurality of said dividers for selecting for input to said divider an input signal of one polarity or of the opposite polarity.

The indicator is preferably an electronic indicator of the liquid crystal or of the light emitting diode type.

The invention is illustrated in the accompanying drawings, in which:—

Figure 1 is a block diagram of one form of watch in accordance with the invention and shows, in face view, a numeric time indicator of the liquid crystal or of the light emitting diode type.

Figure 2 is a circuit diagram of the means provided, on the input side of one of the dividers 3 to 7 of Figure 1, for effecting corrections.

Figure 3 is an explanatory graphical figure showing voltage waveforms, and

Figure 4 is a simplified schematic diagram, provided for purposes of explanation and comparison, of a conventional known arrangement for effecting time indication correction in an electronic watch.

Referring to Figure 1 the time standard of the watch represented by this diagram is an oscillator 1 containing a quartz vibrator of a frequency of the order of kHz or tens of kHz. Output from this oscillator is fed to a frequency divider 2 followed by frequency dividers 3, 4, 5 6 and 7. Divider 2 produces from the output of oscillator 1 a 1 second signal and dividers 3, 4, 5, 6 and 7 produce, respectively 10 second, 1 minute, 10 minute, 1 hour and 24 hour signals. The signal output from each of the dividers 3, 4, 5, 6 and 7 is respectively associated with a driving circuit 3', 4', 5', 6' or 7' which provide, in manner known per se, appropriate signals for driving the hour, minute and second indicating sectors of a digital time indicator D.I. S1, S2, S3, S4 and S5 are switches which can be closed if it is required to correct the 1 sec, 10 sec, 1 min, 10 min and 1 hour indications of the indicator D.I.

In order to understand how correction of indicated time is effected, consider Figure 2 which is a diagram of one of the dividers 3 to 7 of Figure 1—for example of the divider 3. The other dividers 4, 5, 6 and 7 are similar. In Figure 2 the portion A is

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the input arrangement for the divider and the portion B is the divider proper, which is considered as including four MOS transistors *c, d, e, f* connected as shown. The input arrangement includes two MOS transistors *a* and *b*. Normally the gate electrodes of transistors *a* and *b* are at ground or zero voltage by connection to ground GND through a resistance R1, and the states of transistors *a* and *b* are "on" and "off" respectively. In these circumstances input signals of the appropriate polarity and applied at "INPUT" are fed to the frequency divider proper through transistor *a*. When it is required to effect correction switch S1 is closed and a positive potential V_{DD} is applied to the gate electrodes of the MOSTS *a* and *b* so that the state of *a* becomes "off" and that of *b* becomes "on". In this circumstance a polarity inverter I is effectively in circuit and the polarity of the signals reaching the divider proper is reversed. When the switch S1 is opened the transistors *a* and *b* are restored to their original conductivity states. It will therefore be seen that by repeating successive closing and opening actuations of the switch S1 such correction of indicated time as may be required can be effected.

This action is illustrated graphically in conventional manner in Figure 3. Here line 1 represents a wave form input from a preceding stage; line 2 a succession of on and off operations of the correction switch (the upper level in line 2 represents "on" or "closed" and the lower level represents "off"); line 3 represents the resulting wave form appearing at P in Figure 2; and line 4 represents the resulting output signal appearing at Q in Figure 2. By providing in similar fashion, a correction switch for each of the dividers 3 to 7 in Figure 1 any required time correction down to 1 second can be made quickly and easily even if the correction required is a large one.

Figure 4 is a simplified schematic diagram, which will be found almost self-explanatory, of conventional means for providing correction of time indication. Here FF represents one of the frequency dividers of the watch. Polarity of the input thereto is reversed by means of the switch St which, in one position, causes the input to be applied to FF with one polarity and in the other position reverses the input polarity. As will be seen the switch St in Figure 4 for changing over from ground potential to potential V_{DD} is a change over switch, whereas in Figure 2 the switch used is a simple on and off switch which lends itself much better to miniaturisation without loss of reliability and enables full advantage to be taken of the miniaturisation possibilities of integrated circuit MOS construction. By using MOS integrated circuit construction

in accordance with known principles in the construction of an embodiment as represented in Figure 2, relatively great compactness and small size together with a high reliability are obtainable, for the increase in the size of the MOS integrated circuit construction due to the necessity of providing the MOS transmission gates in part A of Figure 2 is negligibly small. As regards miniaturisation the arrangement of Figure 2 is much better than that of Figure 4 which, with its need for external terminals for connection of external resistances involves substantially more occupation of space.

The invention, and especially the preferred embodiment of Figure 2 which uses only simple switches and a minimum of extra circuit elements (resistances) is well adapted for use in small timepieces such as wristwatches.

WHAT WE CLAIM IS:—

1. An electronic timepiece comprising a piezo-electric crystal oscillator which produces a constant frequency output signal as a time standard, associated frequency dividers for producing from said constant frequency output signal a plurality of time signals each having a respective predetermined repetition frequency different from that of each of the others, a numeric time indicator and means for utilising said time signals to drive the appropriate parts of said numeric time indicator, said dividers being constituted by complementary MOS transistors in integrated circuit construction and there being provided for correcting the numeric indication of time given by said indicator means on the input side of at least one divider or on the input side of each of a plurality of said dividers, for selecting for input to said divider an input signal of one polarity or of the opposite polarity.

2. A timepiece as claimed in claim 1 wherein the means for correcting numeric indication of time include switch controlled transmission gates through one or other of which input is applied to the appropriate divider.

3. A timepiece as claimed in claim 2 in which the transmission gates are of the MOS transistor type integrated with the frequency dividing MOS transistors in integrated circuit construction.

4. A timepiece as claimed in claim 2 or 3 wherein the switch control of the transmission gates is effected by changing the potential applied to the gate electrodes thereof to reverse the conductivity states thereof so that in one position of the switch one transmission gate is conductive and the other is not while in the other position of the switch said one transmission gate is cut off and the said other is not, a polarity inverter being provided in effective series with one of the said transmission gates.



the input arrangement for the divider and the portion B is the divider proper, which is considered as including four MOS transistors *c, d, e, f* connected as shown. The input arrangement includes two MOS transistors *a* and *b*. Normally the gate electrodes of transistors *a* and *b* are at ground or zero voltage by connection to ground GND through a resistance R1, and the states of transistors *a* and *b* are "on" and "off" respectively. In these circumstances input signals of the appropriate polarity and applied at "INPUT" are fed to the frequency divider proper through transistor *a*. When it is required to effect correction switch S1 is closed and a positive potential V_{DD} is applied to the gate electrodes of the MOSTS *a* and *b* so that the state of *a* becomes "off" and that of *b* becomes "on". In this circumstance a polarity inverter I is effectively in circuit and the polarity of the signals reaching the divider proper is reversed. When the switch S1 is opened the transistors *a* and *b* are restored to their original conductivity states. It will therefore be seen that by repeating successive closing and opening actuations of the switch S1 such correction of indicated time as may be required can be effected.

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in accordance with known principles in the construction of an embodiment as represented in Figure 2, relatively great compactness and small size together with a high reliability are obtainable, for the increase in the size of the MOS integrated circuit construction due to the necessity of providing the MOS transmission gates in part A of Figure 2 is negligibly small. As regards miniaturisation the arrangement of Figure 2 is much better than that of Figure 4 which, with its need for external terminals for connection of external resistances involves substantially more occupation of space.

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2. A timepiece as claimed in claim 1 wherein the means for correcting numeric indication of time include switch controlled transmission gates through one or other of which input is applied to the appropriate divider.
3. A timepiece as claimed in claim 2 in which the transmission gates are of the MOS transistor type integrated with the frequency dividing MOS transistors in integrated circuit construction.
4. A timepiece as claimed in claim 2 or 3 wherein the switch control of the transmission gates is effected by changing the potential applied to the gate electrodes thereof to reverse the conductivity states thereof so that in one position of the switch one transmission gate is conductive and the other is not while in the other position of the switch said one transmission gate is cut off and the said other is not, a polarity inverter being provided in effective series with one of the said transmission gates.



5. A timepiece as claimed in any of the preceding claims wherein the numeric indicator is an electronic indicator of the liquid crystal or of the light emitting diode type.

- 5 6. Timepieces substantially as herein described with reference to Figures 1, 2 and 3 of the accompanying drawings.

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