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ABSTRACT OF THE DISCLOSURE

The present invention provides a polishing pad used for planarizing inter layer dielectrics and the like by CMP (chemical mechanical polishing) in the manufacturing process of a semiconductor device, a method of producing the polishing pad and a method of producing a semiconductor device by using the polishing pad. The present invention relates to a semiconductor wafer polishing pad having grooves in a polishing surface and formed from a foamed polyurethane, wherein a processed surface of the groove comprising a side surface and a bottom surface has a surface roughness Ra of not more than 10.