CLAIMS

What is claimed is:

1. A method

performed using an electronic circuit comprising at least a DC-DC converter, the method comprising:

establishing a sleep signal relating to powering down ~~an~~ another electronic circuit into a sleep mode;

~~turning off the DC-DC converter in dependence upon the establishment of the sleep signal;~~

establishing a synthesized clock counter to count the number of synthesized clock cycles between the moment the sleep signal is raised and the moment the DC-DC converter is turned off;

retaining the value of this synthesized clock counter during the sleep mode;

turning off the DC-DC converter in dependence upon the establishment of the sleep signal;

subtracting a time value established in dependence upon this retained synthesized clock counter value from a predetermined delay relating to when to wake the electronic circuit out of the sleep mode; whereby

the DC-DC converter is turned-off upon a predetermined edge of a low frequency clock forming part of the electronic circuit and turned-on upon another predetermined edge of the low frequency clock;

the synthesized clock cycles are of a high frequency phase locked loop (PLL) clock signal generated by a PLL based upon the low frequency clock signal; and

at least one of the sleep duration of the electronic circuits and a wireless radio comprising the electronic circuits is now independent of the point within the period of the crystal clock cycle when the sleep signal is raised.

~~2. The method according to claim 1, wherein~~

~~the DC-DC converter is turned-off upon a predetermined edge of a low frequency clock forming part of the electronic circuit.~~

2~~3~~. The method according to claim 1~~2~~, wherein

the low frequency clock is at least one of operating at a frequency of 32kHz and is generated by a crystal oscillator.