



162162



G00002

- 25 -

ABSTRACT

A timing generating circuit with low power consumption and a small layout area, a display apparatus including the timing generating circuit as one peripheral driving circuit, and a portable terminal including the display apparatus as a display output section are provided. In the timing generating circuit, which is formed on an insulating substrate and generates output pulses SRFFlout to SRFFnout having different frequencies based on a master clock MCK, a clock generating circuit (11) generates an operating clock having a lower frequency than the master clock MCK frequency. Then, a counter section (12) operates based on this operating clock and successively outputs shifted pulses S/Rlout to S/Rmount from shift registers (121-1) to (121-m). An output pulse generating section (13) generates output pulses SFlout to SFnout based on combinations of the shifted pulses S/Rlout to S/Rmount.