CLAIMS

1. A memory system comprising:

a plurality of memory packages coupled by a common bus and arranged in groups, each group including a pair of memory packages facing each other, and each memory package including a plurality of memory chips;

an on-die termination (ODT) circuit disposed in all the memory packages and configured to suppress reflection of a signal; and

a controller configured to perform writing or reading of data to or from a memory chip of a designated memory package and to perform on/off control of the ODT circuit of the memory package through the common bus,

wherein the controller maintains an ODT start condition for turning on the ODT circuit set by a 2-bit information signal defined by a periodic signal of at least two cycles, and turns on the ODT circuit when an asserted state of a chip enable signal CEn acquired using the periodic signal is included in a pattern of the ODT start condition.

2. A memory system comprising:

a plurality of memory packages coupled by a common bus and arranged in groups, each group including a pair of memory packages facing each other, and each memory package including a plurality of memory chips;

an on-die termination (ODT) circuit disposed in all the memory chips and configured to suppress reflection of a signal; and

a controller configured to perform writing or reading of data to or from a memory chip of a designated memory package and to perform on/off control of the ODT circuit of the memory chip through the common bus,

wherein the controller maintains an ODT start condition for turning on the ODT circuit set by a 2-bit information signal defined by a periodic signal of at least two cycles, and turns on the ODT circuit when an asserted state of a chip enable signal CEn acquired using the periodic signal is included in a pattern of the ODT start condition.

3. The memory system according to claim 1 or 2, wherein the 2-bit information signal stored in the controller configures a truth value that defines:

after commencement of assertion of the chip enable signal CEn to drive a memory chip of the selected memory package, for which the controller performs data writing or data reading, a first ODT start condition for turning on the ODT circuit to set a target ODT to ON when the asserted state is detected twice in succession and if assertion is detected continuously based on the periodic signal; and

after commencement of assertion of the chip enable signal CEn to drive a memory chip of the memory package not

selected by the controller, a second ODT start condition for turning on the ODT circuit to set a non-target ODT to ON if the asserted state is detected firstly and a negated state is detected secondly based on the periodic signal.

4. The memory system according to claim 1 or 2, wherein the periodic signal has a period of at least two cycles and is applied to a head side of an ODT enable signal ODTEN.

5. The memory system according to claim 1 or 2, wherein the periodic signal has a period of at least two cycles and is applied to a head side of a write enable signal WEn.

6. The memory system according to claim 3, wherein the ODT circuit is ON/OFF-controlled by the first ODT start condition and the second ODT start condition based on the asserted state of the chip enable signal CEn acquired when a target ODT flag is set in all the memory chips and a non-target ODT flag is set in one memory chip in each of the memory packages.

7. The memory system according to claim 1 or 2, wherein the pair of memory packages are mounted on mounting surfaces of both front and back surfaces of a circuit board so as to face each other with the circuit board interposed

therebetween.

8. The memory system according to claim 1 or 2, wherein one cycle from a first rising edge to a second rising edge of the periodic signal has a time width of four times a switching timing of a write enable signal WEn.

9. The memory system according to claim 1, wherein a memory cell included in the memory package is a stacked NAND flash memory.

10. A control method for a memory system including: a plurality of memory packages coupled by a common bus and arranged in groups, each group including a pair of memory packages facing each other, and each memory package including a plurality of memory chips; an on-die termination (ODT) circuit disposed in all the memory packages and configured to suppress reflection of a signal; and a controller configured to perform writing or reading of data to or from a memory chip of a designated memory package, and to perform on/off control of the ODT circuit with respect to the designated memory package through the common bus, the method comprising:

a first ODT start condition and a second ODT start condition set by a 2-bit information signal defined by a periodic signal of at least two cycles applied to a head of a control signal,

as the first ODT start condition,

after commencement of assertion of the chip enable signal CEn to drive a memory chip of the selected memory package, for which the controller performs data writing or data reading, turning on the ODT circuit to set a target ODT to ON when the asserted state is detected twice in succession and if assertion is detected continuously based on the periodic signal; and

as the second ODT start condition,

after commencement of assertion of the chip enable signal CEn to drive a memory chip of the memory package not selected by the controller, turning on the ODT circuit to set a non-target ODT to ON if the asserted state is detected firstly and a negated state is detected secondly based on the periodic signal.

11. A control method of a memory system including: a plurality of memory packages coupled by a common bus and arranged in groups, each group including a pair of memory packages facing each other, and each memory package including a plurality of memory chips; an on-die termination (ODT) circuit disposed in all the memory chips and configured to suppress reflection of a signal; and a controller configured to perform writing or reading of data to or from a designated memory chip and to perform on/off control of the ODT circuit through the common bus, the method comprising:

a first ODT start condition and a second ODT start condition set by a 2-bit information signal defined by a periodic signal of at least two cycles applied to a head of a control signal,

as the first ODT start condition,

after commencement of assertion of the chip enable signal CEn to drive a memory chip of the selected memory package, for which the controller performs data writing or data reading, turning on the ODT circuit to set a target ODT to ON when the asserted state is detected twice in succession and if assertion is detected continuously based on the periodic signal; and

as the second ODT start condition,

after commencement of assertion of the chip enable signal CEn to drive a memory chip of the memory package not selected by the controller, turning on the ODT circuit to set a non-target ODT to ON if the asserted state is detected firstly and a negated state is detected secondly based on the periodic signal.

12. A program causing a hardware processor included in the controller to function as each unit included in the memory system according to claim 1 or 2.