"Resin encapsulated semiconductor device"

This invention relates to a resin-encapsulated type semiconductor device and specifically to a resin encapsulated field effect transistor.

When a field effect transistor for high frequency use, such as an insulated gate type field effect transistor (hereinafter called a "MOSFET"), is employed in a high frequency circuit, it is necessary to ground the source electrode for a.c. signals via a capacitor or the like. If this grounding is not complete, operation in the high frequency circuit becomes unstable. Incomplete grounding also results in the drawback in a dual gate type MOSFET that sufficient gain reduction cannot be obtained by a gain control voltage applied to one gate electrode. When the control voltage of one gate electrode is changed to a predetermined voltage in order to reduce the power gain, the reduction in level of the power gain with respect to a signal applied to the other gate electrode (hereinafter called "maximum gain reduction") is deficient.

Referring now to Figures 1A and 1B of the accompanying drawings, which for explanatory purposes show a MOSFET of a flat package type, it can be seen that a MOSFET element 1 is fitted to one lead S of the leads S, D, G_1, G_2, which extend horizontally thereby forming a source terminal. The electrodes of the element and the leads are wire-bonded together and the element as a whole is encapsulated in a moulded resin body 2. Grounding of the case is not possible unlike a metallic case. Grounding must therefore be made solely by use of the source terminal (lead) S. It has been found, however, that the effect of lead inductance is not negligible when grounding is made in such a way. For this reason, in comparison with a MOSFET having a metallic case, the resin-encapsulated flat package type MOSFET has inferior maximum gain reduction and stability in a high frequency band, especially in or above the UHF band.

It is therefore an object of the present invention to improve the stability of a resin-encapsulated FET.

It is a further object of the present invention to improve the maximum gain reduction of a resin encapsulated FET.

According to the invention there is provided a resin-encapsulated semiconductor device suitable for use in a high frequency circuit comprising a field effect transistor having source, drain and gate electrodes, a plurality of leads connected to said electrodes, a conductor plate which in use of the device provides grounding contact for the device and a resin body integrally encapsulating said field effect transistor and a portion of each of said leads, wherein said source electrode is electrically connected to said conductor plate via one of said leads and at least a part of a surface of said conductor plate to which said source electrode is not connected is exposed outside said resin body and at least some of the remaining surface areas of said conductor plate are covered by said resin body, said exposed surface part providing said grounding contact in use.

The invention further provides such a semiconductor device mounted in a circuit board with the conductor plate in grounding contact with a conductor of said circuit board.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings, in which:-

Figure 1A is a plan view of the resin-encapsulated flat package type MOSFET described above;

Figure 1B is a sectional view of the MOSFET of Figure 1A taken along line A-A' of Figure 1A;

Figure 2 is a sectional view of a first resin encapsulated flat package type MOSFET embodying the present invention;

Figure 3 is a sectional view of a second resin encapsulated flat package type MOSFET embodying the present invention;

Figures 4 to 11 show the fabrication steps of the MOSFET shown in Figure 2, wherein:

Figure 4 is a sectional view of the pellet;

Figure 5 is a plan view of the lead frame;

Figure 6 is a perspective view of the substrate;

Figures 7 to 10 are sectional views of the lead frame during assembly; and

Figure 11 is a perspective view of the MOSFET after assembly;

Figure 12 is a plan view of the lead frame at one stage in the process of fabricating the MOSFET shown in Figure 3;

Figure 13 is a sectional view of the lead frame at one stage in the process of fabricating the MOSFET shown in Figure 3;

Figure 14 is a plan view of the MOSFET of Figure 2 connected to the wiring substrate; and

Figure 15 is a sectional view taken along line C - C' of Figure 14.

Figure 2 is a sectional view corresponding to the B - B' direction of Figure 1A. The MOSFET element 1 is fitted with a lead S serving as a source terminal. A lead G_2 serves as the second gate terminal. The lead S is connected to a conductor plate 3 via an intermediate plate 4. An encapsulating

resin body 2 integrally seals the MOSFET, leads and intermediate plate. As shown in this drawing, the bottom surface of the conductor plate 3 is exposed outside the resin body 2.

Figures 4 to 11 show the fabrication steps of the MOSFET of Figure 2. Figure 4 is a section of the two-gate type MOSFET element. n^+-type diffusion layers 6 and 7 to serve as source and drain are formed on a p-type Si substrate 5 and gates G_1 and G_2 are formed on the surface of the element between the n^+-type diffusion layers 6 and 7 and insulated from the substrate 5 by an insulation film (SiO_2) 8. Electrodes S and D are disposed on the source and drain, respectively.

Figure 5 shows the lead frame of the flat package type to which the MOSFET element is fitted. The lead frame consists of leads corresponding to the aforementioned source S, drain D and gates G_1 and G_2, and of a dam 9 for stopping the flow of the resin during molding. The inner end of the lead S functioning as the source terminal also serves as an element-fitting portion 10.

Figure 6 shows the shape of the conductor plate 3. The intermediate plate 4 is either formed integrally with the conductor plate 3 or connected

to the conductor plate by spot-welding or the like.

The lead frame and conductor plate are combined with each other as shown in Figure 7 and are connected to each other via the intermediate plate 4 as shown in Figure 8. This connection is carried out by welding, brazing or caulking. As shown in Figure 9, the MOSFET element 1 is then fitted onto the lead frame and the electrodes of the element are connected to the corresponding leads by wire-bonding. In carrying out this wire-bonding, it is necessary to interpose a jig 11 or the like between the conductor plate 3 and the other leads G_1, G_2, D that are floating above the conductor plate 3.

Figure 10 shows the moulding of the resin encapsulation by packing the lead frame into upper and lower molds 12,13. Figure 11 shows the appearance of the MOSFET after molding.

Figure 3 shows a further preferred embodiment of the present invention in which the lead S to be connected to the source of the element is integral with the conductor plate. In this case, it is advisable to employ a lead frame having the shape shown in Figure 12. In Figure 12, the lead S to be connected to the source has a conductor plate

14 which extends fully within the dam 9 with suitable gaps between it and the other leads G_1, G_2, D. This conductor plate 14 and the lead S are formed integrally. A part 15 of each of the other leads such as G_2 for example, is bent upwardly as depicted in Figure 13. After the MOSFET element 1 and the leads are wire-bonded as shown in this drawing, resin encapsulation is used to give the construction shown in Figure 3, in which the lower face of the plate 14 is exposed outside the resin.

In the embodiment of Figure 3, the distance from the main body of the pellet (MOSFET element) 1 to the source lead terminal is short and the grounding effect can be increased.

In actually fitting a resin-encapsulated flat package type MOSFET in accordance with the present invention to a printed circuit board or the like, a grounding effect virtually identical to that of the device with a metallic case can be obtained by directly grounding the lower case portion (conductor plate) as shown in Figures 14 and 15.

Figures 14 and 15 show a MOSFET element of the present invention in its connected state which is resin molded onto the printed circuit board.

The leads of the source, drain and gate are shown connected electrically via solder 21 to the metal wires 22 on the printed circuit board having a metal foil such as a copper foil arranged in a predetermined wiring pattern 22 on the surface of the insulation plate 20. The conductor plate 3 is directly connected to the metal wires 22.

The stability and maximum gain reduction of a resin-encapsulated flat package type MOSFET in a high frequency circuit can thus be improved markedly.

The maximum gain reduction possible in a resin-encapsulated flat package type FET of the present invention is increased by about 5 to 7dB when compared with that of the maximum gain reduction of the resin-encapsulated flat package type FET shown in Figures 1A and 1B. Thus, it is possible to obtain good reduction of the power gain.

The present invention is not restricted to the above-described embodiments. For example, the MOSFET may be not of the two-gate type but of the one-gate type. In the latter case, the number of leads is three. The present invention can also be applied to a junction-type FET in the same way as in the above-described embodiments. In the MOSFET shown in Figure 2, the source lead S may be connected

directly to the conductor plate 4 without using the intermediate plate 4.

The present invention provides a remarkable effect in a FET to be used in a high frequency circuit in or higher than the UHF band. Especially good effects can be obtained in a FET used in the tuner of a television receiver.

CLAIMS

1. A resin-encapsulated semiconductor device suitable for use in a high frequency circuit comprising a field effect transistor having source, drain and gate electrodes, a plurality of leads connected to said electrodes, a conductor plate which in use of the device provides grounding contact for the device and a resin body integrally encapsulating said field effect transistor and a portion of each of said leads, wherein said source electrode is electrically connected to said conductor plate via one of said leads and wherein a surface region of said conductor plate to which said source electrode is not directly connected is exposed outside said resin body while at least some other surface regions of said conductor plate are covered by said resin body, said exposed surface region providing said grounding contact in use.

2. A device according to claim 1 wherein said conductor plate is integral with said lead connected to said source electrode.

3. A device according to claim 2 wherein the ends closest to said field effect transistor of said leads other than the lead integral with said conductor plate are located spaced from the conductor plate and on the same side of the conductor plate as the transistor.

4. A device according to any one of the preceding claims wherein the transistor is mounted directly or indirectly on the conductor plate, the said electrodes being on a face of the transistor remote from the conductor plate.

5. A device according to claim 4 wherein the transistor is mounted on the lead connected to the source electrode, which lead is mounted on the conductor plate.

6. A device according to any one of the preceding claims wherein said plurality of leads connected to said source, gate and drain electrodes, protrude outwardly from said resin body.

7. A device according to any one of the preceding claims wherein said resin body has a cylindrical shape.

8. A resin encapsulated semiconductor device according to any one of the preceding claims wherein a wiring substrate having a metallic wiring pattern on the surface thereof is connected to said leads by solder.

9. A resin encapsulated semiconductor device substantially as herein described with reference to and as shown in Figures 2 and 4 to 11 or Figures 3, 12 and 13 of the accompanying drawings.

10. A resin encapsulated semiconductor device according to any one of the preceding claims mounted on a circuit board with the conductor plate in grounding contact with a conductor of said circuit board.

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