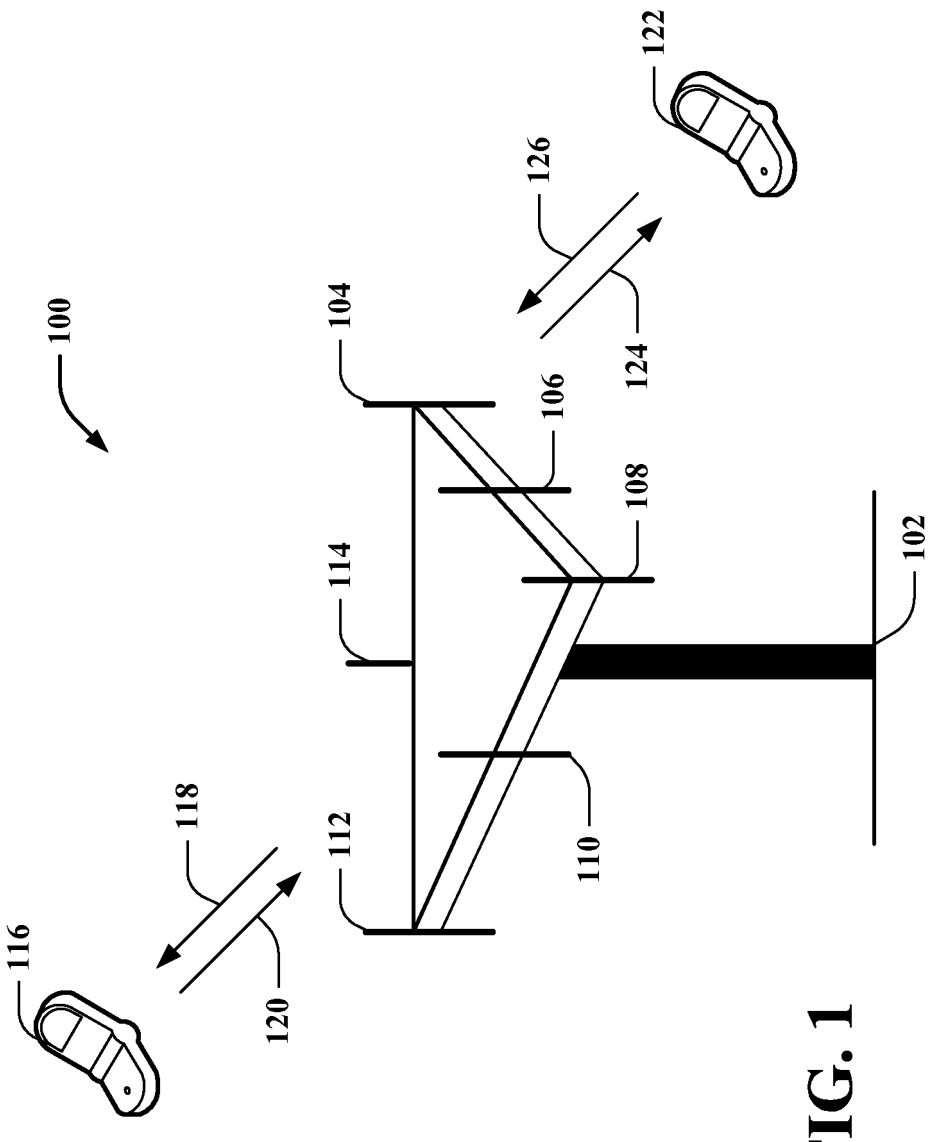


FIG. 1

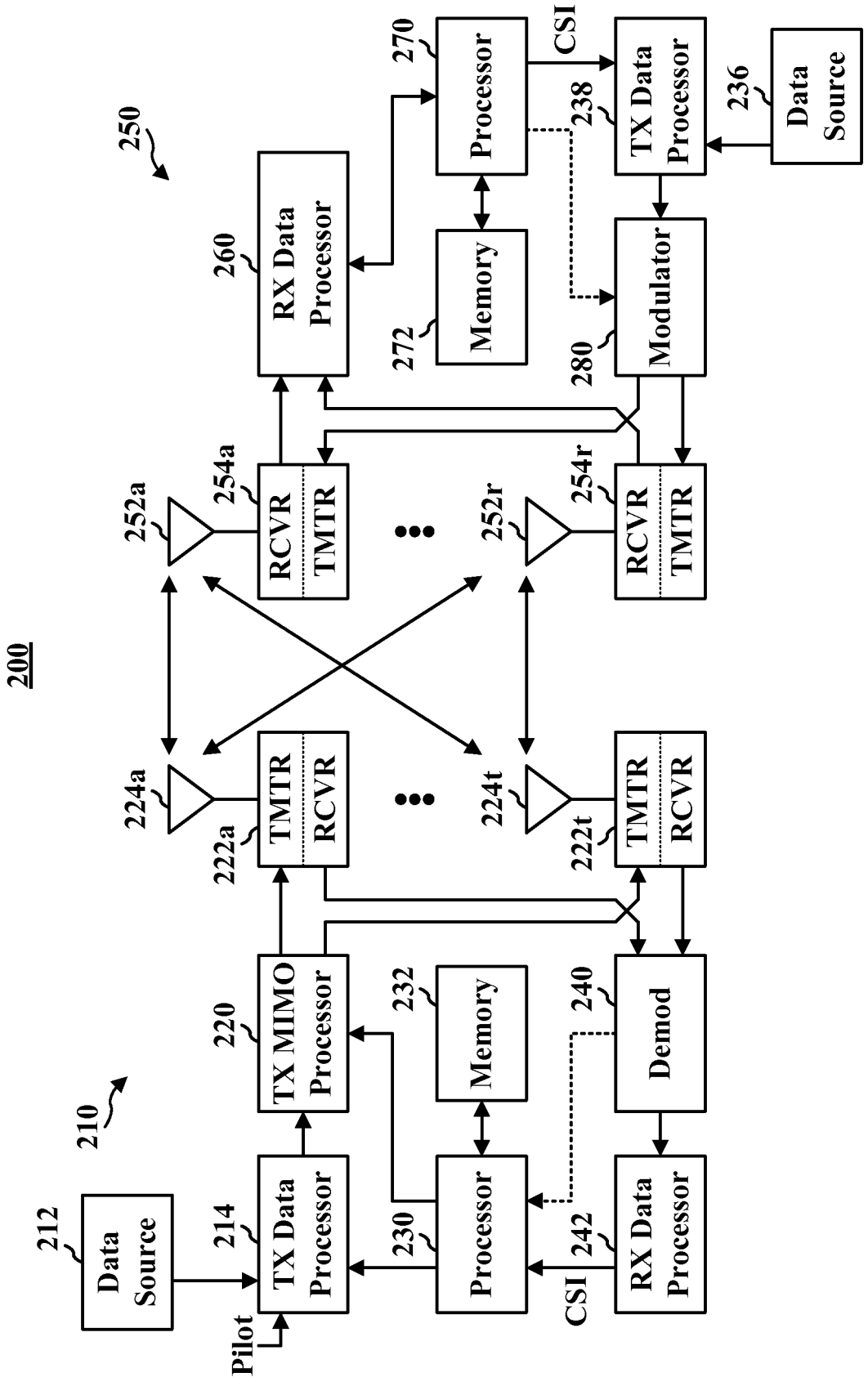

200
210
212
Data Source
214
TX Data Processor
Pilot
220
TX MIMO Processor
222a
TMTR
RCVR
224a
252a
254a
RCVR
TMTR
230
Processor
232
Memory
240
Demod
242
RX Data Processor
CSI
250
260
RX Data Processor
270
Processor
CSI
272
Memory
280
Modulator
238
TX Data Processor
236
Data Source
224t
222t
TMTR
RCVR
252r
254r
RCVR
TMTR

FIG. 2

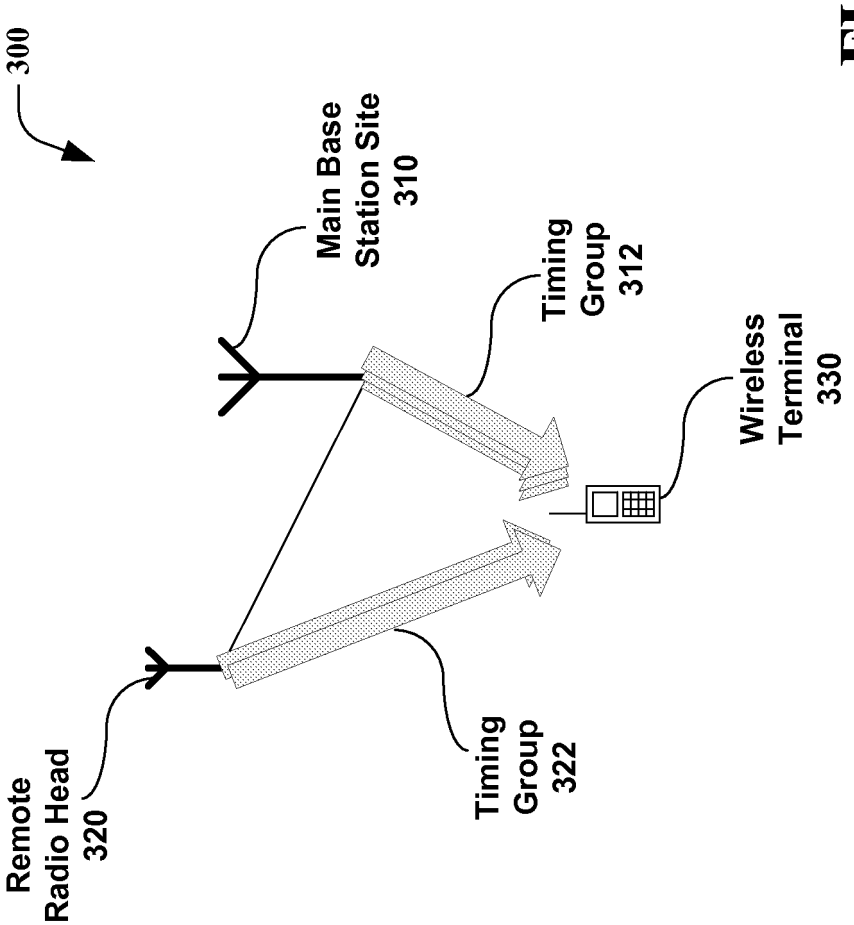

300
Main Base Station Site 310
Timing Group 312
Wireless Terminal 330
Remote Radio Head 320
Timing Group 322

FIG. 3

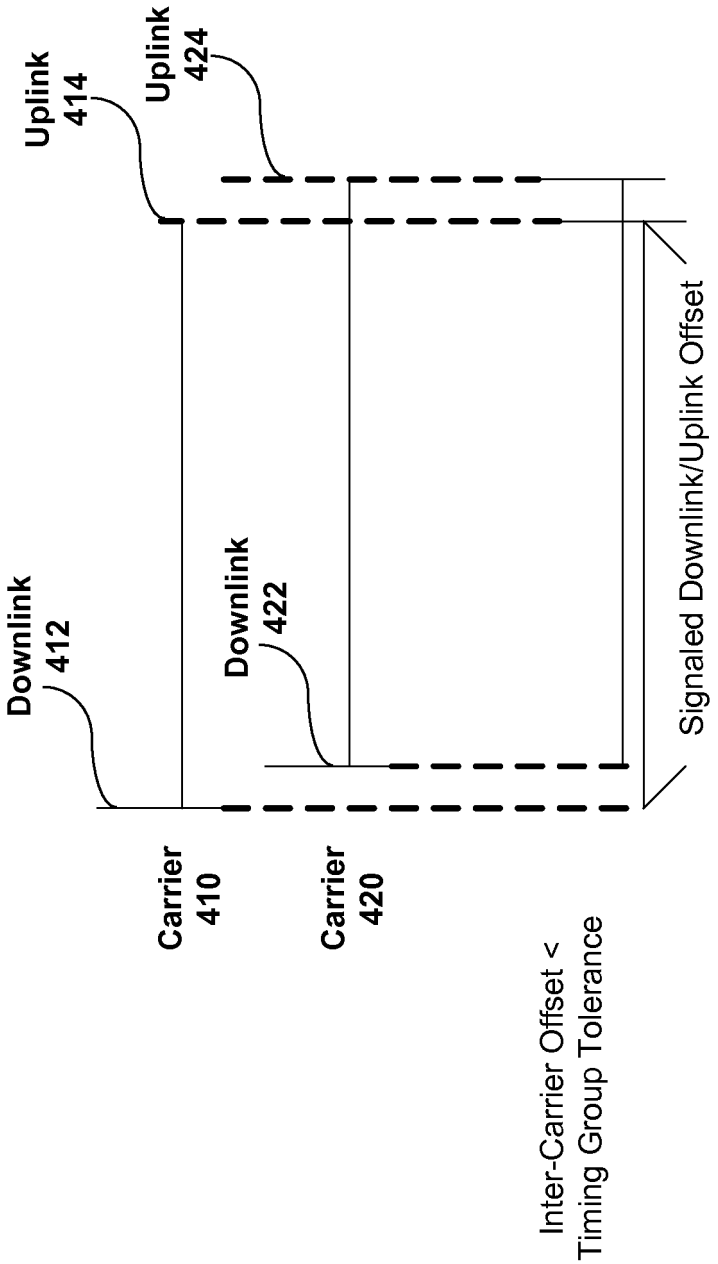

Uplink 414
Uplink 424
Downlink 412
Downlink 422
Signaled Downlink/Uplink Offset
Carrier 410
Carrier 420
Inter-Carrier Offset < Timing Group Tolerance

FIG. 4

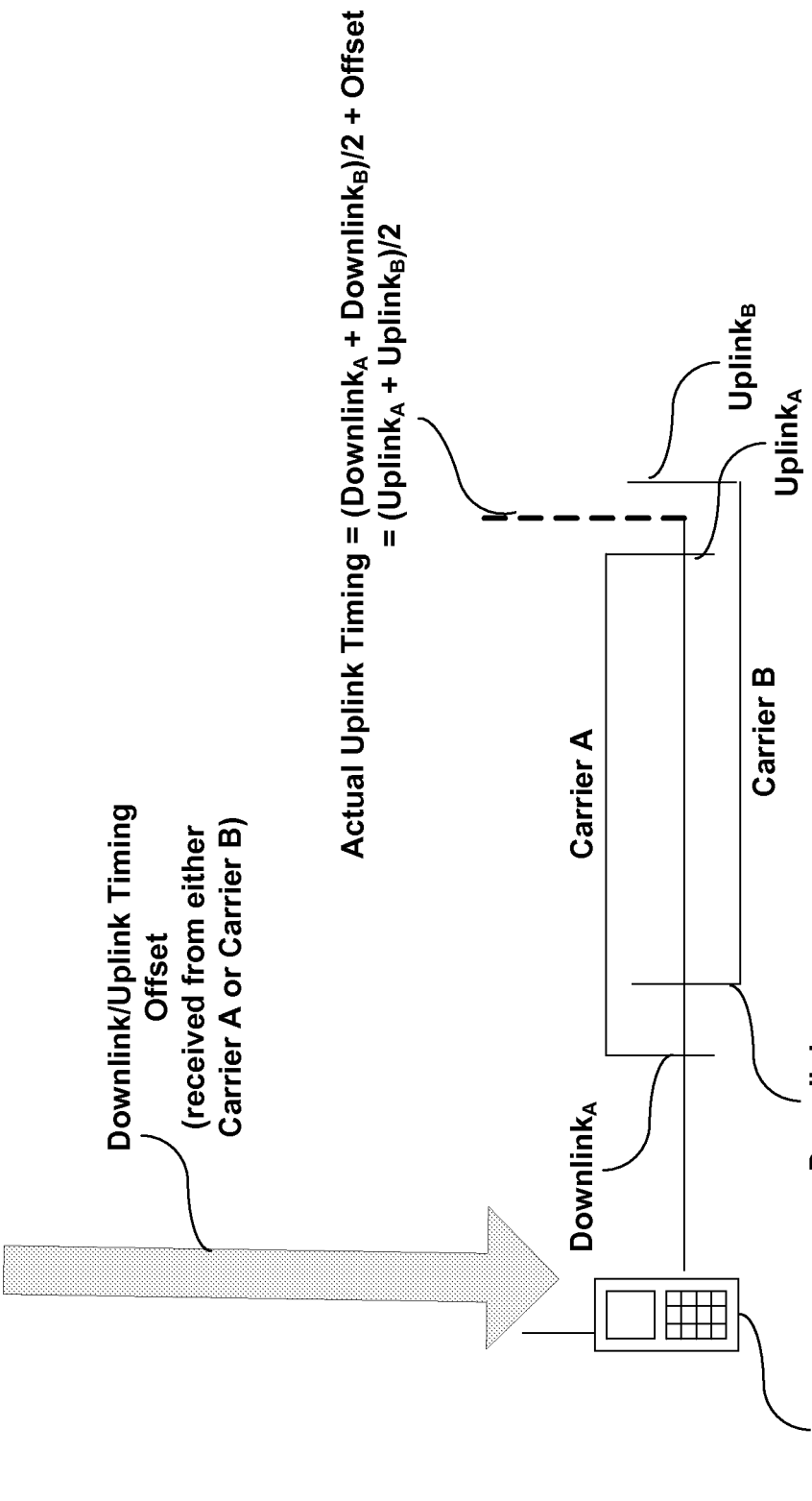

Downlink/Uplink Timing Offset (received from either Carrier A or Carrier B)
Actual Uplink Timing = (Downlink$_A$ + Downlink$_B$)/2 + Offset = (Uplink$_A$ + Uplink$_B$)/2
Carrier A
Carrier B
Downlink$_A$
Downlink$_B$
Uplink$_A$
Uplink$_B$
Wireless Terminal 510

FIG. 5

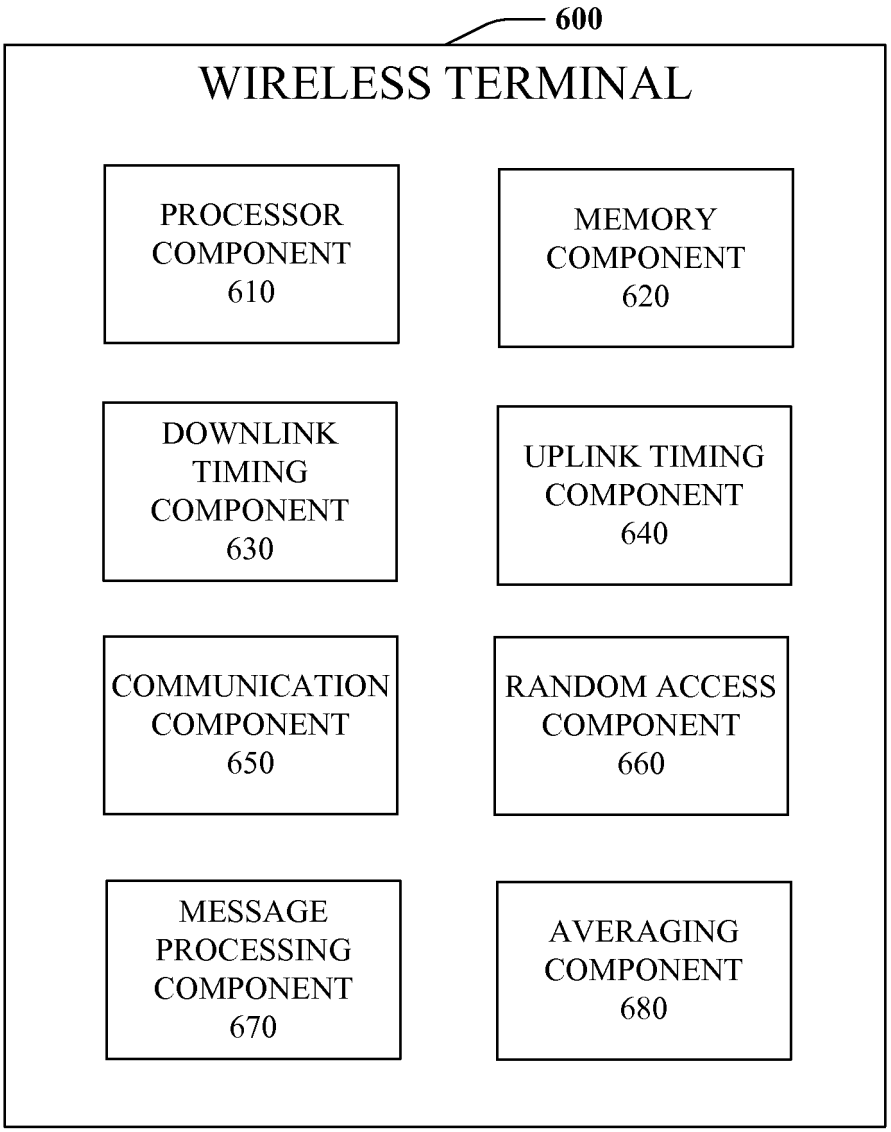

600
WIRELESS TERMINAL
PROCESSOR COMPONENT 610
MEMORY COMPONENT 620
DOWNLINK TIMING COMPONENT 630
UPLINK TIMING COMPONENT 640
COMMUNICATION COMPONENT 650
RANDOM ACCESS COMPONENT 660
MESSAGE PROCESSING COMPONENT 670
AVERAGING COMPONENT 680

FIG. 6

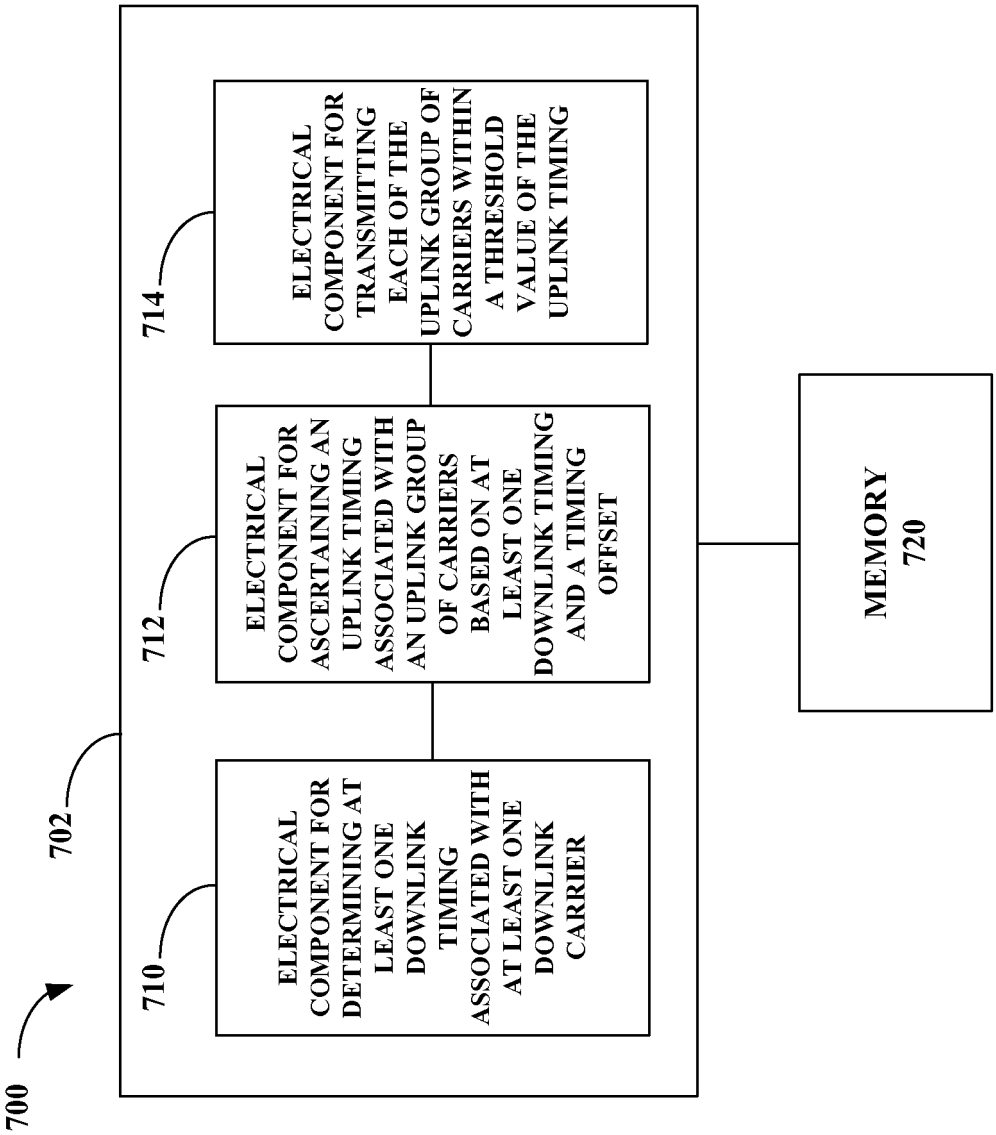

700
702
710
ELECTRICAL COMPONENT FOR DETERMINING AT LEAST ONE DOWNLINK TIMING ASSOCIATED WITH AT LEAST ONE DOWNLINK CARRIER
712
ELECTRICAL COMPONENT FOR ASCERTAINING AN UPLINK TIMING ASSOCIATED WITH AN UPLINK GROUP OF CARRIERS BASED ON AT LEAST ONE DOWNLINK TIMING AND A TIMING OFFSET
714
ELECTRICAL COMPONENT FOR TRANSMITTING EACH OF THE UPLINK GROUP OF CARRIERS WITHIN A THRESHOLD VALUE OF THE UPLINK TIMING
MEMORY 720

FIG. 7

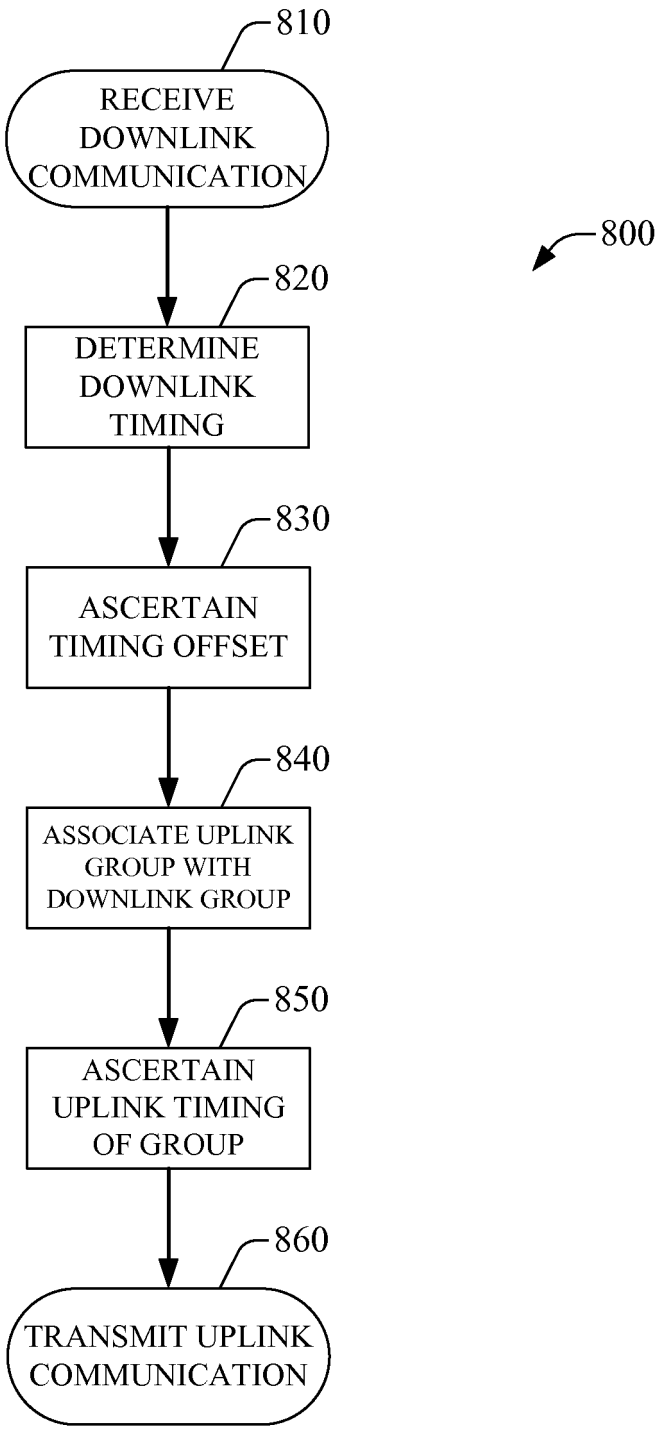

810
RECEIVE DOWNLINK COMMUNICATION
800
820
DETERMINE DOWNLINK TIMING
830
ASCERTAIN TIMING OFFSET
840
ASSOCIATE UPLINK GROUP WITH DOWNLINK GROUP
850
ASCERTAIN UPLINK TIMING OF GROUP
860
TRANSMIT UPLINK COMMUNICATION

FIG. 8

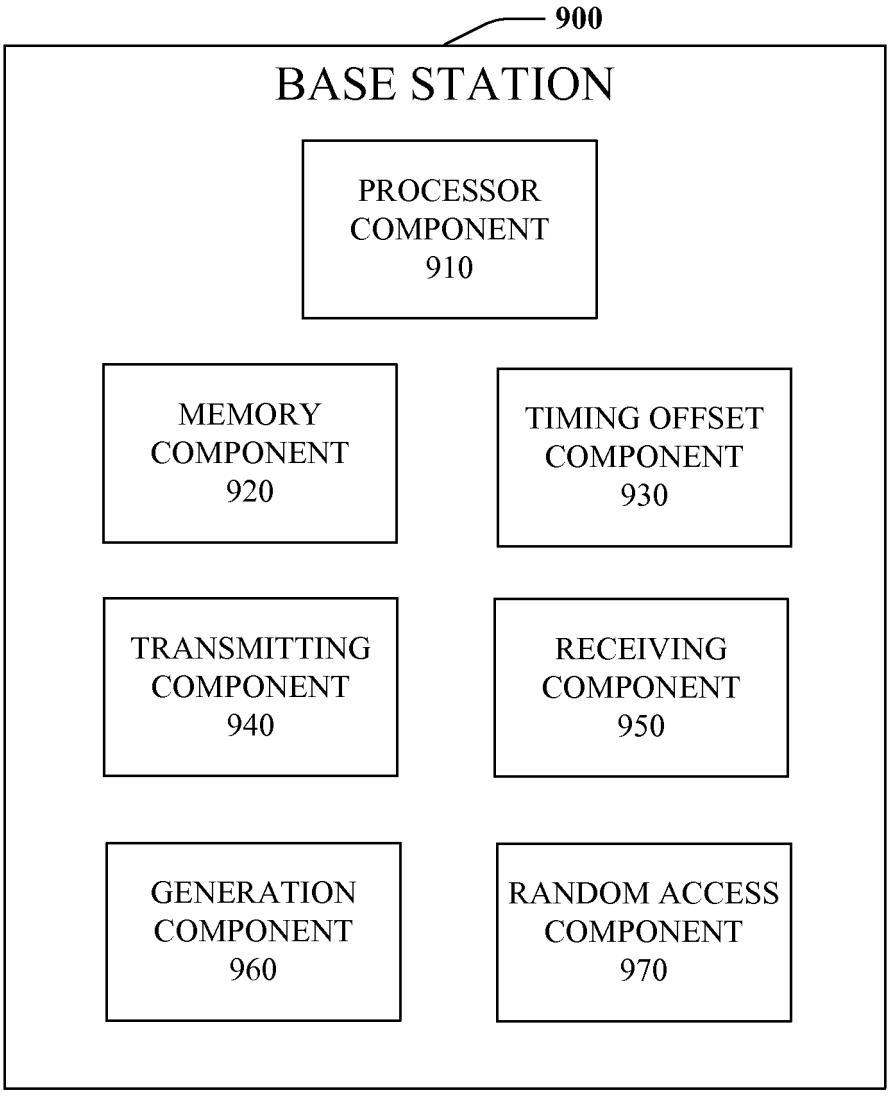

900
BASE STATION
PROCESSOR COMPONENT 910
MEMORY COMPONENT 920
TIMING OFFSET COMPONENT 930
TRANSMITTING COMPONENT 940
RECEIVING COMPONENT 950
GENERATION COMPONENT 960
RANDOM ACCESS COMPONENT 970

FIG. 9

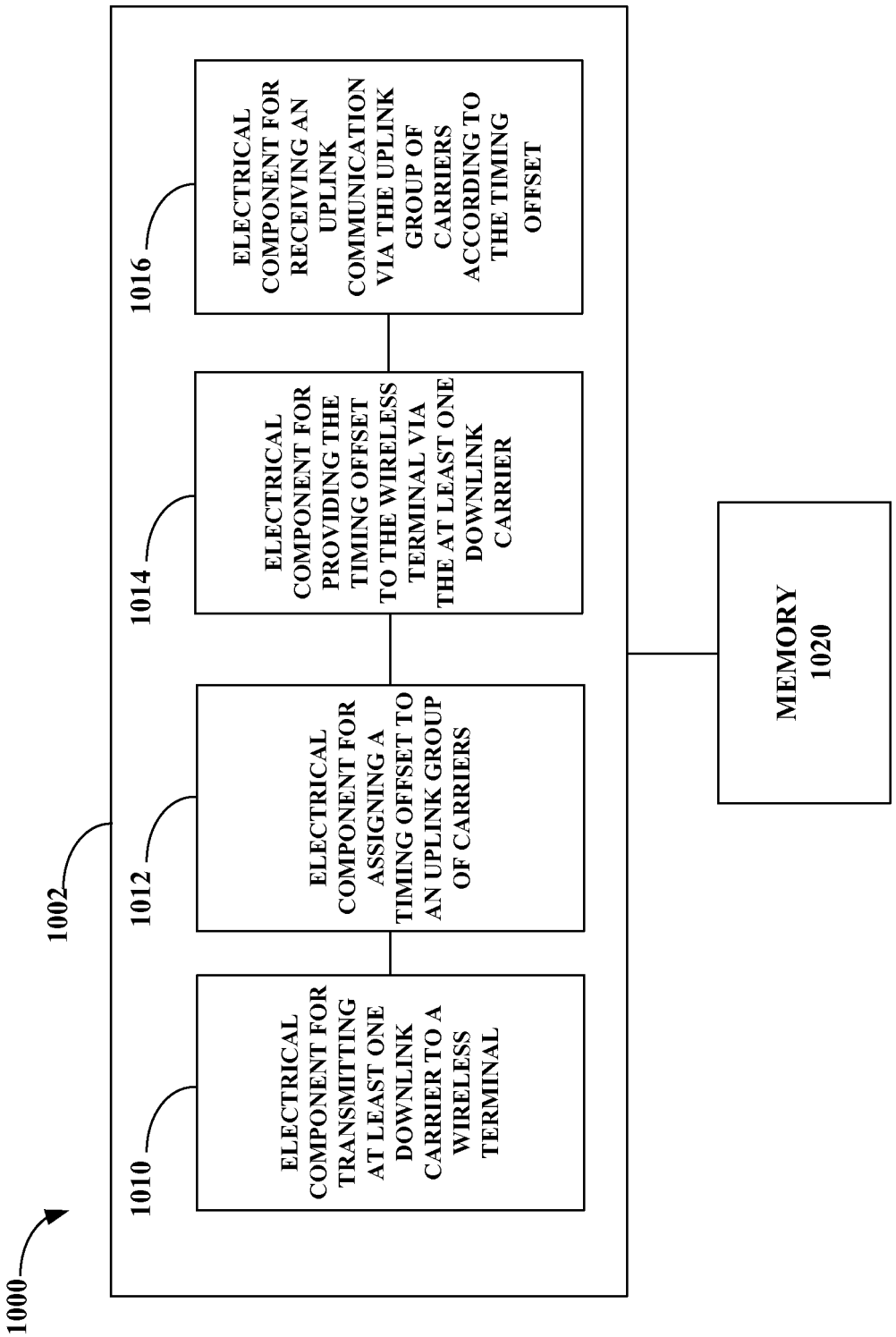

1000
1002
1010
ELECTRICAL COMPONENT FOR TRANSMITTING AT LEAST ONE DOWNLINK CARRIER TO A WIRELESS TERMINAL
1012
ELECTRICAL COMPONENT FOR ASSIGNING A TIMING OFFSET TO AN UPLINK GROUP OF CARRIERS
1014
ELECTRICAL COMPONENT FOR PROVIDING THE TIMING OFFSET TO THE WIRELESS TERMINAL VIA THE AT LEAST ONE DOWNLINK CARRIER
1016
ELECTRICAL COMPONENT FOR RECEIVING AN UPLINK COMMUNICATION VIA THE UPLINK GROUP OF CARRIERS ACCORDING TO THE TIMING OFFSET
MEMORY 1020

FIG. 10

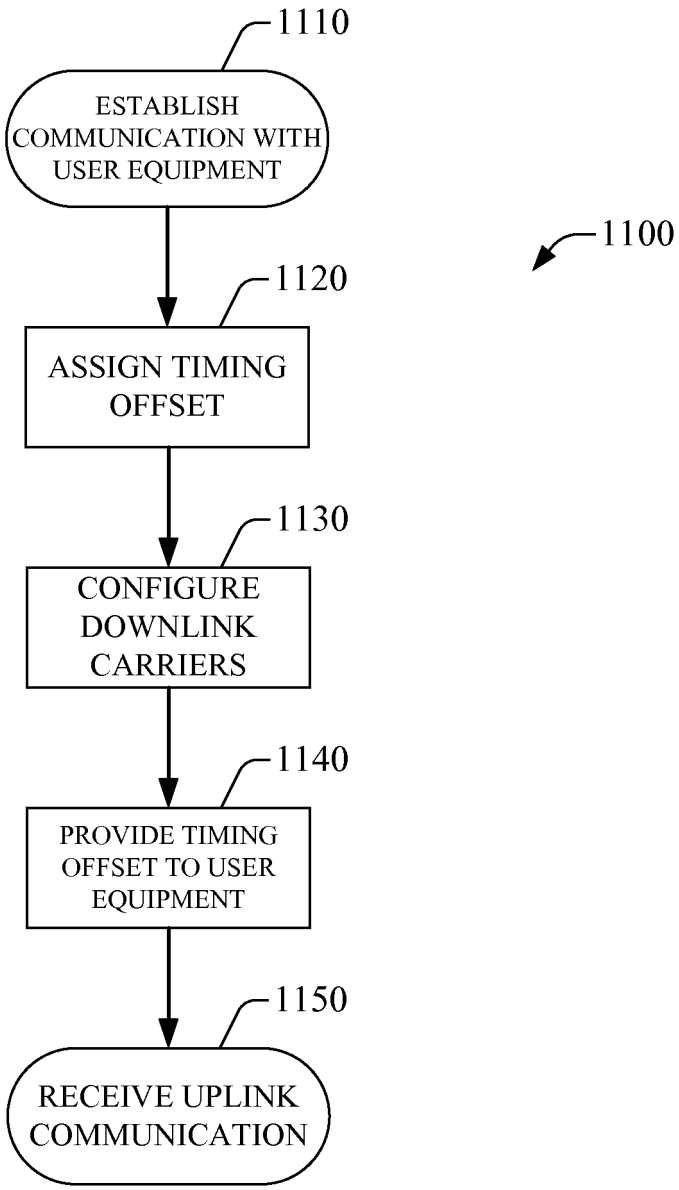

1110
ESTABLISH COMMUNICATION WITH USER EQUIPMENT
1100
1120
ASSIGN TIMING OFFSET
1130
CONFIGURE DOWNLINK CARRIERS
1140
PROVIDE TIMING OFFSET TO USER EQUIPMENT
1150
RECEIVE UPLINK COMMUNICATION

FIG. 11

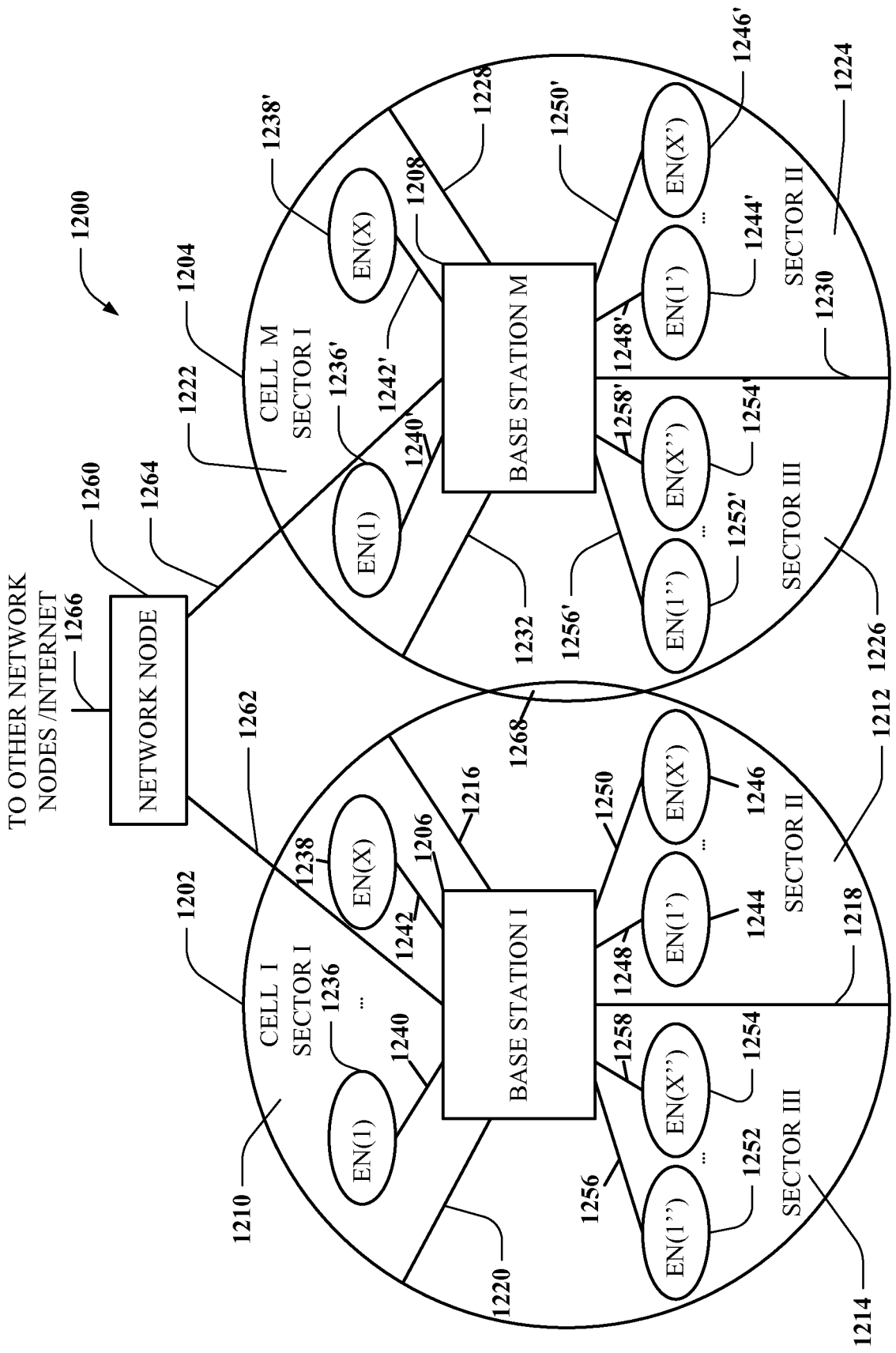

1200
TO OTHER NETWORK NODES /INTERNET
1266
NETWORK NODE
1260
1264
1262
1202
CELL I
SECTOR I
1236
EN(1)
1240
EN(X)
1238
1242
1206
1216
BASE STATION I
1208
1228
1250
1246
EN(X')
1244
EN(1')
1248
1258
1254
EN(X'')
1252
EN(1'')
1256
SECTOR II
SECTOR III
1212
1218
1210
1220
1214
1268
1204
1222
CELL M
SECTOR I
1236'
EN(1)
1240'
EN(X)
1238'
1242'
BASE STATION M
1208'
1228'
1250'
1246'
EN(X')
1244'
EN(1')
1248'
1258'
1254'
EN(X'')
1252'
EN(1'')
1256'
SECTOR II
SECTOR III
1224
1230
1232
1226

FIG. 12

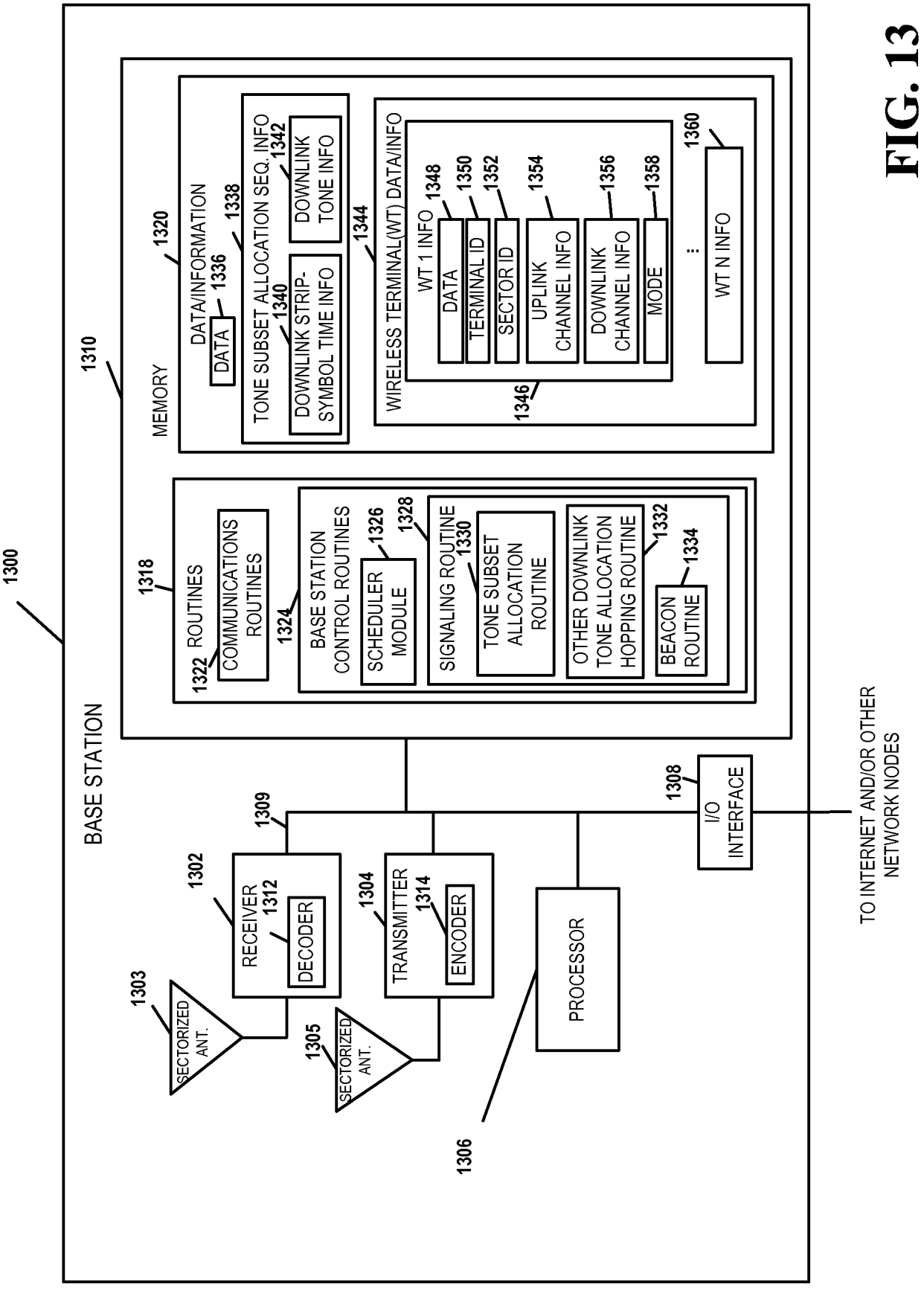

1300
BASE STATION
1310
MEMORY
1320
DATA/INFORMATION
1336
DATA
1338
TONE SUBSET ALLOCATION SEQ. INFO
1340
DOWNLINK STRIP-SYMBOL TIME INFO
1342
DOWNLINK TONE INFO
1344
WIRELESS TERMINAL(WT) DATA/INFO
1346
WT 1 INFO
1348
DATA
1350
TERMINAL ID
1352
SECTOR ID
1354
UPLINK CHANNEL INFO
1356
DOWNLINK CHANNEL INFO
1358
MODE
1360
WT N INFO
1318
ROUTINES
1322
COMMUNICATIONS ROUTINES
1324
BASE STATION CONTROL ROUTINES
1326
SCHEDULER MODULE
1328
SIGNALING ROUTINE
1330
TONE SUBSET ALLOCATION ROUTINE
1332
OTHER DOWNLINK TONE ALLOCATION HOPPING ROUTINE
1334
BEACON ROUTINE
1309
1308
I/O INTERFACE
TO INTERNET AND/OR OTHER NETWORK NODES
1302
RECEIVER
1312
DECODER
1304
TRANSMITTER
1314
ENCODER
1303
SECTORIZED ANT.
1305
SECTORIZED ANT.
1306
PROCESSOR

FIG. 13

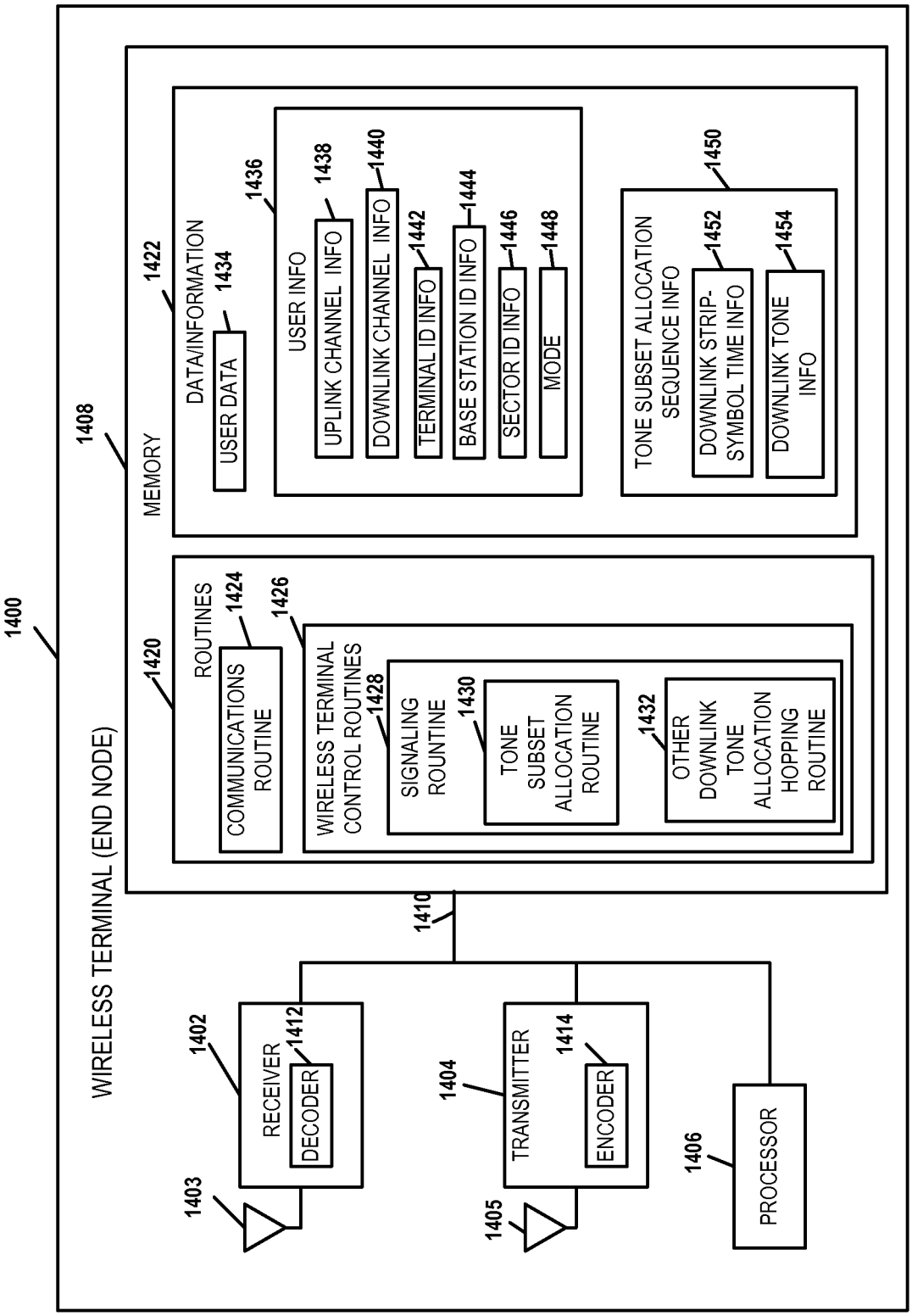

1400
WIRELESS TERMINAL (END NODE)
1408
MEMORY
1422
DATA/INFORMATION
1434
USER DATA
1436
USER INFO
1438
UPLINK CHANNEL INFO
1440
DOWNLINK CHANNEL INFO
1442
TERMINAL ID INFO
1444
BASE STATION ID INFO
1446
SECTOR ID INFO
1448
MODE
1450
TONE SUBSET ALLOCATION SEQUENCE INFO
1452
DOWNLINK STRIP-SYMBOL TIME INFO
1454
DOWNLINK TONE INFO
1420
ROUTINES
1424
COMMUNICATIONS ROUTINE
1426
WIRELESS TERMINAL CONTROL ROUTINES
1428
SIGNALING ROUTINE
1430
TONE SUBSET ALLOCATION ROUTINE
1432
OTHER DOWNLINK TONE ALLOCATION HOPPING ROUTINE
1410
1402
RECEIVER
1412
DECODER
1403
1404
TRANSMITTER
1414
ENCODER
1405
1406
PROCESSOR

FIG. 14