

ABSTRACT OF THE DISCLOSURE

A synchronous semiconductor storage device which operates in synchronization with a system clock signal includes: a first feedback loop which latches an address data signal; a first latch circuit including a first transfer gate which controls the latching by the first feedback loop of the address data signal; a second feedback loop which holds the address data signal latched by the first feedback loop; a second latch circuit including a second transfer gate which controls the holding by the second feedback loop of the address data signal latched by the first feedback loop; a data input control signal generation circuit for generating a data input control signal based on the system clock signal and control signals; and an address latch signal generation circuit for generating an address latch signal from a logical sum of the system clock signal and the data input control signal, wherein the address latch signal is input to the first transfer gate to control the latching of the address data signal, and the data input control signal is input to the second transfer gate to control the holding of the address data signal latched by the first feedback loop.

This Sheet Has Been Replaced
