CLAIMS

1. A semiconductor substrate processing system, comprising:

a substrate support defined to support a substrate in exposure to a processing region;

a first plasma chamber defined to generate a first plasma and supply reactive constituents of the first plasma to the processing region; and

a second plasma chamber defined to generate a second plasma and supply reactive constituents of the second plasma to the processing region,

wherein the first and second plasma chambers are defined to be independently controlled.

2. A semiconductor substrate processing system as recited in claim 1, further comprising:

a first power supply defined to supply a first power to the first plasma chamber;

a first process gas supply defined to supply a first process gas to the first plasma chamber;

a second power supply defined to supply a second power to the second plasma chamber; and

a second process gas supply defined to supply a second process gas to the second plasma chamber.

3. A semiconductor substrate processing system as recited in claim 2, wherein either the first and second power supplies are independently controllable, or the first and second process gas supplies are independently controllable, or both the first and second power supplies and the first and second process gas supplies are independently controllable.

4. A semiconductor substrate processing system as recited in claim 2, wherein the first power is either direct current (DC) power, radiofrequency (RF) power, or a combination of DC and RF power, and wherein the second power is either DC power, RF power, or a combination of DC and RF power.

5. A semiconductor substrate processing system as recited in claim 1, wherein the first and second plasma chambers are defined to operate in either a simultaneous manner or a pulsed manner, wherein the pulsed manner includes either the first plasma chamber or the second plasma chamber operating at a given time and in an alternating sequence.

6. A semiconductor substrate processing system as recited in claim 1, wherein the substrate support is defined to be movable in a direction substantially perpendicular to a top surface of the substrate support upon which the substrate is to be supported.

7. A semiconductor substrate processing system as recited in claim 1, wherein one or both of the first and second plasma chambers is defined to have an energizable plasma outlet region defined to provide supplemental electron generation to increase ion extraction.

8. A semiconductor substrate processing system as recited in claim 2, wherein the substrate support includes an electrode defined to apply a bias voltage across the processing region between the substrate support and the first and second plasma chambers.

9. A semiconductor substrate processing system as recited in claim 1, further comprising:

a baffle structure disposed between the first and second plasma chambers to extend from the first and second plasma chambers toward the substrate support, wherein the baffle structure is defined to reduce fluid communication between the first and second plasma chambers.

10. A semiconductor substrate processing system as recited in claim 1, further comprising:

an exhaust channel formed between the first and second plasma chambers to extend away from the processing region in a direction substantially perpendicular to a top surface of the substrate support upon which the substrate is to be supported.

11. A semiconductor substrate processing system as recited in claim 10, further comprising:

a baffle structure disposed within the exhaust channel between the first and second plasma chambers so as to extend from the first and second plasma chambers toward the substrate support, wherein the baffle structure is defined to reduce fluid communication between the first and second plasma chambers, and wherein the baffle structure is sized smaller than the exhaust channel so as to provide for exhaust flow through the exhaust channel around the baffle structure.

12. A semiconductor substrate processing system, comprising:

a chamber having a top structure, a bottom structure, and sidewalls extending between the top and bottom structures, wherein the chamber encloses a processing region;

a substrate support disposed within the chamber and defined to support a substrate in exposure to the processing region;

a top plate assembly disposed within the chamber above the substrate support, the top plate assembly having a lower surface exposed to the processing region and opposite the top surface of the substrate support, the top plate assembly including a first plurality of plasma

ports connected to supply reactive constituents of a first plasma to the processing region, the top plate assembly including a second plurality of plasma ports connected to supply reactive constituents of a second plasma to the processing region.

13. A semiconductor substrate processing system as recited in claim 12, wherein the substrate support is defined to be movable in a direction substantially perpendicular to a top surface of the substrate support upon which the substrate is to be supported.

14. A semiconductor substrate processing system as recited in claim 12, wherein the substrate support includes an electrode defined to apply a bias voltage across the processing region between the substrate support and the lower surface of the top plate assembly.

15. A semiconductor substrate processing system as recited in claim 12, further comprising:

a first plurality of plasma microchambers each defined to generate the first plasma and supply reactive constituents of the first plasma to one or more of the first plurality of plasma ports; and

a second plurality of plasma microchambers each defined to generate the second plasma and supply reactive constituents of the second plasma to one or more of the second plurality of plasma ports.

16. A semiconductor substrate processing system as recited in claim 15, further comprising:

a first power supply defined to supply a first power to the first plurality of plasma microchambers;

a first process gas supply defined to supply a first process gas to the first plurality of plasma microchambers;

a second power supply defined to supply a second power to the second plurality of plasma microchambers; and

a second process gas supply defined to supply a second process gas to the second plurality of plasma microchambers.

17. A semiconductor substrate processing system as recited in claim 16, wherein either the first and second power supplies are independently controllable, or the first and second process gas supplies are independently controllable, or both the first and second power supplies and the first and second process gas supplies are independently controllable.

18. A semiconductor substrate processing system as recited in claim 12, further

comprising:

a first plasma chamber defined to generate the first plasma and supply reactive constituents of the first plasma to each of the first plurality of plasma ports; and

a second plasma chamber defined to generate the second plasma and supply reactive constituents of the second plasma to each of the second plurality of plasma ports.

19. A semiconductor substrate processing system as recited in claim 18, further comprising:

a first power supply defined to supply a first power to the first plasma chamber;

a first process gas supply defined to supply a first process gas to the first plasma chamber;

a second power supply defined to supply a second power to the second plasma chamber; and

a second process gas supply defined to supply a second process gas to the second plasma chamber.

20. A semiconductor substrate processing system as recited in claim 19, wherein either the first and second power supplies are independently controllable, or the first and second process gas supplies are independently controllable, or both the first and second power supplies and the first and second process gas supplies are independently controllable.

21. A method for processing a semiconductor substrate, comprising:

placing a substrate on a substrate support in exposure to a processing region;

generating a first plasma of a first plasma type;

generating a second plasma of a second plasma type different than the first plasma type; and

supplying reactive constituents of both the first and second plasmas to the processing region to affect a processing of the substrate.

22. A method for processing a semiconductor substrate as recited in claim 21, wherein the first plasma is generated to have a first ratio of ion density to radical density, and wherein the second plasma is generated to have a second ratio of ion density to radical density, the second ratio of ion density to radical density in the second plasma being different than the first ratio of ion density to radical density in the first plasma.

23. A method for processing a semiconductor substrate as recited in claim 21, further comprising:

using a first power and a first process gas to generate the first plasma; and

using a second power and a second process gas to generate the second plasma.

24. A method for processing a semiconductor substrate as recited in claim 23, further comprising:

independently controlling either the first and second powers, or the first and second process gases, or both the first and second powers and the first and second process gases.

25. A method for processing a semiconductor substrate as recited in claim 23, wherein the first power is either direct current (DC) power, radiofrequency (RF) power, or a combination of DC and RF power, and wherein the second power is either DC power, RF power, or a combination of DC and RF power.

26. A method for processing a semiconductor substrate as recited in claim 21, wherein reactive constituents from both the first and second plasmas are supplied in a substantially uniform manner throughout the processing region in exposure to the substrate.

27. A method for processing a semiconductor substrate as recited in claim 21, wherein reactive constituents from the first and second plasmas are generated and supplied in either a simultaneous manner or a pulsed manner, wherein the pulsed manner includes generation and supply of reactive constituents of either the first plasma or the second plasma at a given time and in an alternating sequence.

28. A method for processing a semiconductor substrate as recited in claim 21, further comprising:

generating supplemental electrons to increase ion extraction from one or both of the first and second plasmas into the processing region.

29. A method for processing a semiconductor substrate as recited in claim 21, further comprising:

applying a bias voltage across the processing region from the substrate support so as to attract ions from one or both of the first and second plasmas toward the substrate.

30. A method for processing a semiconductor substrate as recited in claim 21, further comprising:

positioning a baffle structure between a first port through which the first plasma is supplied to the processing region and a second port through which the second plasma is supplied to the processing region.

31. A semiconductor substrate processing system, comprising:

a plate assembly having a process-side surface exposed to a plasma processing region;

an exhaust channel formed through the process-side surface of the plate assembly to

provide for removal of exhaust gases from the plasma processing region;

a plasma microchamber formed inside the exhaust channel;

a gas supply channel formed through the plate assembly to flow a process gas to the plasma microchamber in the exhaust channel; and

a power delivery component formed within the plate assembly to transmit power to the plasma microchamber, so as to transform the process gas into a plasma within the plasma microchamber in the exhaust channel.

32. A semiconductor substrate processing system as recited in claim 31, further comprising:

an electrode disposed outside of the plate assembly that when energized causes ions to be attracted from the plasma microchamber in the exhaust channel into the plasma processing region.

33. A semiconductor substrate processing system as recited in claim 32, further comprising:

a substrate support disposed to support a substrate in exposure to the plasma processing region, wherein the electrode is disposed within the substrate support.

34. A semiconductor substrate processing system as recited in claim 33, wherein the exhaust channel is defined to remove gases from the processing region in a direction substantially perpendicular to and away from a surface of the substrate support upon which the substrate is to be supported.

35. A semiconductor substrate processing system as recited in claim 31, further comprising:

a power supply defined to supply the power to the power delivery component; and

a process gas supply defined to supply a process gas to the gas supply channel.

36. A semiconductor substrate processing system as recited in claim 31, wherein the power delivery component is defined as a coil formed within the plate assembly to circumscribe the plasma microchamber in the exhaust channel.

37. A semiconductor substrate processing system, comprising:

a chamber having a top structure, a bottom structure, and sidewalls extending between the top and bottom structures, the chamber including a processing region;

a substrate support disposed within the chamber, the substrate support having a top surface defined to support a substrate in exposure to the processing region;

a top plate assembly disposed within the chamber above the substrate support, the top

plate assembly having a lower surface exposed to the processing region and opposite the top surface of the substrate support, the top plate assembly including:

a first set of plasma microchambers each formed into the lower surface of the top plate assembly,

a first network of gas supply channels formed to flow a first process gas to each of the first set of plasma microchambers, each of the first set of plasma microchambers defined to transform the first process gas into a first plasma in exposure to the processing region,

a set of exhaust channels formed through the lower surface of the top plate assembly to provide for removal of exhaust gases from the processing region,

a second set of plasma microchambers respectively formed inside the set of exhaust channels, and

a second network of gas supply channels formed to flow a second process gas to each of the second set of plasma microchambers, each of the second set of plasma microchambers defined to transform the second process gas into a second plasma in exposure to the processing region.

38. A semiconductor substrate processing system as recited in claim 37, wherein the first set of plasma microchambers are interspersed with the second set of plasma microchambers in a substantially uniform manner across the lower surface of the top plate assembly.

39. A semiconductor substrate processing system as recited in claim 37, further comprising:

a first power supply defined to supply a first power to the first set of plasma microchambers;

a first process gas supply defined to supply a first process gas to the first network of gas supply channels;

a second power supply defined to supply a second power to the second set of plasma microchambers; and

a second process gas supply defined to supply a second process gas to the second network of gas supply channels.

40. A semiconductor substrate processing system as recited in claim 39, wherein either the first and second power supplies are independently controllable, or the first and second process gas supplies are independently controllable, or both the first and second

power supplies and the first and second process gas supplies are independently controllable.

41. A semiconductor substrate processing system as recited in claim 39, further comprising:

a first set of power delivery components respectively disposed within the top plate assembly about the first set of plasma microchambers, each of the first set of power delivery components connected to receive the first power from the first power supply; and

a second set of power delivery components respectively disposed within the top plate assembly about the second set of plasma microchambers, each of the second set of power delivery components connected to receive the second power from the second power supply.

42. A semiconductor substrate processing system as recited in claim 37, wherein the first and second sets of plasma microchambers are defined to operate in either a simultaneous manner or a pulsed manner, wherein the pulsed manner includes either the first set of plasma microchambers or the second set of plasma microchambers operating at a given time and in an alternating sequence.

43. A semiconductor substrate processing system as recited in claim 37, wherein the substrate support is defined to be movable in a direction extending perpendicularly between the top surface of the substrate support upon which the substrate is to be supported and the lower surface of the top plate assembly.

44. A semiconductor substrate processing system as recited in claim 37, wherein the substrate support includes an electrode defined to apply a bias voltage across the processing region between the substrate support and the lower surface of the top plate assembly.

45. A method for processing a semiconductor substrate, comprising:

placing a substrate on a substrate support in exposure to a processing region;

operating a first set of plasma microchambers in exposure to the processing region, whereby each of the first set of plasma microchambers generates a first plasma and supplies reactive constituents of the first plasma to the processing region, the first set of plasma microchambers located above the processing region opposite from the substrate support; and

operating a second set of plasma microchambers in exposure to the processing region, whereby each of the second set of plasma microchambers generates a second plasma and supplies reactive constituents of the second plasma to the processing region, wherein the second plasma is different than the first plasma, the second set of plasma microchambers

located above the processing region opposite from the substrate support and interspersed in a substantially uniform manner among the first set of plasma microchambers.

46. A method for processing a semiconductor substrate as recited in claim 45, further comprising:

supplying a first power to the first set of plasma microchambers;

supplying a first process gas to the first set of plasma microchambers;

supplying a second power to the second set of plasma microchambers; and

supplying a second process gas to the second set of plasma microchambers.

47. A method for processing a semiconductor substrate as recited in claim 46, further comprising:

independently controlling either the first and second powers, or the first and second process gases, or both the first and second powers and the first and second process gases.

48. A method for processing a semiconductor substrate as recited in claim 46, wherein the first power is either direct current (DC) power, radiofrequency (RF) power, or a combination of DC and RF power, and wherein the second power is either DC power, RF power, or a combination of DC and RF power.

49. A method for processing a semiconductor substrate as recited in claim 46, further comprising:

removing exhaust gases from the processing region through a set of exhaust channels defined to remove gases from the processing region in a direction substantially perpendicular to and away from a top surface of the substrate support upon which the substrate is placed.

50. A method for processing a semiconductor substrate as recited in claim 49, wherein the second set of plasma microchambers are respectively defined inside the set of exhaust channels.

51. A method for processing a semiconductor substrate as recited in claim 45, further comprising:

operating the first set of plasma microchambers to generate the first plasma to have a first ratio of ion density to radical density; and

operating the second set of plasma microchambers to generate the second plasma to have a second ratio of ion density to radical density, the second ratio of ion density to radical density in the second plasma being different than the first ratio of ion density to radical density in the first plasma.

52. A method for processing a semiconductor substrate as recited in claim 51,

wherein the first plasma has a higher radical density than ion density, and wherein the second plasma has a higher ion density than radical density.

53. A method for processing a semiconductor substrate as recited in claim 45, wherein the first and second sets of plasma microchambers are operated in a simultaneous manner.

54. A method for processing a semiconductor substrate as recited in claim 45, wherein the first and second sets of plasma microchambers are operated in a pulsed manner, wherein the pulsed manner includes operation of either the first set of plasma microchambers or the second set of plasma microchambers at a given time and in an alternating sequence.

55. A method for processing a semiconductor substrate as recited in claim 45, further comprising:

applying a bias voltage across the processing region from the substrate support so as to attract ions from one or both of the first and second plasmas toward the substrate.

CLAIMS:

1. A semiconductor substrate processing system, comprising: a substrate support defined to support a substrate in exposure to a processing region; a first plasma chamber defined to generate a first plasma within an interior region of the first plasma chamber and supply reactive constituents of the first plasma from the interior region of the first plasma chamber to the processing region, the first plasma chamber including a first upper electrode positioned on an upper surface within the interior region of the first plasma chamber, the first upper electrode including at least one hole defined to enable fluid communication of a first process gas to the interior region of the first plasma chamber, the first plasma chamber including a first lower electrode positioned on a lower surface within the interior region of the first plasma chamber, the first lower electrode including at least one hole defined to enable passage of reactive constituents of the first plasma from the interior region of the first plasma chamber to the processing region, the first upper electrode and the first lower electrode positioned in a substantially parallel orientation with the substrate support, the first upper electrode and the first lower electrode separated from each other by the interior region of the first plasma chamber; a second plasma chamber defined to generate a second plasma within an interior region of the second plasma chamber and supply reactive constituents of the second plasma from the interior region of the second plasma chamber to the processing region, the second plasma chamber including a second upper electrode positioned on an upper surface within the interior region of the second plasma chamber, the second upper electrode including at least one hole defined to enable fluid communication of a second process gas to the interior region of the second plasma chamber, the second plasma chamber including a second lower electrode positioned on a lower surface within the interior region of the second plasma chamber, the second lower electrode including at least one hole defined to enable passage of reactive constituents of the second plasma from the interior region of the second plasma chamber to the processing region, the

second upper electrode and the second lower electrode positioned in a substantially parallel orientation with the substrate support, the second upper electrode and the second lower electrode separated from each other by the interior region of the second plasma chamber, wherein the first and second plasma chambers are defined to be independently controlled; and an exhaust channel formed between the first and second plasma chambers; a baffle structure disposed within the exhaust channel between the first and second plasma chambers and separated from the first and second plasma chambers, the baffle structure configured to be movable in a first direction toward the substrate support and in a second direction away from the substrate support, the baffle structure configured to be movable in the first and second directions without corresponding movement of the first and second plasma chambers, the baffle structure sized smaller than the exhaust channel so as to provide for exhaust flow through the exhaust channel between the baffle structure and each of the first and second plasma chambers.

2. A semiconductor substrate processing system as recited in claim 1, further comprising: a first power supply defined to supply a first power to the first upper electrode and the first lower electrode within the first plasma chamber; a first process gas supply defined to supply a first process gas to the interior region of the first plasma chamber; a second power supply defined to supply a second power to the second upper electrode and the second lower electrode within the second plasma chamber; and a second process gas supply defined to supply a second process gas to the interior region of the second plasma chamber.

3. A semiconductor substrate processing system as recited in claim 2, wherein either the first and second power supplies are independently controllable, or the first and second process gas supplies are independently controllable, or both the first and second power supplies and the first and second process gas supplies are independently controllable.

4. A semiconductor substrate processing system as recited in claim 2, wherein the first power is either direct current (DC) power, radiofrequency (RF) power, or a combination of DC and RF power, and wherein the second power is either DC power, RF power, or a combination of DC and RF power.

5. A semiconductor substrate processing system as recited in claim 2, wherein the substrate support includes an electrode defined to apply a bias voltage across the processing region between the substrate support and the first and second plasma chambers.

6. A semiconductor substrate processing system as recited in claim 1, wherein the first and second plasma chambers are defined to operate in either a simultaneous manner or a pulsed manner, wherein the pulsed manner includes either the first plasma chamber or the second plasma chamber operating at a given time and in an alternating sequence.

7. A semiconductor substrate processing system as recited in claim 1, wherein the substrate support is defined to be movable in a direction substantially perpendicular to a top surface of the substrate support upon which the substrate is to be supported.

8. A semiconductor substrate processing system as recited in claim 1, wherein one or both of the first and second plasma chambers is defined to have an energizable plasma outlet region defined to provide supplemental electron generation to increase ion extraction.

9. A semiconductor substrate processing system as recited in claim 1, wherein the exhaust channel is formed to extend away from the processing region in a direction substantially perpendicular to a top surface of the substrate support upon which the substrate is to be

supported.

10. A semiconductor substrate processing system as recited in claim 9, wherein the baffle structure is defined to reduce fluid communication between the first and second plasma chambers.

11. A semiconductor substrate processing system as recited in claim 1, wherein the baffle structure is formed of a dielectric material to reduce power communication between the first and second plasma chambers.

12. A method for processing a semiconductor substrate, comprising: placing a substrate on a substrate support in exposure to a processing region; generating a first plasma of a first plasma type within an interior region of a first plasma chamber, the first plasma chamber including a first upper electrode positioned on an upper surface within the interior region of the first plasma chamber, the first upper electrode including at least one hole defined to enable fluid communication of a first process gas to the interior region of the first plasma chamber, the first plasma chamber including a first lower electrode positioned on a lower surface within the interior region of the first plasma chamber, the first lower electrode including at least one hole defined to enable passage of reactive constituents of the first plasma from the interior region of the first plasma chamber to the processing region, the first upper electrode and the first lower electrode positioned in a substantially parallel orientation with the substrate support, the first upper electrode and the first lower electrode separated from each other by the interior region of the first plasma chamber; generating a second plasma of a second plasma type within an interior region of a second plasma chamber, the second plasma chamber including a second upper electrode positioned on an upper surface within the interior region of the second plasma chamber, the second upper electrode including at least one hole defined to enable fluid

communication of a second process gas to the interior region of the second plasma chamber, the second plasma chamber including a second lower electrode positioned on a lower surface within the interior region of the second plasma chamber, the second lower electrode including at least one hole defined to enable passage of reactive constituents of the second plasma from the interior region of the second plasma chamber to the processing region, the second upper electrode and the second lower electrode positioned in a substantially parallel orientation with the substrate support, the second upper electrode and the second lower electrode separated from each other by the interior region of the second plasma chamber, the second plasma type different than the first plasma type, wherein the first and second plasma chambers are independently controlled; supplying reactive constituents of both the first and second plasmas to the processing region to affect a processing of the substrate; positioning a baffle structure within an exhaust channel located between the first and second plasma chambers, the baffle structure sized smaller than the exhaust channel such that an exhaust flow is provided from the processing region through the exhaust channel between the baffle structure and each of the first and second plasma chambers; and moving the baffle structure in a first direction toward the substrate support without corresponding movement of the first and second plasma chambers, or moving the baffle structure in a second direction away the substrate support without corresponding movement of the first and second plasma chambers.

13. A method for processing a semiconductor substrate as recited in claim 12, wherein the first plasma is generated to have a first ratio of ion density to radical density, and wherein the second plasma is generated to have a second ratio of ion density to radical density, the second ratio of ion density to radical density in the second plasma being different than the first ratio of ion density to radical density in the first plasma.

14. A method for processing a semiconductor substrate as recited in claim 12, further

comprising: using a first power and a first process gas to generate the first plasma; and using a second power and a second process gas to generate the second plasma.

15. A method for processing a semiconductor substrate as recited in claim 14, further comprising: independently controlling either the first and second powers, or the first and second process gases, or both the first and second powers and the first and second process gases.

16. A method for processing a semiconductor substrate as recited in claim 14, wherein the first power is either direct current (DC) power, radiofrequency (RF) power, or a combination of DC and RF power, and wherein the second power is either DC power, RF power, or a combination of DC and RF power.

17. A method for processing a semiconductor substrate as recited in claim 12, wherein reactive constituents from both the first and second plasmas are supplied in a substantially uniform manner throughout the processing region in exposure to the substrate.

18. A method for processing a semiconductor substrate as recited in claim 12, wherein reactive constituents from the first and second plasmas are generated and supplied in either a simultaneous manner or a pulsed manner, wherein the pulsed manner includes generation and supply of reactive constituents of either the first plasma or the second plasma at a given time and in an alternating sequence.

19. A method for processing a semiconductor substrate as recited in claim 12, further comprising: generating supplemental electrons to increase ion extraction from one or both of the first and second plasmas into the processing region.

20. A method for processing a semiconductor substrate as recited in claim 12, further comprising: applying a bias voltage across the processing region from the substrate support so as to attract ions from one or both of the first and second plasmas toward the substrate.