ABSTRACT

A three-dimensional semiconductor device comprises a first active region on a substrate and including a lower channel pattern and a lower source/drain pattern connected to the lower channel pattern, a second active region stacked on the first active region and including an upper channel pattern and an upper source/drain pattern connected to the upper channel pattern, a gate electrode on the lower channel pattern and the upper channel pattern, a first active contact electrically connected to the lower source/drain pattern, an upper separation structure between the first active contact and the upper source/drain pattern, a second active contact electrically connected to the upper source/drain pattern, and a lower separation structure between the second active contact and the lower source/drain pattern.

FIG. 4C