



DATA DETECTION FOR LOCAL PROBE DATA STORAGE DEVICES

The present invention relates to methods and apparatus for data detection in local probe storage devices.

An example of a local probe storage device is described in "The "Millipede" - More than one thousand tips for future AFM data storage", P. Vettiger et al, IBM Journal of Research and Development, Vol.44 No.3, May 2000. The Millipede device comprises an array of thermal resistance sensor probes. Such arrays may be employed in the detection of the topography of a surface in applications such as surface visualization and data storage. In the data storage application, data recorded in a surface topography may be read by moving a thermal resistance sensor over the surface and detecting changes in thermal conductance between the sensor and the surface as the distance between the sensor and the surface varies. As described in the aforementioned Vettiger et al. reference, the Millipede device comprises a two dimensional array of cantilever sensors fabricated on a silicon substrate. Each cantilever is attached at one end to the substrate. The other end of each cantilever carries a resistive heater element and an outward facing tip. Each cantilever is addressable via row and column conductors. The row and column conductors permit selective passage of electrical current through each cantilever to heat the heating element thereon. In both reading and writing operations, the tips of the array are brought into contact with and moved relative to a storage medium comprising a polymer film storage surface carried on a plane substrate.

Data is written to the storage medium by a combination of applying a local force to the film via each tip and selectively heating each tip via application of data signals through the corresponding row and column conductors to a level sufficient to locally deform the film, leaving an indentation or pit therein.

Each heating element also provides a thermal read back sensor because it has a resistance which is dependent on temperature. For data reading operations, a heating signal is applied sequentially to each row in the array. The heating signal heats all heating elements in the selected row, but now to a temperature which is



insufficient to deform the film. The thermal conductance between the heating elements and the surface varies according to distance between the heating elements and the surface. When a tip moves into a pit as the array is scanned across the surface, the distances between the associated heating element and the storage medium reduce. The medium between the heating elements and the surface transfers heat between the heating elements and the storage surface. Heat transfer between each heating element and the surface becomes more efficient when the associated tip moves into a pit. The temperature and therefore the resistance of the heating element therefore reduces. Changes in temperature of the continuously heated heating elements of each row can be monitored in parallel, thereby facilitating detection of recorded bits. A problem associated with such detection is that the signals received from the heating elements may contain unwanted offsets. Another problem associated with such detection is that the signals received from the heating elements may contain noise components. Such unwanted features of the signals received from the heating elements can interfere with bit recovery. Accordingly it would be desirable to provide detection methods and apparatus in which such problems are alleviated.

In accordance with the present invention, there is now provided apparatus for detecting data in a sensor signal generated by a read sensor in a local probe data storage device, the apparatus comprising: a differentiator for subtracting a value of the sensor signal from the succeeding value of the sensor signal to generate a ternary difference signal; and a convertor connected to the differentiator for converting the difference signal into a binary output signal indicative of the detected data. This advantageously prevents offsets in the sensor signal from interfering with recovery of the data. The differentiator effectively acts as a high pass filter.

A low pass filter may be connected to the differentiator for filtering the sensor signal prior to the sensor signal reaching the differentiator. This advantageously eliminates unwanted high frequency noise components from the input to the differentiator.

In particularly preferred embodiments of the present invention, a subtractor is connected to the low pass filter for subtracting a reference signal generated by a

reference sensor from the sensor signal prior to the sensor signal reaching the low pass filter. This advantageously reduces dynamic range demand at the input to the low pass filter.

In an embodiment of the present invention which is particularly preferred in the interests of simplicity the differentiator comprises a memory for storing the value of the sensor signal to be subtracted from the succeeding value of the sensor signal and a subtracter connected to the memory for subtracting the value of the sensor signal stored in the memory from the succeeding value to generate the ternary difference signal. In the interests of further simplicity, the subtracter preferably comprises an inverter for inverting the value of the sensor signal stored in the memory to generate an inverted value and an adder connected to the inverter for adding the inverted value to the succeeding value of the sensor signal to generate the ternary difference signal.

The convertor preferably converts the extremities of the ternary difference signal into a first value of the binary output signal and converts the intermediate value of the ternary difference signal into a second value of the binary output signal. Again, In the interests of simplicity, the convertor preferably comprises an integrator for generating a ramp having a slope dependent on the value of a sample of the ternary difference signal and a counter connected to the integrator for determining the binary output in dependence on the time taken for the ramp to reach a preset threshold level.

It will be appreciated that the present invention extends to a local probe data storage device comprising: a storage surface; a read sensor moveable relative to the storage surface in a plane parallel to the storage surface for generating a sensor signal in dependence on data stored in the surface in the form of topographical features thereof; and apparatus as hereinbefore described connected to the sensor for detecting the data in the sensor signal generated by the read sensor as the read sensor is moved relative to the storage surface.

The present invention also extends to a local probe data storage device comprising a read sensor moveable relative to the storage surface in a plane parallel to the storage surface for generating a sensor signal in dependence on data stored in the surface in the form of topographical features thereof; a reference sensor for generating a reference signal in dependence on a reference point in the surface; and apparatus as claimed in any claim dependent on claim 3 connected to the read sensor and the reference sensor for detecting the data in the sensor signal generated by the read sensor as the read sensor is moved relative to the storage surface.

Preferably, local probe storage devices embodying the present invention further comprise a precoder for precoding data to be written onto the storage surface, the precoder comprising an exclusive or gate having an output determined for each bit of an input bit stream to be recorded onto the storage surface in dependence on the value of the bit to be recorded and the value of the output of the exclusive or gate corresponding to the preceding bit of the input bit stream. Also, it will be appreciated that such a storage device may comprise a plurality of read sensors.

Viewing the present invention from another aspect, there is now provided a method for detecting data in a sensor signal generated by a read sensor in a local probe data storage device, the method comprising: subtracting a value of the sensor signal from the succeeding value of the sensor signal to generate a ternary difference signal using a differentiator; and converting the difference signal into a binary output signal indicative of the detected data using a convertor connected to the differentiator.

Preferred embodiments of the present invention will now be described by way of example only with reference to the accompanying drawings, in which:

Figure 1 is a simplified plan view of an example of a local probe data storage device;

Figure 2 is a simplified circuit diagram of a sensor of the device;

Figure 3 is a Norton equivalent circuit of the sensor;

Figure 4 is a block diagram of an example of a detection channel for the sensor;

Figure 5 is a simplified block diagram of a low pass filter for the detection channel;

Figure 6 is a simplified block diagram of a high pass filter for the detection channel;

Figure 7 is a block diagram of an analog to digital convertor for the detection channel;

Figure 8 is a detailed block diagram of the detection channel;

Figure 9 is a detailed block diagram of a modification of the detection channel;

Figure 10 is a block diagram of a detection channel in which precoding is employed;

Figure 11 is a block diagram of a precoder for the detection channel of Figure 10;

Figure 12 is a simplified circuit diagram of a sensor circuit for the device;

Figure 13 is a simplified circuit diagram of another sensor circuit for the device;

Figure 14 is a graph of the input characteristic of a preamplifier of the Figure 13 sensor circuit;

Figure 15 is a circuit diagram of an example of the preamplifier implemented in CMOS;

Figure 16 is a circuit diagram of an example of the low pass filter implemented in CMOS;

Figure 17 is a circuit diagram of another example of the low pass filter implemented in CMOS;

Figure 18 is a bloc diagram of another example of the low pass filter;

Figure 19 is a block diagram of another example of the high pass filter;

Figure 20 is a circuit diagram of a memory stage and inverter of the high filter implemented in CMOS;

Figure 21 is a block diagram of an example of the analog to digital convertor;

Figure 22 is a block diagram of an implementation of the analog to digital convertor shown in Figure 21;

Figure 23 is a block diagram of another implementation of the analog to digital convertor;

Figure 24 is a block diagram of an example of the detection channel;

Figure 25 is a block diagram of another example of the detection channel

Figure 26 is a circuit diagram of an example of the detection channel.

Referring first to Figure 1, an example of a local probe data storage device comprises a two dimensional array of cantilever sensors 10 disposed on a silicon substrate. Row conductors 30 and column conductors 40 are also disposed on the substrate. Each sensor 10 is addressed by a different combination of the row conductors 30 and column conductors 40. There are a pair of row conductors and associated with each column of sensors 10 and one row conductor associated with each row of sensors 10. Each sensor 10 comprises a silicon cantilever structure of a length in the region of 70 micrometres and micrometre thickness. Limbs of the cantilever are fixed, at their distal ends, to the substrate. The apex of the cantilever

has freedom for movement in a direction normal to the substrate. The cantilever carries, at its apex, a resistive heater element and a silicon tip facing away from the substrate. The limbs of the cantilever are highly doped to provide a conductive current path. The heater element is formed by doping the apex of the cantilever to a lesser extent, thereby introducing a region of increased electrical resistance to current flow through the cantilever. The current path through the cantilever extends between the associated row conductor and the associated column conductors. One of the column conductors is connected to the cantilever via an intermediate diode D. Specifically, the cathode of the diode D is connected to the column conductor. The other column conductor is connected to the cantilever via a drive circuit 60. The anode of the diode D and the input to the drive circuit 60 are connected to the corresponding row conductor via the heater element. The row conductors 30, column conductors 40, diodes D and drivers 60 are also disposed on the substrate. The cantilevers are pre-stressed to resiliently bias the tips away from the substrate.

In operation, the tip is urged against to a planar storage medium 70 in the form of a polymer layer such as a film of polymethylmethacrylate (PMMA) of a thickness in the region of 40 nm. The polymer layer is carried by a silicon substrate.

Data is written to the storage medium by a combination of applying a local force to the polymer layer 70 via the tip and heating the tip by passing a write current through the cantilever from the corresponding row conductor 30 to the corresponding column conductor 40. Passage of current through the cantilever causes the heater element to heat up. Heat energy is passed from the heater element into the tip via thermal conductance. The write current is selected to heat the tip to a level sufficient to locally deform the polymer layer 70 to leave a pit 20 therein of a diameter in the region of 40 nm. By way of example, it has been found that local deformation of a PMMA film can be achieved by heating the tip to a temperature of the order of 700 degrees centigrade.

The heating element also provides a thermal read back sensor because it has a resistance which is dependent on temperature. For data reading operations, a heating current is passed through the cantilever from the corresponding row

conductor 30 to the corresponding column conductor 40. Accordingly, the heating element is again heated, but now to a temperature which is insufficient to deform the polymer layer 70. Reading temperatures of the order of 400 degrees centigrade are, for example, insufficient to deform a PMMA film, but nevertheless provide acceptable reading performance. The thermal conductance between the heating element and the polymer layer 70 varies according to distance between the heating element and the polymer layer 70. When the tip moves into a pit 20 as the array is scanned across the polymer layer, the distances between the heating element and the polymer layer 70 reduce. The medium between the heating element and the polymer layer transfers heat between the heating element and the polymer layer. Heat transfer between the heating element and the polymer layer more efficient when the tip moves in the pit 20. The temperature and therefore the resistance of the heating element reduces. Changes in temperature of the continuously heated heating element can be monitored, thereby facilitating detection of recorded bits.

The aforementioned heating current is produced by applying a heating voltage pulse to the corresponding row conductor 30. Accordingly, a heating current flows through each sensor 10 connected to the row conductor 30 to which the heating voltage pulse is applied. All the heating elements in the corresponding row of the array are therefore heated. Recorded data is then read out from in parallel from the heated row of sensors. Each row of the array is thus read sequentially according to a multiplexing scheme.

The array is moveable relative to the polymer layer in a plane 70 parallel to the polymer layer 70 such that each tip can be scanned over a corresponding field 80 of the polymer layer 70. Each field 80 can accommodate a plurality of pits 20. In both reading and writing operations, the tips of the array are moved across the surface of the storage medium 70.

Referring to Figure 2, in a preferred embodiment of the present invention, a read/write current flows from a row conductor 30 to which a voltage V_s is applied through a heater element in the corresponding sensor to a lower voltage level applied to the associated column conductor via the diode D. With reference to

Figure 3, this arrangement approximates to a current source I' in series with a variable resistor VR representative of the heater element. The heater element transform the physical value carrying stored information into an electrical signal. The value of variable resistor VR depends on the temperature at the tip. As indicated earlier, during read operation, the tip reaches different temperatures as it moves from the site of a pit (value "1") to the site of no pit (value "0"). A detection circuit for such a system senses a voltage which dependent on the value of the resistance of the heater element and makes a decision as to whether a "1" or a "0" is written at the location of the tip. A "1" produces a relative change in resistance typically of the order of $\Delta R/R = 10^{-4}$. An important issue in detecting the presence or absence of a pit is the relatively large resolution desirable to extract a signal containing information indicative of whether the bit is a "1" or a "0". Such detection is complicated by the presence of various offsets such as those produced by manufacturing tolerances. Conventional threshold detection methods are unsuitable because of the relatively high precision in analog to digital conversion they demand and the uncertainty associated with the offset present in the system.

In a preferred embodiment of the present invention, there is provided a robust detection scheme for such thermomechanical sensor arrays as hereinbefore described. The scheme operates in the analog domain. Offsets in the system are obviated by employing three level decision element to be described shortly. The three level decision element avoids the aforementioned processing of signals exhibiting a relatively wide dynamic range. Additionally, a precoding scheme may be employed to avoid error propagation after the three level decision element without incurring rate loss. It will be appreciated from the following detailed description that the detection schemes embodying the present invention are applicable to both current driven and voltage driven thermomechanical sensor systems.

Referring now to Figure 4, an example of a detection subsystem embodying the present invention comprises a low pass filter 100 and a high pass filter 110 connected in series. An analog to digital convertor (ADC) 120 is connectable to the output of the high pass filter 110 via a sample and hold switch 120. In operation, the low pass filter 100 limits the bandwidth of high frequency noise in an input signal

from a sensor connected thereto. With reference to Figure 5, the low pass filter 100 comprises an integrator having an virtual earth amplifier 140 with a feedback path comprising a capacitor C_f and an input resistance R_s . It will be appreciated that such a low pass filter 100 has a transfer function of $1/s$, where s is the Laplace operator. Referring to Figure 6, the high pass filter comprises a differentiator stage having delay stage 150 and a summing block 160. The delay T imposed by the delay stage 150 is set to the interval between two consecutive decisions on bits stored on the storage medium. This interval corresponds to the time required for the sensor to move from one site at which one pit or absence of pit may be written to the next. The summing block 160 thus adds the outputs from the low pass filter 100 corresponding to two consecutive bit read operations. It will be appreciated that such a high pass filter 110 has a transfer function of $1-e^{-sT}$. In operation, the high pass filter eliminates offsets and low frequency noise. The low pass filter 100 and the high pass filter 110 in cascade produce a three level signal at the input to the ADC 120. Referring to Figure 7, the ADC 120 comprises a three level decision element 170.

Referring to Figure 8, a preferred example of a detection channel embodying the present invention for a constant current source sensor arrangement as hereinbefore described with reference to Figure 3 comprises the low pass filter 100 hereinbefore described with reference to Figure 5, the high pass filter hereinbefore described with reference to Figure 6, the switch 130, and the ADC 170 hereinbefore described with reference to Figure 7.

Referring to Figure 9, in a modification of the embodiment of the present invention hereinbefore described with reference to Figure 8, the dynamic range of the signal input to the low pass filter 100 is reduced. This reduction is achieved by taking an output from a reference sensor represented in Figure 9 by Norton equivalent circuit comprising current source I'' and variable resistance VR' . The output from the reference sensor is subtracted from the sensor output of interest by a differencing block 180. A precision reference signal is not required because the high pass filter 110 removes any offset that may be present at the output of the low pass filter 100. It is sufficient that the variation of the reference signal over two consecutive read intervals is negligible with respect to the difference signal from the output of the

differencing block 180. The reference signal may be obtained for example from a sensor reading a dedicated field in which all bits are equal to "0".

The detection channels hereinbefore described with reference to Figures 8 and 9 are examples of so-called discrete time 1-D channels, where D is the delay. Symbol by symbol detection at the output of a discrete time 1-D channel with a binary input symbol sequence has drawbacks. In the presence of noise, a loss in performance of 2 to 3 dB can be experienced, together with error propagation. The performance loss depends on the noise spectral characteristics. Such losses can be at least partially overcome by maximal likelihood detection of the input sequence. However, maximal likelihood detection requires relatively high complexity. Referring to Figure 10, in a preferred embodiment of the present invention, a precoder 200 is employed to precode the sequence of information bits to be recorded on the storage medium 70. The precoding eliminates error propagation. The ADC 120 comprises combinational logic 210 for equating a "+1" or "-1" from the output of the high pass filter 110 to a "1" at the channel output and for equating a "0" at the output of the high pass filter 110 to a "0" at the channel output. In general, for 1-D^k precoding, a $1/(1 \oplus D^k)$ precoder is employed, where $\oplus$ denotes modulo 2 addition. Referring to Figure 11, the precoder 200 comprises a delay stage 220 having a delay of T and a summing stage 230. In operation, an information bit to be precoded are input to the summing stage and summed with the output from the summing stage 220 for the preceding information bit. The output from the summing stage is fed back to the summing stage via the delay stage 220.

With reference to Figure 12, in a preferred embodiment of the present invention, the sensors operate in current mode as hereinbefore mentioned. In other words, each sensor comprises a current source I' driving a sense resistor VR and providing a voltage signal at the output via a voltage follower 300. A range of standard voltage mode circuits can provide accurate detection of such a signal. However, conventional voltage mode circuits have drawbacks. Specifically, such circuits typically require relatively large chip area and exhibit relatively low performance at relatively low supply voltages. These problems are alleviated in the sense circuit shown in Figure 13. In the Figure 13 sense circuit is suitable for current mode

detection circuits and array architectures. Specifically, the Figure 13 circuit comprises a voltage source V' during the sense resistance V_R and a limiting preamplifier 310 having an input characteristic as shown in Figure 14. The preamplifier 310 limits the power dissipation in the sensor circuit and transfers the sensor signal to the subsequent detection circuitry. Referring now to Figure 15, a simple CMOS implementation of the preamplifier 310 comprises 3 transistors T1, T2, and T3.

An integrator for voltage mode of operation by a passive integrator or by an active integrator. Figure 16 shows an example of a passive integrator circuit in a CMOS implementation comprising transistor T4, capacitor C1 and switch S1. Figure 18 shows an example of an active integrator circuit comprising a virtual earth amplifier 320, a capacitor C3 and a switch S3. Figure 17 shows a CMOS implementation of an integrator circuit for current mode of operation comprising transistor T5, capacitor C2 and switch S2. The integrator shown in Figure 17 is a transintegrator circuit. In general, the low pass filter 100 may be implemented by any one of a variety of approaches, including RC filters, MOSFET filters, transconductance-C (gm-C, OTA-C) filters, switched capacitor filters and current switched filters. In the circuits hereinbefore described with reference to Figures 16, 17, and 18, each of switches S1, S2, and S3 permit the corresponding integrator to be periodically reset. Resetting of such integrators will be described in detail shortly.

As indicated earlier, the differentiator circuit of the high pass filter 110 subtracts a previous signal value from a present signal value to provide an approximation of the derivative of the information signal. Referring now to Figure 19, in a preferred embodiment of the present invention, the high pass filter 110 comprises a memory element 400 having an output connected to an inverter gate 410. The output of the inverter gate 410 and the input to the memory element 400 are connected to the input of a summing stage so that the output of the summing stage produces the value equal to the difference between two consecutive information bits. Figure 20 shows a current mode CMOS implementation of the memory element 400 and the inverter 410 comprising an inverting memory cell based on a switched current transistor memory cell having transistor T6, and switches S4, S5, and S6. The summing stage 410 for the current mode of operation can be implemented simply by

a wired node connection. High pass filter approaches such as RC filters, MOSFET filters, transconductance-C (gm-C, OTA-C) filters, switched capacitor filters and current switched filters have limitation similar to those hereinbefore described with reference to the low pass filter 100. It will be appreciated that switches S1-S6 may be implemented by pass transistors in VLSI embodiments of the present invention.

As mentioned earlier, in preferred embodiments of the present invention, the ADC 120 has a resolution of three levels for the detection of the information signal. Referring now to Figure 21, in a preferred embodiment of the present invention, the ADC 120 comprises an integrator 500 connected to a ramp analog to digital convertor (RADC) 510. The integrator 500 may for example be of any of the forms hereinbefore described with reference to Figures 16, 17 and 18. In operation, the integrator 500 is periodically reset in synchronization with input bits of the ternary output from the high pass filter. For each input bit, the integrator 500 generates a ramp. The slope of the ramp is dependent on the value of the input bit. The RADC 510 measures the slope of the ramp signal by determining the time for the ramp to reach a preset threshold level. Referring now to Figure 22, in a particularly preferred embodiment of the present invention, the RADC 510 is implemented by a comparator 520 preset to the aforementioned threshold level and a counter 530. With reference to Figure 23, a modification to the preferred embodiment of the present invention hereinbefore described with reference to Figure 22 combines three level ADC and inverse precoder functions. In operation, a pair of comparators 600 and 610 each receive the bit stream to be decoded. Comparator 600 compares the bit stream to a first voltage level V1. Comparator 610 compares the bit stream to a second voltage level V2. The outputs of the comparators are combined via a two input NAND gate 620 to provide a data input to a single D type latch 630 clocked at $1/T$. The output of the latch 630 provides the decoded bit stream.

Referring now to Figure 24, in a preferred embodiment of the present invention there is provided an integrator 700 for integrating two consecutive read back signals for the same fixed integration time. The output of the integrator 700 is sampled by a sample and hold circuit 710. The output of the sample and hold circuit is fed to a differentiator comprising a memory element 720, inverter gate 730 and summing

block 740. The differentiator subtracts the current value of the output from the integrator 700 from the preceding value stored in the memory element 730. A second integrator 750 then integrates the resulting value and converts it via the RADC 760. Specifically, the second integrator 750 generates a ramp which is, in turn, compared with a predetermined threshold. The time taken for the ramp to reach the threshold is inversely proportional to the difference between the last two values provided at the output of the sample and hold circuit 710. Thus, in an ideal noiseless case, three possible values of time corresponding to $+d$, 0, and $-d$ are provided at the output of the RADC 760. In the case of a noisy signal, a continuum of time values is quantized into the aforementioned three values.

As shown in Figure 25, integrators 700 and 730 of the Figure 24 embodiment can be combined. In the Figure 25, embodiment only the previous signal value is integrated for a fixed integration time and subsequently stored in the memory cell 720,. The stored value is directly subtracted from the continuously integrated signal value at the output of the integrator 70 upstream of the sample and hold circuit 710. The difference at the output of the adder 740 is then fed to the RADC 760. The integrator 70 in the Figure 25 embodiment simultaneously provides the signal to be stored in the memory element 720 for the next sample and the signal to be fed to the RADC 760 via the adder 740.

With reference to Figure 26, a particularly preferred embodiment of the present invention comprises a CMOS implementation including a first voltage source 810 connected to a thermomechanical detector under test 830 comprising a variable resistance VR. A second voltage source 800 is connected to reference thermomechanical detector comprising a variable resistance VR'. The detector under test 830 is connected to the input of an integrator 850 via a preamplifier 840 comprising transistor T12, T13, and T21. The reference detector 820 is connected to the input of the integrator 850 via a second preamplifier 900 comprising transistors T7, T8 and T9. In operation, the reference detector 820 functions as hereinbefore described with reference to Figure 9. The integrator 850 comprises switch S7, capacitor C4, and transistors T14 and T15. The output of the integrator is connected via transistor T14 to a sampler 880 comprising switch S11. The sampler

S11 is in turn connected to the input of an inverting memory 890 comprising switches S8, S9, S10, S11, S12, S13 and transistors T16, T17, and T18. The output of the memory 890 is connected to an adder 860 constituted by a circuit node. Also coupled to the adder 860 via transistor T15 and switch S14 is the output of the integrator 850. The output of the adder is connected to a comparator 870 comprising a transistors T19 and T20. The sampler 880, memory 890, and adder 860 collectively constitute a differentiator as hereinbefore described. The comparator 870 constitutes an ADC as hereinbefore described.

In summary, there have been hereinbefore described examples of apparatus for detecting data in a sensor signal generated by a read sensor in a local probe data storage device comprising a differentiator for subtracting a value of the sensor signal from the succeeding value of the sensor signal to generate a ternary difference signal; and a convertor connected to the differentiator for converting the difference signal into a binary output signal indicative of the detected data. A local probe data storage device comprising such apparatus is also described..

CLAIMS

1. Apparatus for detecting data in a sensor signal generated by a read sensor in a local probe data storage device, the apparatus comprising: a differentiator for subtracting a value of the sensor signal from the succeeding value of the sensor signal to generate a ternary difference signal; and a convertor connected to the differentiator for converting the difference signal into a binary output signal indicative of the detected data.
2. Apparatus as claimed in claim 1, further comprising a low pass filter connected to the differentiator for filtering the sensor signal prior to the sensor signal reaching the differentiator.
3. Apparatus as claimed in claim 2, further comprising a subtracter connected to the low pass filter for subtracting a reference signal generated by a reference sensor from the sensor signal prior to the sensor signal reaching the low pass filter.
4. Apparatus as claimed in any preceding claim, wherein the differentiator comprises a memory for storing the value of the sensor signal to be subtracted from the succeeding value of the sensor signal and a subtracter connected to the memory for subtracting the value of the sensor signal stored in the memory from the succeeding value to generate the ternary difference signal.
5. Apparatus as claimed in claim 4, wherein the subtracter comprises an inverter for inverting the value of the sensor signal stored in the memory to generate an inverted value and an adder connected to the inverter for adding the inverted value to the succeeding value of the sensor signal to generate the ternary difference signal.
6. Apparatus as claimed in any preceding claim, wherein the convertor converts the extremities of the ternary difference signal into a first value of the binary output signal and converts the intermediate value of the ternary difference signal into a second value of the binary output signal.

7. Apparatus as claimed in claim 6, wherein the convertor comprises an integrator for generating a ramp having a slope dependent on the value of a sample of the ternary difference signal and a counter connected to the integrator for determining the binary output in dependence on the time taken for the ramp to reach a preset threshold level.
8. A local probe data storage device comprising: a storage surface; a read sensor moveable relative to the storage surface in a plane parallel to the storage surface for generating a sensor signal in dependence on data stored in the surface in the form of topographical features thereof; and apparatus as claimed in any preceding claim connected to the sensor for detecting the data in the sensor signal generated by the read sensor as the read sensor is moved relative to the storage surface.
9. A local probe storage device comprising a storage surface; a read sensor moveable relative to the storage surface in a plane parallel to the storage surface for generating a sensor signal in dependence on data stored in the surface in the form of topographical features thereof; a reference sensor for generating a reference signal in dependence on a reference point in the surface; and apparatus as claimed in any claim dependent on claim 3 connected to the read sensor and the reference sensor for detecting the data in the sensor signal generated by the read sensor as the read sensor is moved relative to the storage surface.
10. A local probe storage device as claimed in claim 8 or claim 9, comprising a precoder for precoding data to be written onto the storage surface, the precoder comprising an exclusive or gate having an output determined for each bit of an input bit stream to be recorded onto the storage surface in dependence on the value of the bit to be recorded and the value of the output of the exclusive or gate corresponding to the preceding bit of the input bit stream.
11. A local probe storage device as claimed in any of claims 8 to 10, comprising a plurality of sensors.

12. A method for detecting data in a sensor signal generated by a read sensor in a local probe data storage device, the method comprising: subtracting a value of the sensor signal from the succeeding value of the sensor signal to generate a ternary difference signal using a differentiator; and converting the difference signal into a binary output signal indicative of the detected data using a convertor connected to the differentiator.