(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 October 2008 (02.10.2008)

PCT

(10) International Publication Number
WO 2008/118811 A1

(51) International Patent Classification:
H01L 21/336 (2006.01) *H01L 29/78* (2006.01)

(21) International Application Number:
PCT/US2008/057910

(22) International Filing Date: 21 March 2008 (21.03.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/729,192 27 March 2007 (27.03.2007) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DATTA, Suman** [IN/US]; 16659 NW Talkingstick Way, Beaverton, Oregon 97006 (US). **KAVALIEROS, Jack** [US/US]; 14260 NW Belle Court, Portland, Oregon 97229 (US). **DOYLE, Brian** [IE/US]; 11156 NW Montreux Lane, Portland, Oregon 97229 (US). **SOMASEKHAR, Dinesh** [IN/US]; 621 NW 112th Avenue, Portland, Oregon 97229 (US). **KESHAVARZI, Ali** [IR/US]; 2341 N.W. Birdendene Street, Portland, Oregon 97229 (US).

(74) Agents: **VINCENT, Lester J.** et al.; Blakely Sokoloff Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH,

[Continued on next page]

(54) Title: ON-CHIP MEMORY CELL AND METHOD OF MANUFACTURING SAME

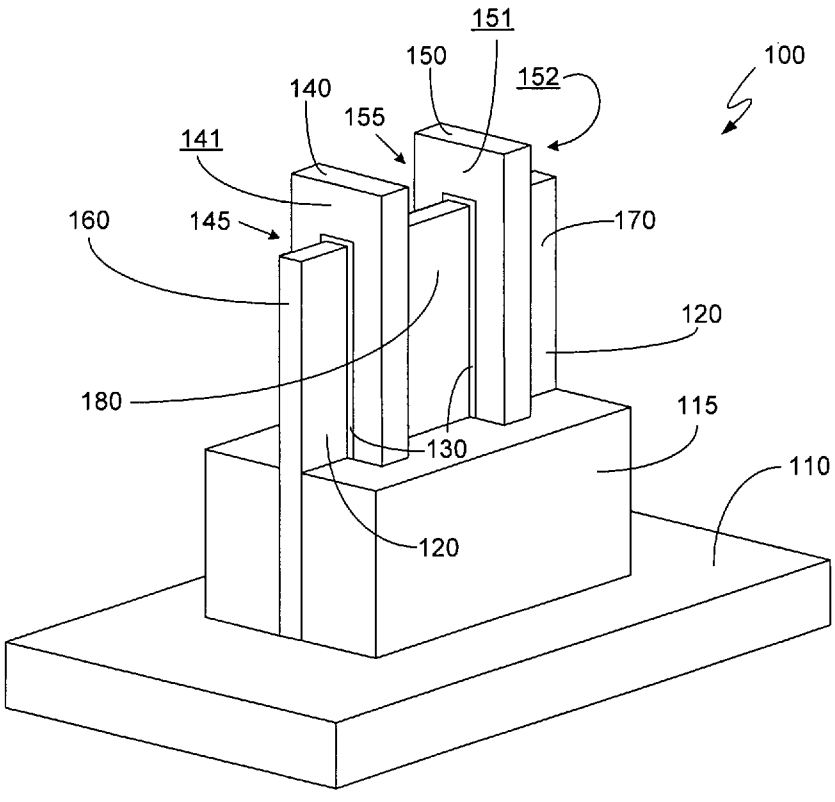

FIG. 1

(57) Abstract: An on-chip memory cell comprises a tri-gate access transistor (145) and a tri-gate capacitor (155). The on-chip memory cell may be an embedded DRAM on a three-dimensional tri-gate transistor and capacitor structures which is fully compatible with existing tri-gate logic transistor fabrication process. Embodiments of the invention use the high fin aspect ratio and inherently superior surface area of the tri-gate transistors to replace the "trench" capacitor in a commodity DRAM with an inversion mode tri-gate capacitor. The tall sidewalls of the tri-gate transistor provide large enough surface area to provide storage capacitance in a small cell area.

WO 2008/118811 A1

GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*