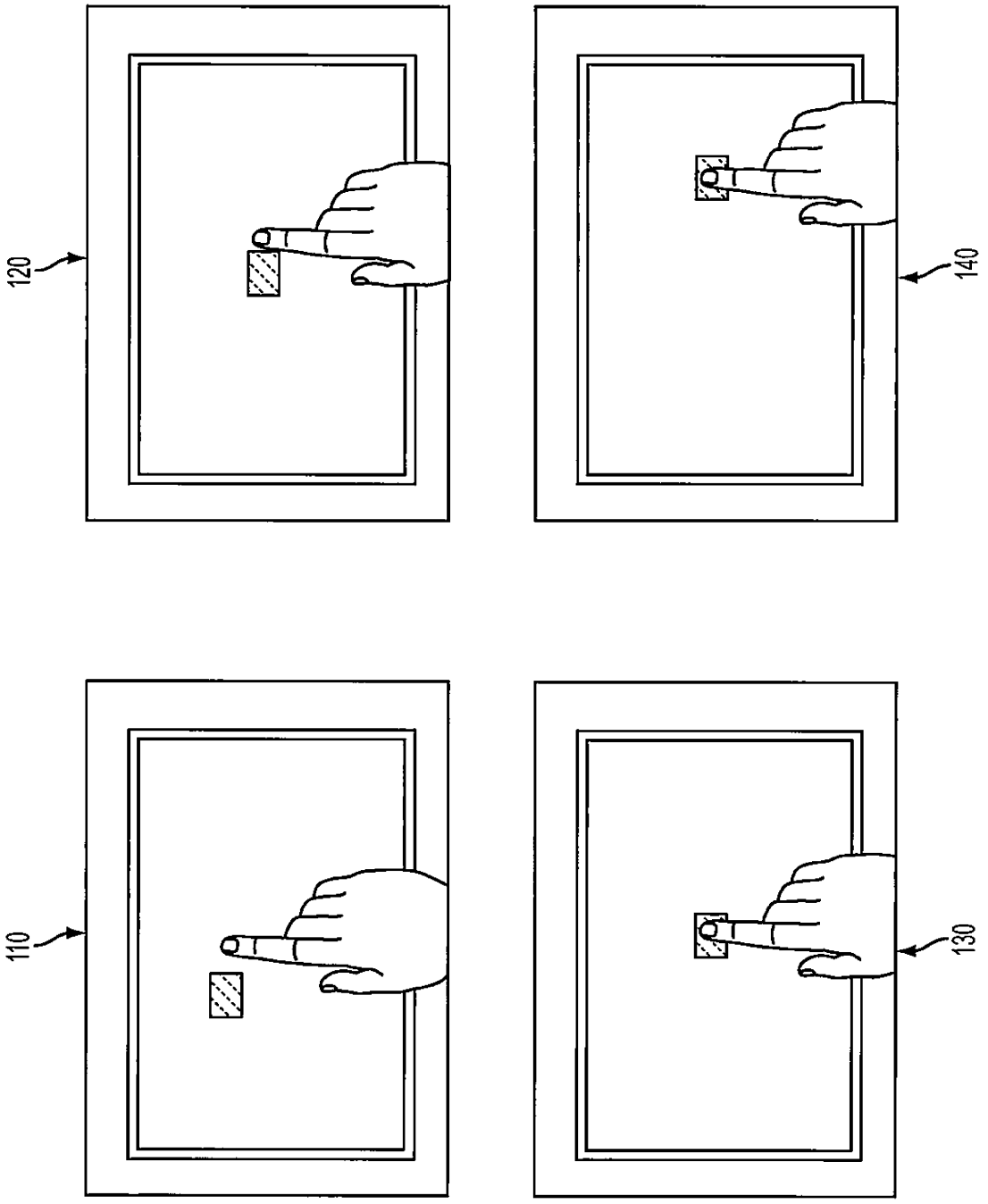

FIG. 1

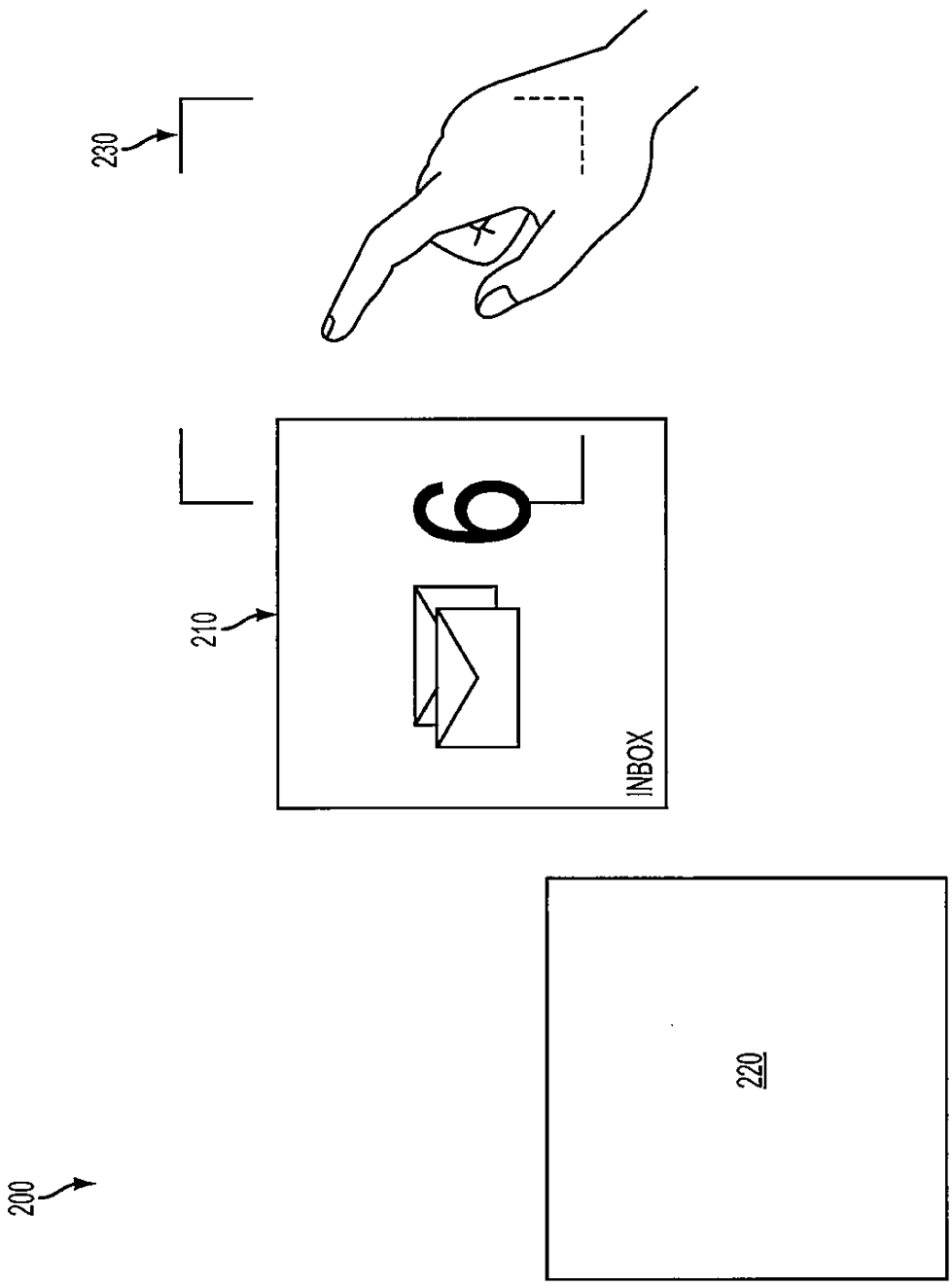

FIG. 2

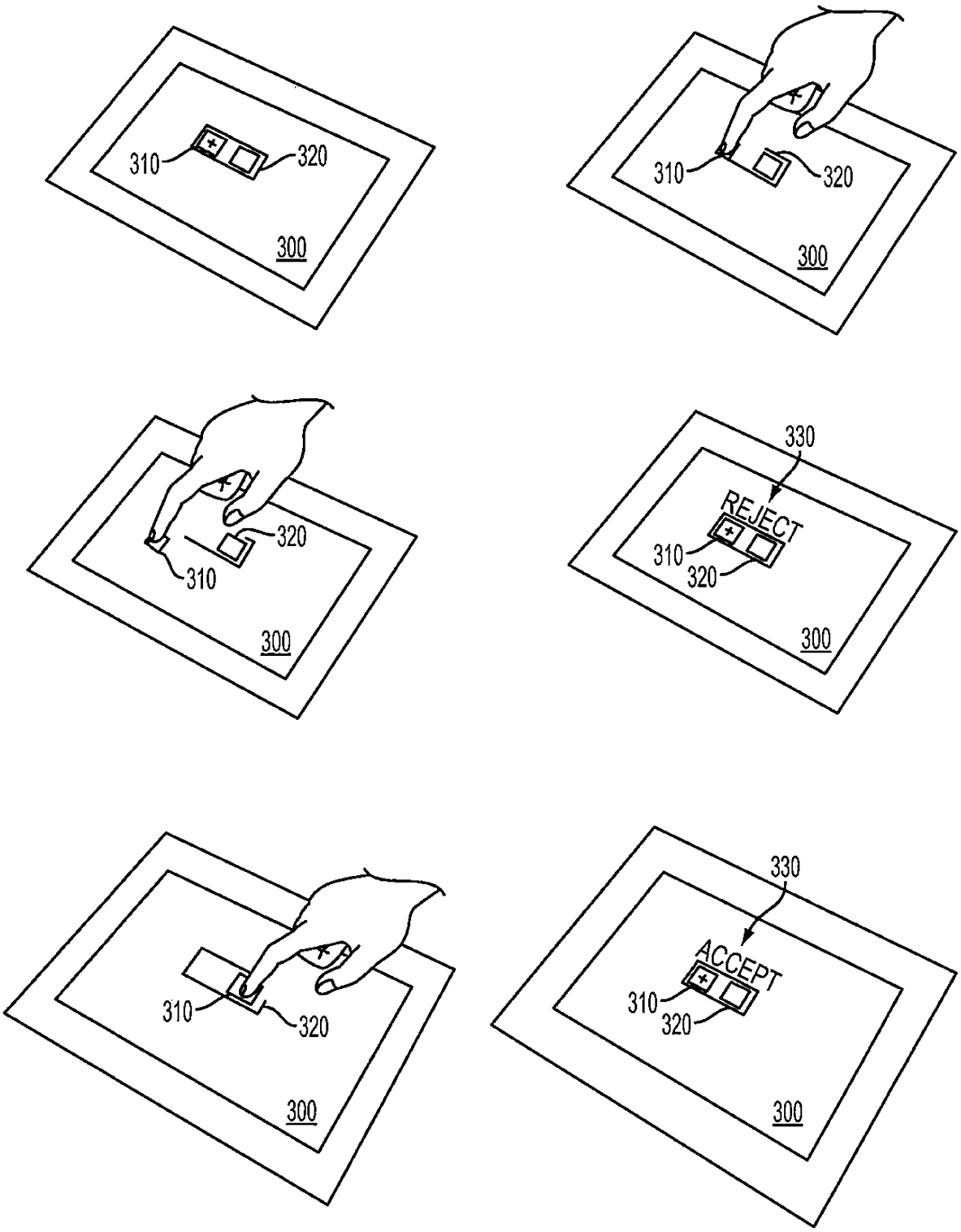
310
320
300
310
320
300
320
310
300
330
REJECT
310
320
300
310
320
300
330
ACCEPT
310
320
300

FIG. 3

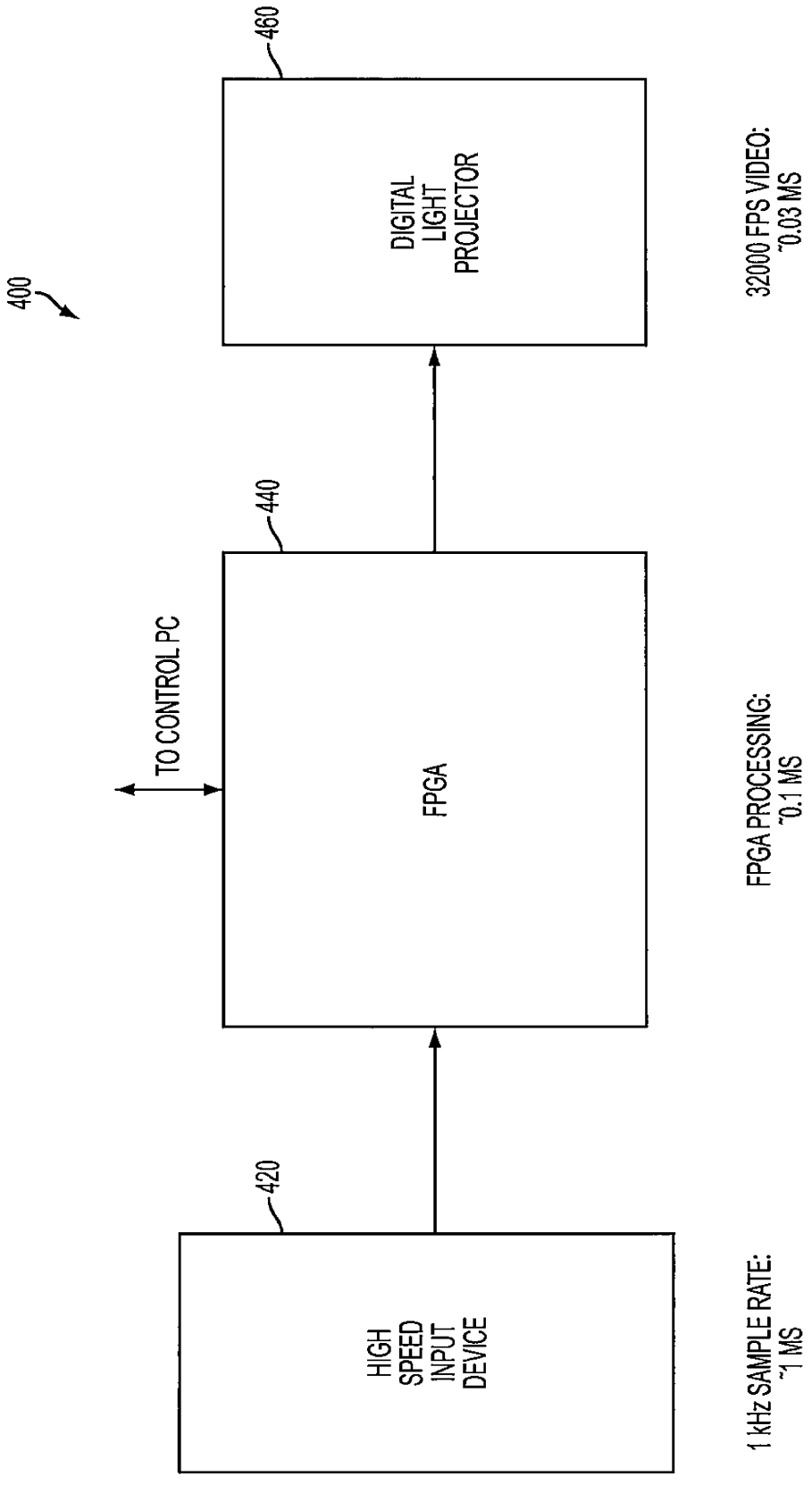
400
460
DIGITAL LIGHT PROJECTOR
32000 FPS VIDEO: ~0.03 MS
440
TO CONTROL PC
FPGA
FPGA PROCESSING: ~0.1 MS
420
HIGH SPEED INPUT DEVICE
1 kHz SAMPLE RATE: ~1 MS

FIG. 4

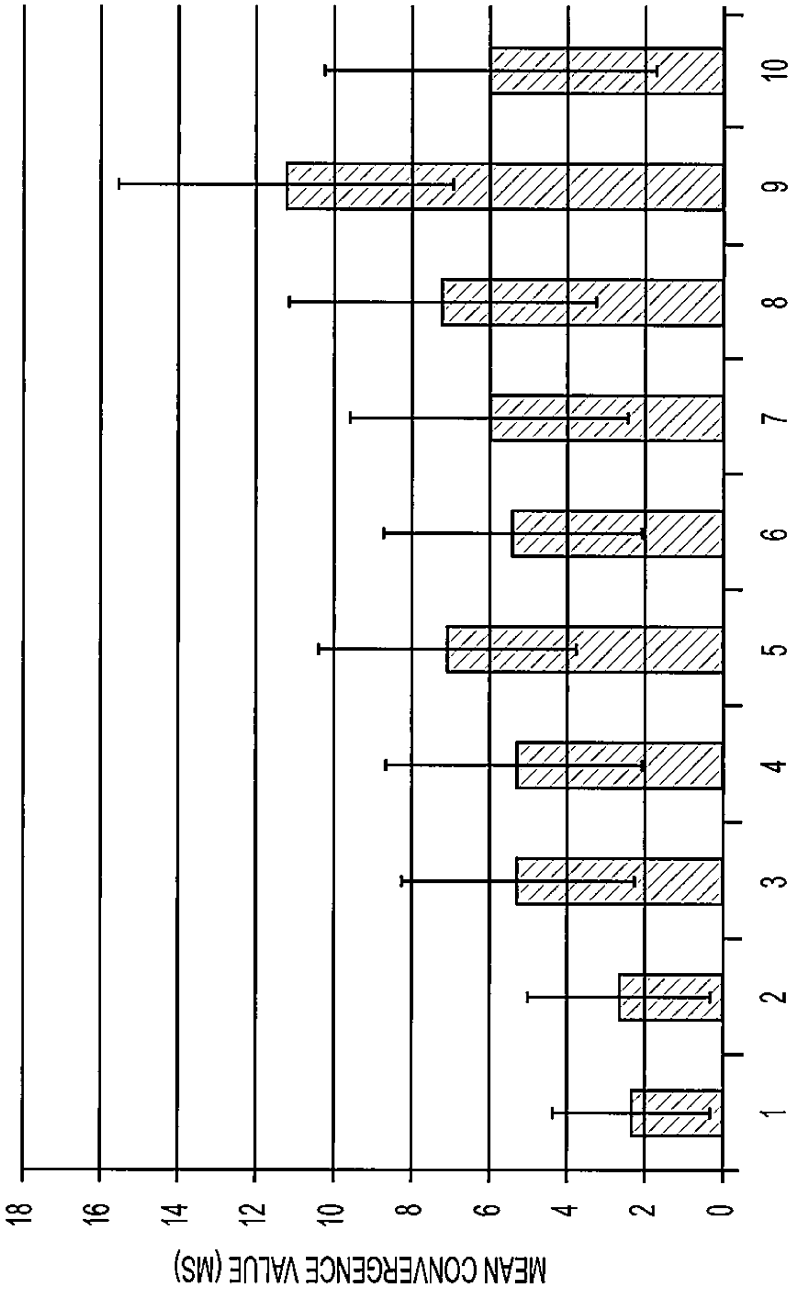
MEAN CONVERGENCE VALUE (MS)
0
2
4
6
8
10
12
14
16
18
PARTICIPANT
1
2
3
4
5
6
7
8
9
10

FIG. 5

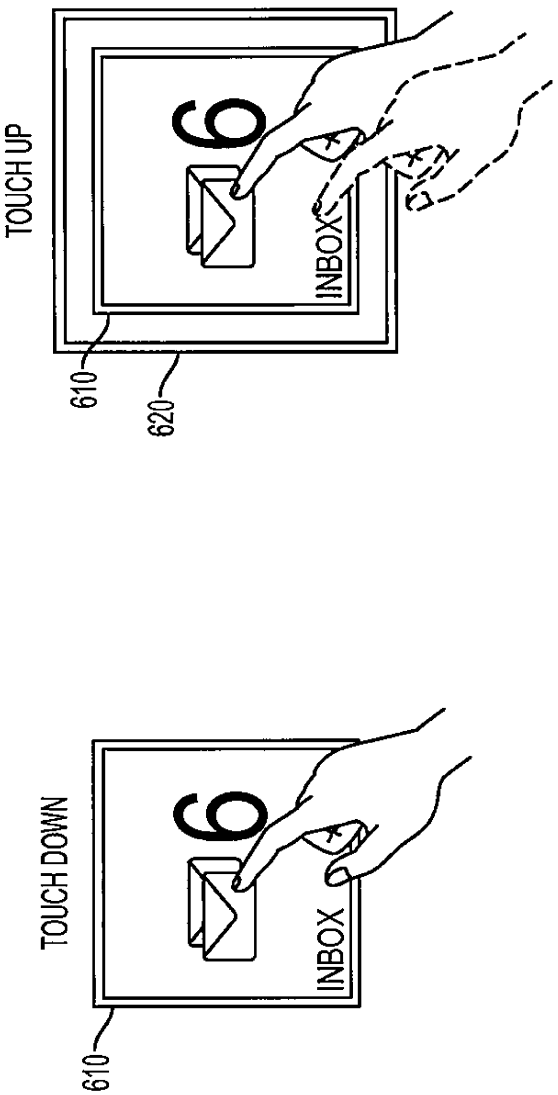

FIG. 6

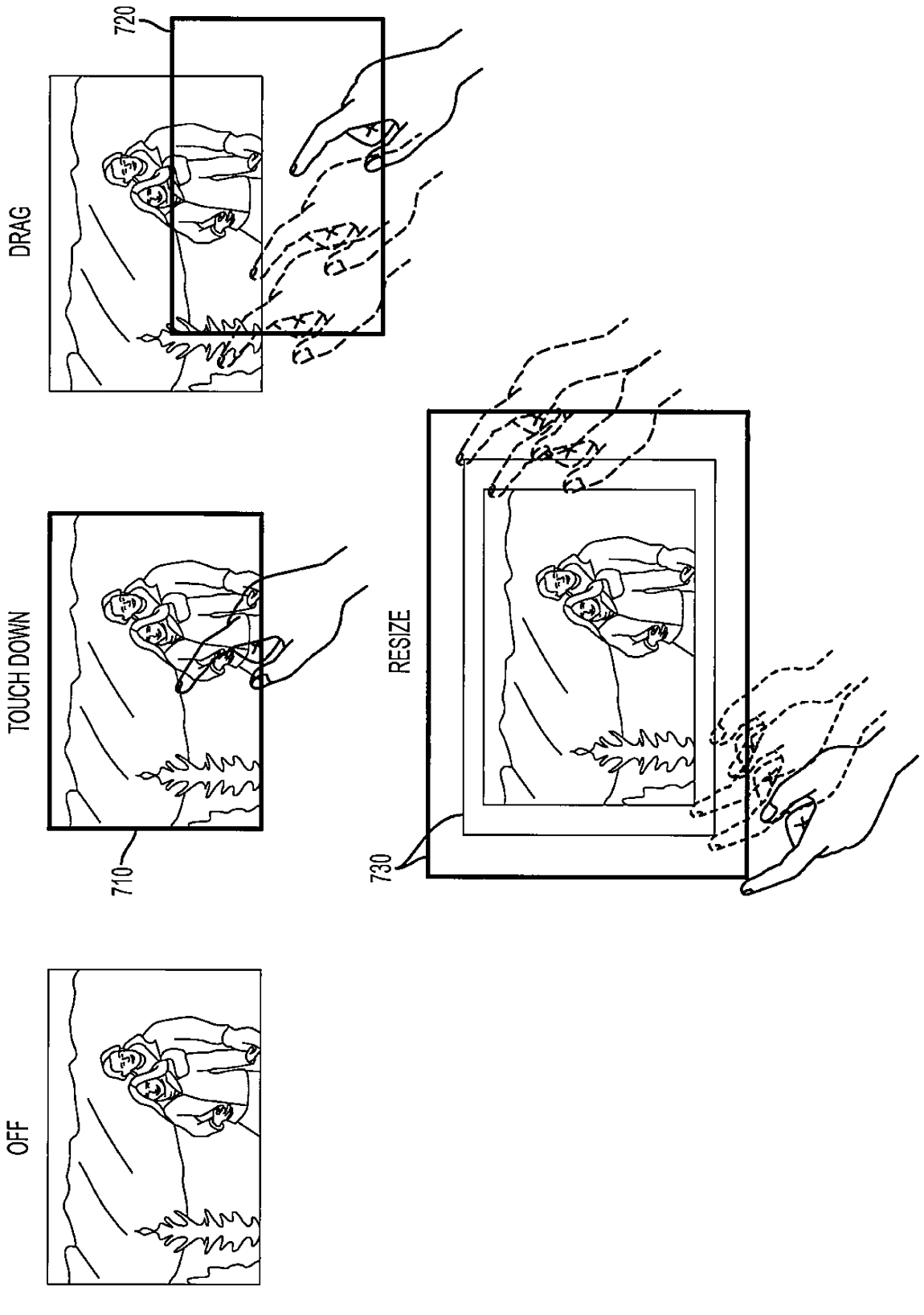

FIG. 7

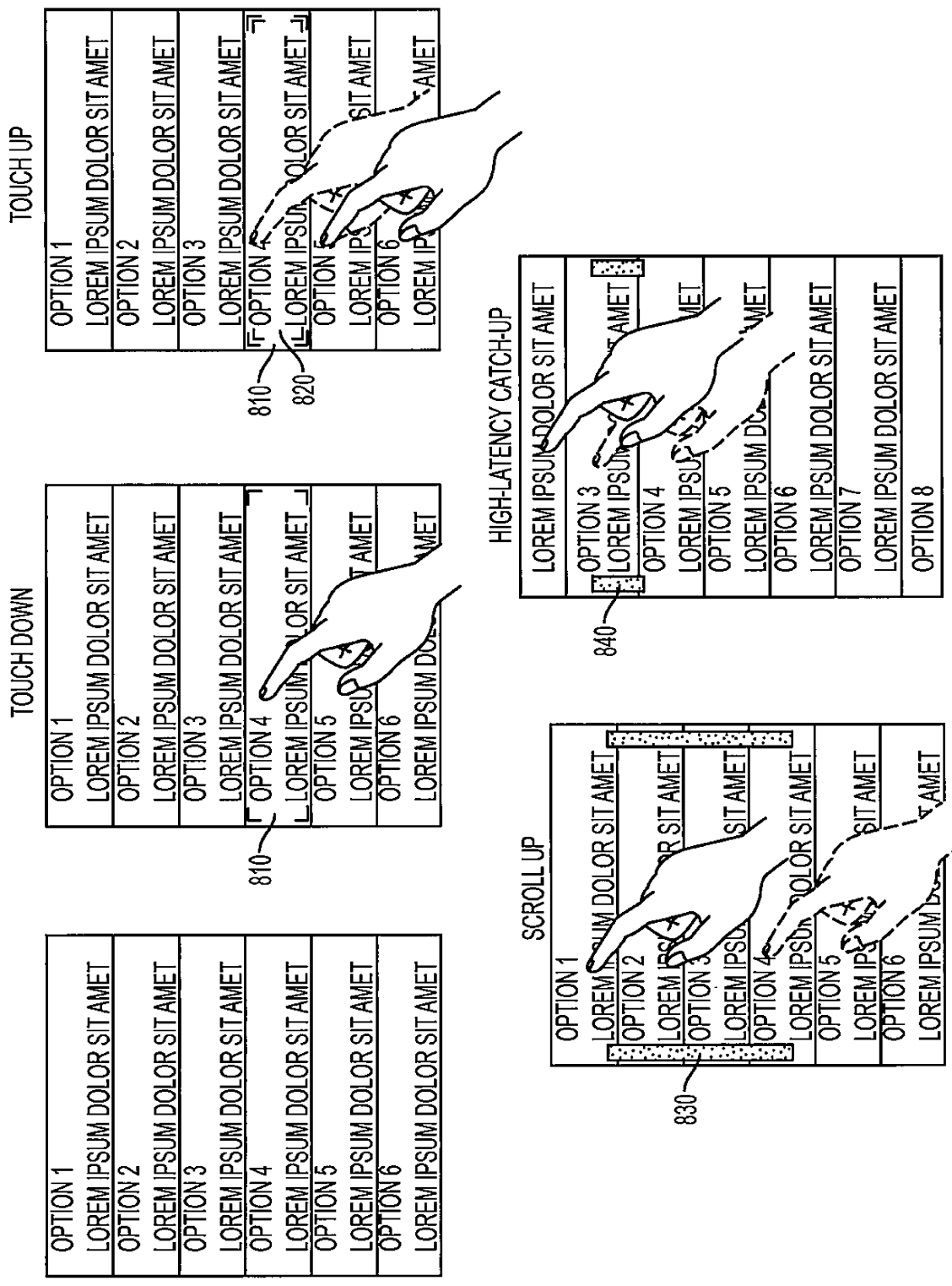
TOUCH UP
TOUCH DOWN
HIGH-LATENCY CATCH-UP
SCROLL UP
OPTION 1
LOREM IPSUM DOLOR SIT AMET
OPTION 2
OPTION 3
OPTION 4
OPTION 5
OPTION 6
OPTION 7
OPTION 8
810
820
830
840

FIG. 8

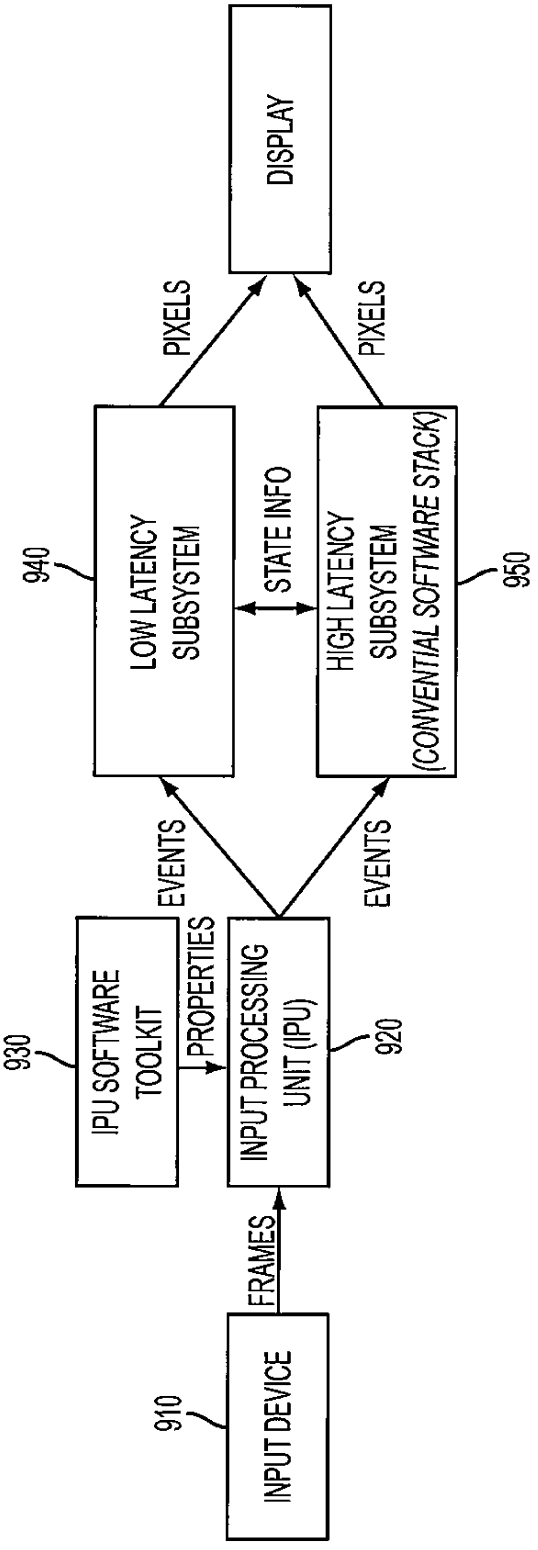
DISPLAY
PIXELS
PIXELS
940
LOW LATENCY SUBSYSTEM
STATE INFO
HIGH LATENCY SUBSYSTEM (CONVENTIAL SOFTWARE STACK)
950
EVENTS
EVENTS
930
IPU SOFTWARE TOOLKIT
PROPERTIES
INPUT PROCESSING UNIT (IPU)
920
FRAMES
910
INPUT DEVICE

FIG. 9

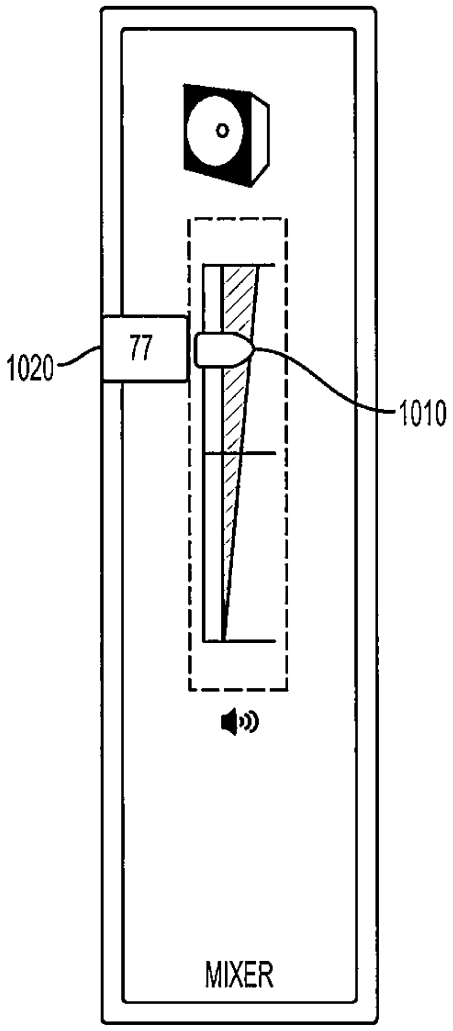

FIG. 10

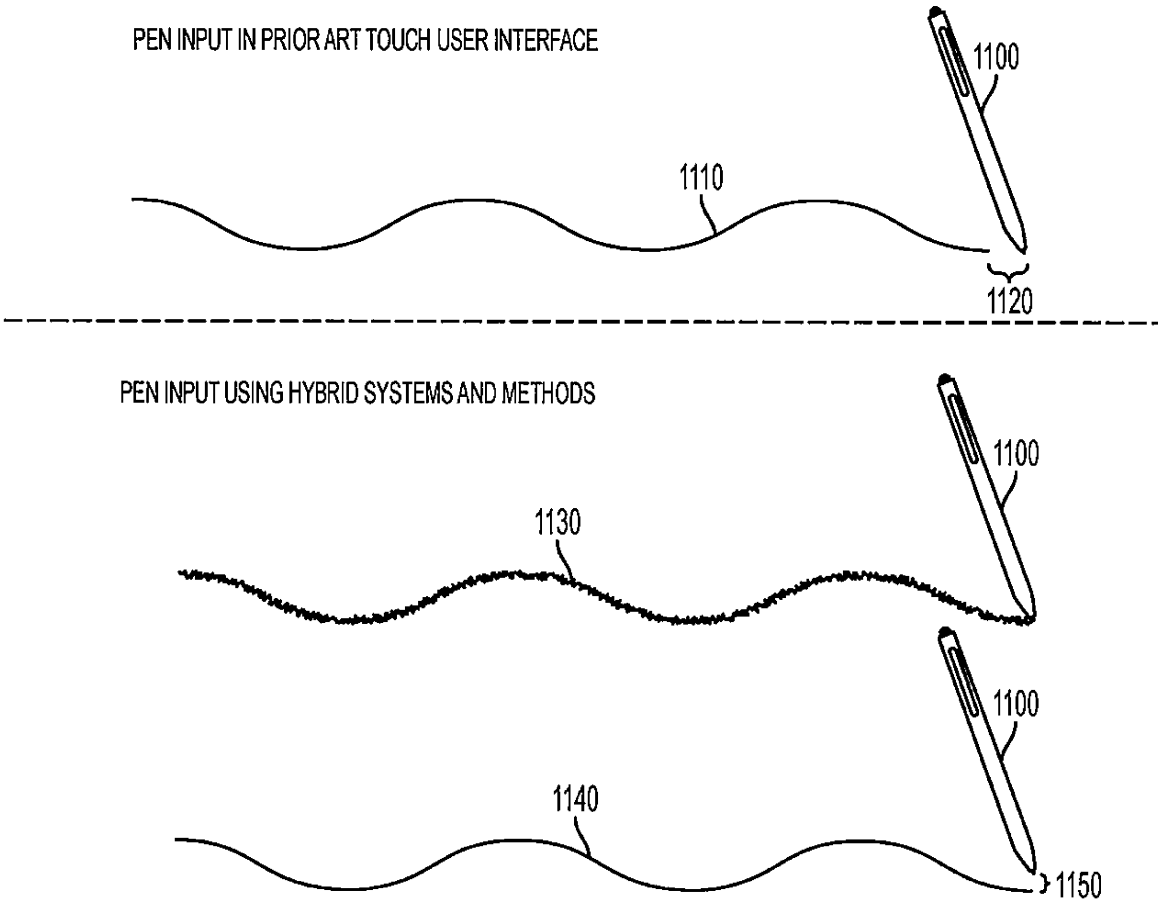
PEN INPUT IN PRIOR ART TOUCH USER INTERFACE
1100
1110
1120
PEN INPUT USING HYBRID SYSTEMS AND METHODS
1100
1130
1100
1140
1150

FIG. 11

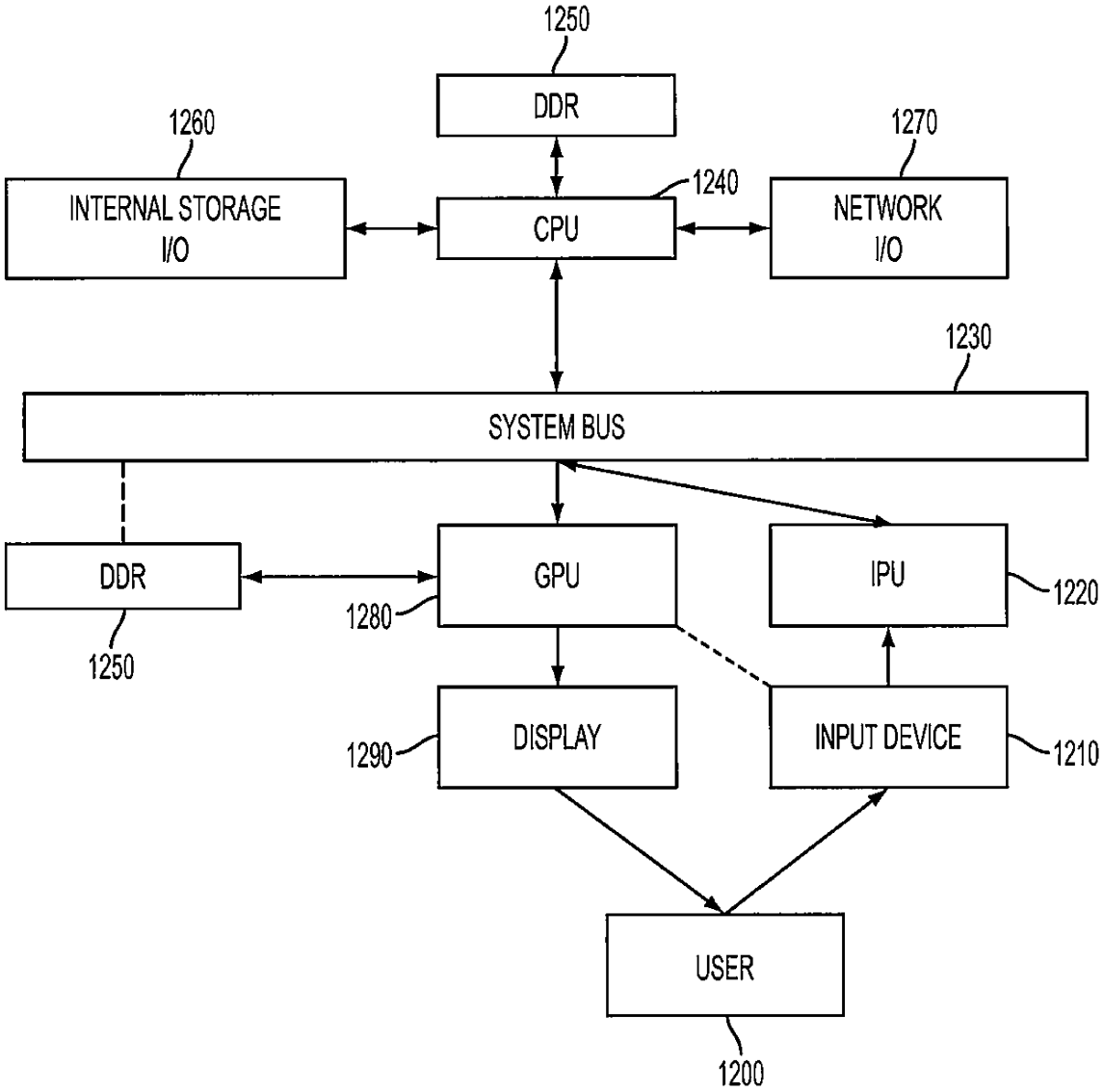
1250
DDR
1260
INTERNAL STORAGE I/O
1240
CPU
1270
NETWORK I/O
1230
SYSTEM BUS
DDR
1250
GPU
1280
IPU
1220
DISPLAY
1290
INPUT DEVICE
1210
USER
1200

FIG. 12

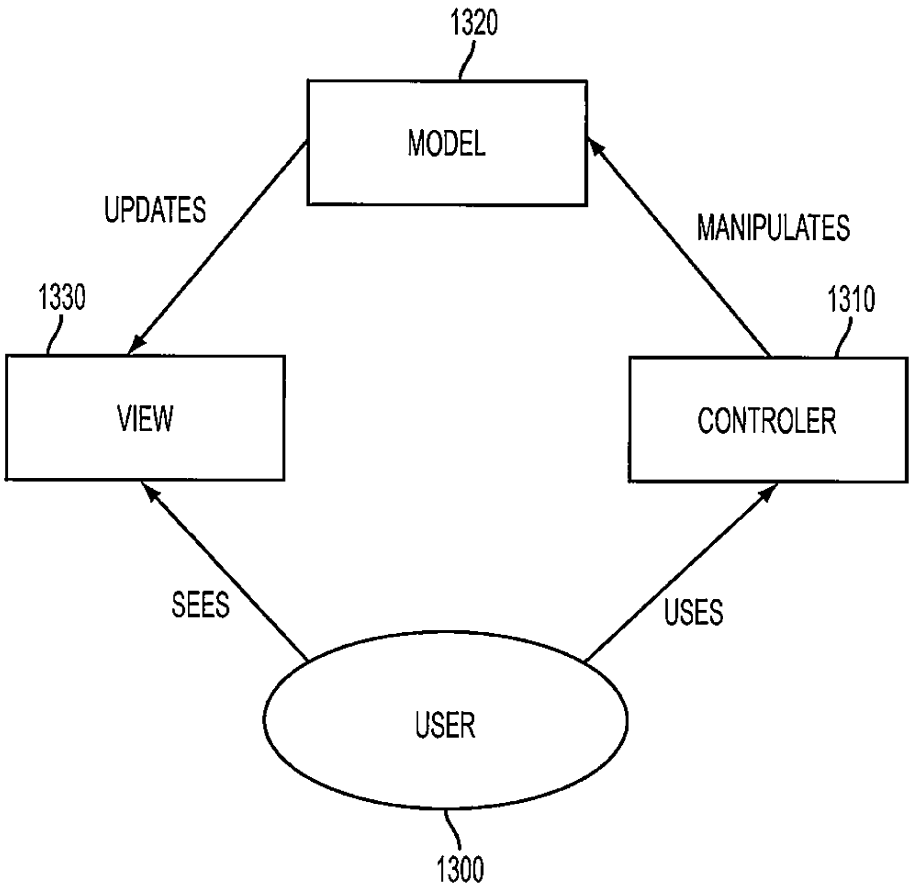
1320
MODEL
UPDATES
MANIPULATES
1330
1310
VIEW
CONTROLER
SEES
USES
USER
1300

FIG. 13

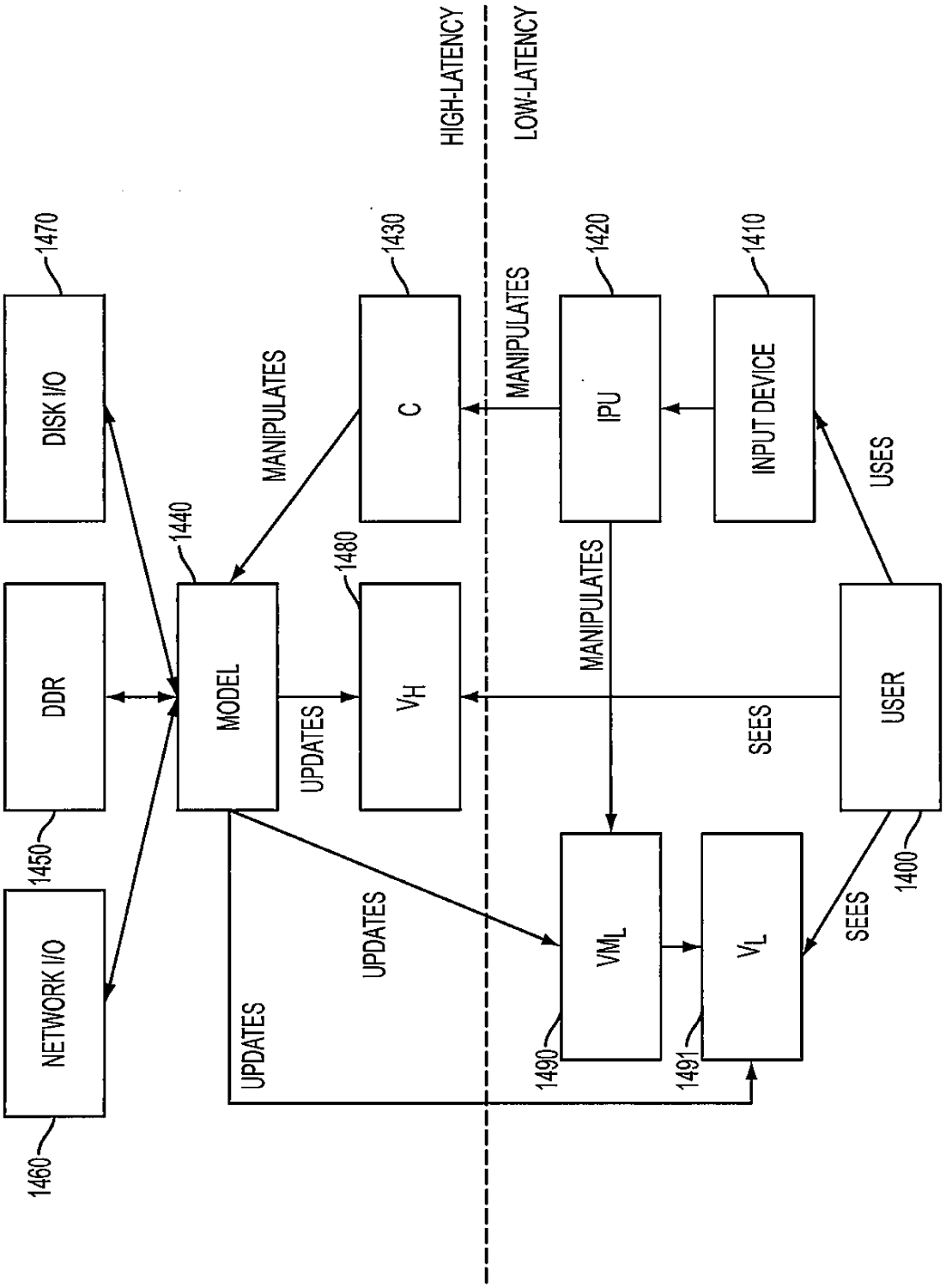
HIGH-LATENCY
LOW-LATENCY
1470
DISK I/O
1450
DDR
1460
NETWORK I/O
1440
MODEL
1480
V_H
1430
C
1420
IPU
1410
INPUT DEVICE
1490
VM_L
1491
V_L
1400
USER
MANIPULATES
MANIPULATES
MANIPULATES
USES
UPDATES
UPDATES
UPDATES
SEES
SEES

FIG. 14