CLAIMS

1. A method for comparing execution of a plurality of processing systems of a device, comprising: comparing execution of a program on a first processing system of the plurality of processing systems and execution of the program on a second processing system of the plurality of processing systems using a first comparator circuit; comparing the execution of the program on the first processing system and the execution of the program on the second processing system using a second comparator circuit; and running a diagnosis program, configured to diagnose a failure of the second comparator circuit, on the second comparator circuit while the comparing using the first comparator circuit is ongoing.

2. The method of claim 1, further comprising: running the diagnosis program or another diagnosis program on the first comparator circuit while the comparing using the second comparator circuit is ongoing.

3. The method of claim 1, further comprising: disabling the second comparator circuit prior to running the diagnosis program; and enabling the second comparator circuit subsequent to running the diagnosis program.

4. The method of claim 1, wherein comparing the execution of the program on the first processing system and the execution of the program on the second processing system comprises comparing first outputs written to a memory by the first processing system with second outputs written to the memory by the second processing system.

5. The method of claim 1, wherein comparing the execution of the program on the first processing system and the execution of the program on the second processing system comprises comparing first outputs transmitted via one or more buses by the first processing system with second outputs transmitted via one or more buses by the second processing system.

6. The method of claim 5, wherein the one or more buses comprise at least one of an advanced extensible interface (AXI) bus or an accelerator coherency port (ACP) bus.

7. The method of claim 1, wherein: comparing the execution of the program on the first processing system and the execution of the program on the second processing system using the first comparator circuit comprises comparing first outputs of the first processing system with second outputs of the second processing system; and comparing the execution of the program on the first processing system and the execution of the program on the second processing system using the second comparator circuit comprises comparing third outputs, of the first processing system, that are different from the first outputs with fourth outputs, of the second processing system, that are different from the second outputs.

8. The method of claim 1, wherein: the first processing system comprises a first core of a multi-core processor; and the second processing system comprises a second core of the multi-core processor.

9. The method of claim 1, wherein: the first processing system comprises a first processor of the device; and the second processing system comprises a second processor of the device.

10. The method of claim 1, wherein the diagnosis program detects a fault in the second comparator circuit, and the method further comprises: outputting an indication that the device has the fault and is operating safely.

11. The method of claim 1, wherein: comparing the execution of the program on the first processing system and the execution of the program on the second processing system using the first comparator circuit comprises comparing outputs, from the first processing system and the second processing system, that control another device; and comparing the execution of the program on the first processing system and the execution of the program on the second processing system using the second comparator circuit comprises: comparing the outputs, from the first processing system and the second processing system, that control the other device, and comparing other outputs from the first processing system with corresponding other outputs from the second processing system.

12. An apparatus, comprising: a first processing system; a second processing system; a first comparator circuit operable to compare execution of a program on the first processing system and execution of the program on the second processing system; and a second comparator circuit operable to compare the execution of a program on the first processing system and the execution of the program on the second processing system and to run a diagnosis program, configured to diagnose a failure of the second comparator circuit, while the first comparator circuit is comparing the execution of the program on the first processing system and the execution of the program on the second processing system.

13. The apparatus of claim 12, wherein the first comparator circuit is operable to run the diagnosis program or another diagnosis program while the second comparator circuit is comparing the execution of the program on the first processing system and the execution of the program on the second processing system.

14. The apparatus of claim 12, wherein the second comparator circuit is operable to be disabled prior to running the diagnosis program and operable to be enabled subsequent to running the diagnosis program.

15. The apparatus of claim 12, wherein: the first comparator circuit is configured to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing first outputs written to a memory by the first processing system with second outputs written to the memory by the second processing system; and the

second comparator circuit is configured to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing the first outputs with the second outputs.

16. The apparatus of claim 12, wherein: the first comparator circuit is configured to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing first outputs transmitted via one or more buses by the first processing system with second outputs transmitted via one or more buses by the second processing system; and the second comparator circuit is configured to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing the first outputs with the second outputs.

17. The apparatus of claim 16, wherein the one or more buses comprise at least one of an advanced extensible interface (AXI) bus or an accelerator coherency port (ACP) bus.

18. The apparatus of claim 12, wherein: the first comparator circuit is configured to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing first outputs of the first processing system with second outputs of the second processing system; and the second comparator circuit is configured to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing third outputs, of the first processing system, that are different from the first outputs and fourth outputs, of the second processing system, that are different from the second outputs.

19. The apparatus of claim 12, wherein: the first processing system comprises a first core of a multi-core processor; and the second processing system comprises a second core of the multi-core processor.

20. The apparatus of claim 12, wherein: the first processing system comprises a first processor of the apparatus; and the second processing system comprises a second processor of the apparatus.

21. The apparatus of claim 12, wherein: at least one of the first processing system, the second processing system, the first comparator circuit, and the second comparator circuit is operable to detect a fault in the second comparator circuit based on the second comparator circuit running the diagnosis program; and at least one of the first processing system and the second processing system is operable to output an indication that the apparatus has the fault and is operating safely.

22. The apparatus of claim 12, wherein: the first comparator circuit is operable to compare the execution of the program on the first processing system and the execution of the program on the second processing system by comparing outputs, from the first processing system and the second processing system, that control a device; and the second comparator circuit is operable to compare the execution of the program on the first processing system and the execution of the program on the second processing system by: comparing the outputs, from the first processing

system and the second processing system, that control the device, and comparing other outputs from the first processing system with corresponding other outputs from the second processing system.

23. An apparatus, comprising: first means for processing; second means for processing; first means for comparing execution of a program on the first means for processing and execution of the program on a second means for processing; second means for comparing the execution of the program on the first means for processing and the execution of the program on the second means for processing; and means for running a diagnosis program, configured to diagnose a failure of the second means for comparing, on the second means for comparing while the first means for comparing is comparing the execution of the program on the first means for processing and the execution of the program on the second means for processing.

24. The apparatus of claim 23, further comprising: means for running the diagnosis program or another diagnosis program on the first means for comparing while the second means for comparing is comparing the execution of the program on the first means for processing and the execution of the program on the second means for processing.

25. The apparatus of claim 23, further comprising: means for disabling the second means for comparing prior to running the diagnosis program; and means for enabling the second means for comparing subsequent to running the diagnosis program.

26. The apparatus of claim 23, wherein: the first means for comparing comprises means for comparing first outputs written to a memory by the first means for processing with second outputs written to the memory by the second means for processing; and the second means for comparing comprises means for comparing the first outputs with the second outputs.

27. The apparatus of claim 23, wherein: the first means for comparing comprises means for comparing first outputs transmitted via one or more buses by the first means for processing with second outputs transmitted via one or more buses by the second means for processing; and the second means for comparing comprises means for comparing the first outputs with the second outputs.

28. The apparatus of claim 27, wherein the one or more buses comprise at least one of an advanced extensible interface (AXI) bus or an accelerator coherency port (ACP) bus.

29. The apparatus of claim 23, wherein: the first means for comparing comprises means for comparing first outputs of the first means for processing with second outputs of the second means for processing; and the second means for comprises means for comparing third outputs, of the first processing system, that are different from the first outputs with fourth outputs, of the second processing system, that are different from the second value outputs.

30. The apparatus of claim 23, wherein: the first means for processing comprises a first core of a multi-core processor; and the second means for processing comprises a second core of the multi-core processor.

31. The apparatus of claim 23, wherein: the first means for processing comprises a first processor of the apparatus; and the second means for processing comprises a second processor of the apparatus.

32. The apparatus of claim 23, wherein: at least one of the first means for processing, the second means for processing, the first means for comparing, and the second means for comparing comprises means for detecting a fault in the second means for comparing based on the second means for comparing running the diagnosis program; and at least one of the first means for processing and the second means for processing comprises means for outputting an indication that the apparatus has the fault and is operating safely.

33. The apparatus of claim 23, wherein: the first means for comparing comprises means for comparing outputs, from the first means for processing and the second means for processing, that control another device; and the second means for comparing comprises: means for comparing the outputs, from the first means for processing and the second means for processing, that control the other device, and means for comparing other outputs from the first means for processing with corresponding other outputs from the second means for processing.

34. A non-transitory computer-readable medium comprising instructions, the instructions when executed by one or more processing systems cause the one or more processing systems to perform operations comprising: comparing execution of a program on a first processing system of the plurality of processing systems and execution of the program on a second processing system of the plurality of processing systems using a first comparator circuit; comparing the execution of the program on the first processing system and the execution of the program on the second processing system using a second comparator circuit; and running a diagnosis program, configured to diagnose a failure of the second comparator circuit, on the second comparator circuit while the comparing using the first comparator circuit is ongoing.