"A semiconductor memory device". 2150750

The present invention relates to a semiconductor memory device, and more particularly to a technique which is effective when applied to a dynamic random access memory (DRAM).

Each memory cell of a DRAM consists of a storage capacitor and a switching MISFET. The storage capacitor is constructed of a capacitor of the MIS type. Specifically, it is constructed of a semiconductor substrate, an insulator film which is formed on the semiconductor substrate, and a capacitor electrode which is formed on the insulator film and to which a predetermined voltage is applied. Charges in a quantity corresponding to the information of "1" or "0" are stored in an inversion layer which is formed within the semicondcutor substrate under the capacitor electrode having the predetermined voltage applied thereto.

For integrating the DRAM at a high packing density, it is effective to make the capacitor small in area while holding a capacitance of certain magnitude.

A DRAM which meets this requirement is disclosed in Japanese Patent Application No. 53883/75. The capacitor of this DRAM is constructed of a trench (also called "U-groove") which is formed so

as to extend from one main surface of a semiconductor substrate inwardly of the same, an insulator film which is formed along the trench, and a capacitor electrode which is formed so as to cover the insulator film.

It holds true, however, that charges are stored in a depletion layer and an inversion layer within the semiconductor substrate.

We have found by experiment that the DRAM composed of memory cells of the type which stores charges in a depletion layer and an inversion layer is not suited for high-density integration.

The memory cell of this type cannot exclude the influence of minority carriers appearing due to α-particles or minority carriers injected from a peripheral circuit portion. Insofar as the charges are stored in the depletion layer and the inversion layer, the quantity of charges fluctuates due to the minority carriers. Accordingly, the occupying area of a storage capacitor cannot be made smaller than a certain value. Since the influence of the minority carriers increases the deeper one goes from the surface of a semiconductor substrate, deepening the trench is not very effective.

Moreover, with the memory cells of the specified type, it is impossible to reduce in size an isolation region for electrically isolating the

adjacent memory cells. The reason is that, since the depletion layers and inversion layers of the capacitors of the adjacent memory cells need to be prevented from coupling, the distance between the memory cells cannot be made smaller than a certain value. In the case where a field oxide film is used as the isolation region, the problem of bird's beak is also involved. Meanwhile, the depletion layer couples to the depletion layer of the adjacent trench more easily in the deep part of the trench than in the shallow part thereof. For this reason, the distance between the trenches cannot be made smaller than a certain value.

It is an object of the present invention to provide a DRAM capable of integration at a higher packing density.

Another object of the present invention is to prevent the leakage of charges between the storage capacitors of the adjacent memory cells of a DRAM, and to reduce the degree of influence of minority carriers in the storage capacitor of the memory cell of a DRAM.

Yet another object of the present invention is to lengthen the data retension time of the storage capacitors of a DRAM, thereby making it possible to enhance the operating speed of the DRAM.

According to the present invention there is provided a semiconductor memory device having memory cell arrays in which memory cells are arranged in the shape of a matrix, said each memory cell comprising a switching element and a first capacitor which is formed on a main surface of a semiconductor substrate of a first conductivity type and which is connected with said switching element, wherein:-

(a) said capacitor comprises a first insulator film which is formed on the main surface of said semiconductor substrate, a first electrode a part of which is electrically connected with said switching element and which is formed on said first insulator film, said first electrode being independent for said each memory cell, and a semiconductor region to serve as a second electrode, which is formed in said semiconductor substrate under said first insulator film and which has the first conductivity type and an impurity concentration higher than that of said semiconductor substrate; and

(b) the semiconductor regions of one memory cell and at least one of the memory cells which adjoin said one memory cell within the identical memory cell array are formed commonly.

The capacitor may be formed within a groove, the groove being formed by removing the

the semiconductor substrate from the main surface thereof inwardly. The semiconductor region may be formed in the main surface of the semiconductor substrate and a surface of the groove.

The semiconductor memory device may include a second capacitor which is formed on the first capacitor, the second capacitor comprising the first electrode, a second insulator film which is formed on at least the first electrode, and a third electrode which is formed on at least the second insulator film.

The present invention will now be described in greater detail by way of examples with reference to the accompanying drawings, wherein:-

Figure 1 is an equivalent circuit diagram to illustrate the essential portions of the memory cell array of a DRAM for explaining an embodiment of the present invention;

Figure 2A is a plan view of the essential portions of a DRAM memory cell which forms a first embodiment of the present invention;

Figure 2B is a sectional view taken along line II-II in Figure 2A;

Figures 3A and 3B are graphs for explaining the principle of the present invenion;

Figures 4A, 5A, 6A, 7A and 8A are plan views of the essential portions of the DRAM memory cell illustrating the manufacturing steps of the DRAM shown in Figures 2A and 2B;

Figures 4B, 5B, 6B, 7B and 8B are sectional views taken along cutting-plane lines indicated in Figures 4A, 5A, 6A, 7A and 8A, respectively;

Figure 5C is a plan view showing the manufacturing steps of a memory cell array in the DRAM of Figures 2A and 2B;

Figure 9A is a plan view of the essential portions of a DRAM memory cell which forms a second embodiment of the present invention;

Figure 9B is a sectional view taken along line IX - IX in Figure 9A;

Figure 10 is a plan view of the essential portions of a schematic memory cell array in the DRAM shown in Figures 9A and 9B;

Figures 11A and 12A are plan views of the essential portions of the DRAM memory cell illustrating the manufacturing steps of the DRAM shown in Figures 9A and 9B;

Figs. 11B and 12B are sectional views taken along cutting-plane lines indicated in Figures 11A and 12A, respectively;

Figures 13, 14 and 15 are plan views of the essential portions of a memory cell array illustrating the manufacturing steps of a DRAM memory cell which forms a third embodiment of the present invention;

Figure 16A is a plan view of the essential portions of a DRAM memory cell which forms a fourth embodiment of the present invention;

Figure 16B is a sectional view taken along line XVI - XVI in Figure 16A;

Figures 17A, 18A, 20A, 21A, 22A and 23A are plan views of the essential portions of the memory cell illustrating the various manufacturing

steps of the DRAM shown in Figures 16A and 16B;

Figures 17B, 18B, 20B, 21B 22B and 23B are sectional views taken along cutting-plane lines indicated in Figures 17A, 18A, 20A, 21A, 22A and 23A respectively;

Figure 19 is a plan view showing an intermediate state in the manufacturing process of the DRAM shown in Figures 16A and 16B;

Figure 24A is a plan view of the essential portions of a DRAM memory cell which forms a fifth embodiment of the present invention;

Figure 24B is a sectional view taken along line XXIV - XXIV in Figure 24A;

Figure 25 is a plan view of the essential portions of a schematic memory cell array in the DRAM shown in Figures 24A and 24B; and

Figures 26, 27 and 28 are plan views showing the manufacturing steps of a DRAM memory cell which forms a sixth embodiment of the present invention.

Referring first to Figure 1, the memory cell array of a DRAM includes: sense amplifiers SA1, SA2....., each of which serves to amplify the minute potential difference between a predetermined memory cell and a predetermined dummy cell to be described later; bit lines BL11 and BL12 which extend in the row direction from one side end of the sense

amplifier SA_1; bit lines BL_{21} and BL_{22} which extend in the row direction from one side end of the sense amplifier SA_2. These bit lines BL serve to transmit charges as information. The memory cell array also includes word lines WL_1 and WL_2 which extend in the column direction and word lines WL_3 and WL_4 which also extend in the column direction. The word lines WL_1 and WL_2 are connected to predetermined gate electrodes which constitute the switching MISFETs of the dummy cells to be described later, and they serve to turn "on" and "off" these MISFETs. The word lines WL_3 and WL_4 are connected to predetermined gate electrodes which constitute the switching MISFETs of the memory cells to be described later, and they serve to turn "on" and "off" these MISFETs. The memory cell array further includes memory cells M_{11}, M_{12}, M_{21}, M_{22}, ... which hold the charges serving as the information. The memory cells M_{11}, M_{12}, M_{21}, M_{22}, ... are respectively constituted by MISFETs Q_{11}, Q_{12}, Q_{21}, Q_{22}, ... one end of each MISFET being connected to the predetermined bit line BL and the gate electrode of each MISFET being connected to the predetermined word line WL; and capacitors C_{11}, C_{12}, C_{21}, C_{22}, ... one end of each capacitor being connected to the other end of the respective MISFETs Q_{11}, Q_{12}, Q_{21}, Q_{22}, ... and the other end of each capacitor being connected to a fixed potential

V_{SS} such as earth potential (0 V) or a substrate back bias potential (-2.5 to - 3.0 V). The memory cell array also includes dummy cells D_{11}, D_{12}, D_{21}, D_{22}, ... which holds charges permitting the judgement of "1" and "0" that are the information of the memory cells M. The dummy cells D_{11}, D_{12}, D_{21}, D_{22}, ... are respectively constituted by MISFETs Q_{D11}, Q_{D12}, Q_{D21}, Q_{D22}, ... one end of which each MISFET being connected to the predetermined bit line BL and the gate electrode of each MISFET being connected to the predetermined word line WL; capacitors C_{D11}, C_{D12}, C_{D21}, C_{D22}, ... one end of each capacitor being connected to the other end of respective MISFETs Q_{D11}, Q_{D12}, Q_{D21}, Q_{D22},... and the other end of each capacitor being connected to the terminal of the fixed potential V_{SS}; and a clearing MISFET CQ which serves to clear the charges stored in the capacitors C_{D11}, C_{D12}, C_{D21}, C_{D22}, ... A terminal ϕ_D is connected with the gate electrode of the clearing MISFET CQ.

The structure of the first embodiment of the present invention will be described with reference to Figures 2A and 2B.

The DRAM memory cell includes a p^--type semiconductor substrate 1, which serves to constitute the DRAM; and a field oxide film 2 which is formed on the main surface portion of the semiconductor substrate 1 so as to be located

among predetermined memory cells and among semiconductor elements constituting peripheral circuits (not shown), for example, an address selecting circuit, a reading circuit and a writing circuit, and which serves to electrically isolate them. The memory cells are surrounded with and defined by the field oxide films 2 so that the pattern of one pair of memory cells may be repeated in the direction in which a bit line 15 to be described later extends (hereinafter called "row direction"). The insulator films 2 are indicated by dotted lines. No insulator film 2 exists between the memory cells which adjoin each other in the row direction.

The DRAM memory cell also includes an insulator film 3 which is provided on the main surface portion of the semiconductor substrate 1 in at least an area for forming a storage capacitor, and which serves to constitute the dielectric of the storage capacitor. Charges, for example, holes are stored by the first electrode of the capacitor (hereinafter termed "first conductive plate") and the second electrode of the capacitor (hereinafter termed "Second conductive plate") to be described later, with the insulator film 3 interposed therebetween.

A p^+-type semiconductor region 4 serves as the second conductive plate, which is provided in the surface of the semiconductor substrate 1 in the

area for forming the storage capacitor and which is provided integrally with the storage capacitors adjacent in the row direction. It serves to constitute the storage capacitor C and simultaneously to electrically isolate the storage capacitors adjacent in the row direction. The p^+-type semiconductor region 4 is provided in order that the charges of holes or the charges of a depletion layer to be stored in the capacitor with the insulator film 3 interposed between this region 4 and the first conductive plate may be obtained in as great a number as possible, or that a threshold voltage higher than a voltage which is applied to the first conductive plate to be described later may be provided in the vicinity of the surface of the semiconductor substrate 1. The semiconductor region 4 serves also to suppress the stretch of the depletion layer which is formed, upon the application of the voltage to the first conductive plate, so as to extend from the underlying surface portion of the semiconductor substrate 1 inwardly of this semiconductor substrate. The semiconductor region 4 has an impurity concentration higher than that of the semiconductor substrate 1. The p^+-type semiconductor region 4 should desirably be located apart from an n^+-type semiconductor region to be described later. This is intended to avoid lowering in the breakdown voltage of a junction.

(57)

A contact hole 5 serves for electrically connecting the first conductive plate 7 to be described later and one semiconductor region 6 or 12 of a MISFET Q. The n^+-type semiconductor region 6 is formed in the surface of the semiconductor substrate 1 corresponding to the contact hole 5, and serves to electrically connect the first conductive plate to be described later and one semiconductor region of the MISFET Q.

The first conductive plate 7 is provided on the insulator film 3 in the storage capacitor forming area independently for each memory cell, in such a manner that one end part thereof is electrically connected through the contact hole 5 and the semiconductor region 6 with one semiconductor region of the MISFET Q to be described later. The first conductive plate 7 serves to constitute the storage capacitor C. It is indicated by a two-dot chain line. The storage capacitor C of the memory cell is principally composed of the first conductive plate 7, the semiconductor region 4 being the second conductive plate, and the insulator film 3.

An insulator film 8 is formed so as to cover the first conductive plate 7, and serves for electrically isolating the first conductive

plate 7 and a word line 11 to be described later.

An insulator film 9 is provided on the main surface portion of the semiconductor substrate 1 in the MISFET forming area, and serves principally to construct a gate insulator film. A gate electrode is formed on the predetermined insulator film 3, and serves to construct the MISFET Q.

The word line (WL) 11 is arranged so as to be electrically connected with the gate electrodes 10 of the memory cells adjacent in the column direction and to extend in the column direction integrally with the gate electrodes 10. It serves for turning "on" and "off" (switching operation) MISFETs to be described later (hereinafter, the direction in which the word line 11 extends shall be called the column direction).

As shown n^+-type semiconductor regions 12 are formed in the surface of the semiconductor substrate 1 on both the sides of the gate electrode 10. These regions 12 serve as a source region and a drain region of the MISFET Q. The switching transistor (MISFET) Q is composed of the gate electrode 10, the semiconductor regions 12 and the insulator film 9. One of the semiconductor regions 12 is electrically connected with the semiconductor region 6, and is electrically connected with the first conductive plate 7 as

connected with the first conductive plate 7 as stated above.

An insulator film is formed so as to cover the whole surface, and serves for electrically isolating the gate electrode 10 as well as the word line (WL) 11 and a bit line 15 to be described later.

A contact hole 14 is provided by locally removing the insulator films 9 and 13 on the other semiconductor region 12, and serves for electrically connecting the semiconductor region 12 and the bit line to be described below.

The bit line (BL) 15 is arranged in a manner to be electrically connected with the semiconductor region 12 through the contact hole 14 and to extend in the row direction. It serves to transmit a voltage serving as information.

The principle of operation of the DRAM according to the present invention having the above construction will now be described with reference to Figures 3A and 3B. In these figures, the axis of the abscissa represents the voltage value V_p [V] which is applied across the two capacitor electrodes of the MIS type storage capacitor. The axis of the ordinate represents the concentration of charges Q_{SC} [/cm^2] per unit area, the charges being held in the surface of the lower p-type semiconductor region by the voltage applied across the capacitor

electrodes. The axis of the ordinate has a logarithmic scale. Since, in Figures 3A and 3B, the p-type silicon semiconductor substrate is exemplified, the charges to be induced in the surface are negative charges for the voltages across the capacitor electrodes, $V_p > V_{FB}$ and positive charges for $V_p < V_{FB}$. In this case V_{FB} denotes a flatband voltage. The negative charges are electrons or acceptor impurities, while the positive charges are holes.

Figure 3A illustrates the case where the holes which are space charges in the depletion layer are principally utilized as the charges which are stored as information. This corresponds to the case where the p^+-type semiconductor region 4 shown in Figures 2A and 2B is included.

The principle of the prior art DRAM will be first explained with reference to Figure 3A.

Curves (a), (b) and (c) illustrate the relationships between the voltage V_p and the charge concentration Q_{SC} in the vicinity of the surface, in the prior art DRAM. In the figure, h indicates an accumulation region in which an accumulation layer is formed, k a depletion region in which a depletion layer is formed, and m an inversion region in which an inversion layer is formed.

In the figure, the curves (a), (b) and (c) indicate the numbers of electrons and acceptor impurities (the numbers of negative charges) n and the number of holes p in the case where the threshold voltage (V_{th}) of the vicinity of the semiconductor substrate surface in the storage capacitor is rendered about −0.2 V. The curve (a) indicates the number of holes p in the accumulation region h, which is expressed by $p \fallingdotseq |C_{ox}/q\ (V_p - V_{FB})|$ ·····(1). The curve (c) indicates the number of electrons and acceptor impurities n in the inversion region m, which is expressed by $n \fallingdotseq C_{ox}/q\ (V_p - V_{th})$ ·····(2). Here, C_{ox} denotes the thickness of the insulator film which is the dielectric of the capacitor. The curve (b) indicates the number of acceptor impurities appearing in the state (deep depletion state) in which no inversion layer is formed despite the inversion region, the number being approximately expressed by $Q_{SC} \propto \sqrt{V_p - V_{FB}}$. When, from the above, the surface charge concentrations Q_{SC} in the essential parts of the curves (a), (b) and (c) are evaluated, the surface negative charge concentration at the voltage $V_p = V_{th}$ becomes $Q_{IF} = 1 \times 10^{11}$ [/cm^2], and the surface negative charge concentration at the voltage $V_p = 0$ becomes $Q_{IO} = 2.2 \times 10^{11}$ [/cm^2].

In the storage capacitor of the prior-art DRAM

memory cell, charges to serve as information have been the electrons in the inversion region m. Specifically, a fixed voltage, for example, a voltage of about 5 [V] is applied across the capacitor electrodes so as to bring the operating region into the inversion region m. Thereunder, the quantity of charges Q_{IL} in the case of forming the inversion layer by externally supplying charges (the state of the curve (c)) and the quantity of charges Q_{IH} in the case of the deep depletion state without externally supplying charges (the state of the curve (b)) are established in correspondence with information. By way of example, the quantity of charges Q_{IL} corresponds to a signal "0" (namely, "L"), and the quantity of charges Q_{IH} a signal "1" (namely, "H"). The signals are read out by utilizing the difference of the quantities of charges in the two statuses, $\Delta Q_I = Q_{IL} - Q_{IH} = 5.3 \times 10^{12}$ [/cm^2].

In contrast, in the storage capacitor of the DRAM memory cell of the present invention, the charges to serve as information are space charges in, at least, a depletion region. That is, the DRAM of the present invention is characterized in that an inversion layer is not utilized.

Curves (d) and (e) illustrate the relationships between the voltage of the capacitor electrode (the voltage of the first conductive plate) V_p and the charge

concentration Q_{SC} in the vicinity of the surface of the semiconductor region 4, in the DRAM of the present invention. The curve (d) approximates a curve which is obtained by moving the curve (a) in the negative direction of the voltage V_p (leftward in the figure). The curve (e) indicates the quantity of space charges which appear in the depletion layer, not in the inversion state. The flatband voltage is set at V_{FBD} = -1.2 [V] from V_{FBI} = -0.9 [V] in the prior art. In order to increase the quantity of space charges in the depletion state by scarcely changing the flatband voltage, the p^+ -type semiconductor region 4 is formed. Specifically the impurity concentration is raised to 1.5×10^{19} [/cm^3] from the impurity concentration of the p^--type substrate 1, which is 1.5×10^{15} [/cm^3]. Thus, the quantity of charges to be fetched is increased. The ranges of voltages to establish the accumulation region h, the depletion region k and the inversion region m change similarly.

As thus far described, the space charges of the depletion region are permitted to be effectively utilized by changing the relationship between V_p and Q_{SC}. More specifically, when the first conductive plate 7 being the capacitor electrode has V_p = 0 [V] or 5 [V] applied thereto in correspondence with information, the quantity of charges as the information to be stored changes in

accordance with the curve (e). That is, the inversion layer is not formed, and the deep depletion state is established. Thus, the quantity of charges Q_{DL} at V_p = 0 [V] or the quantity of charges Q_{DH} at V_p = 5 [V] is stored. By way of example, the quantity of charges Q_{DL} corresponds to a signal "0", and the quantity of charges Q_{DH} a signal "1". When the difference between the two quantities of charges, $\Delta Q_D = Q_{DH} - Q_{DL} = 5.6 \times 10^{12}$ [/cm^2] is utilized, the information of 1 bit can be stored in the memory cell. This quantity of charges is equal or above that of the memory cell of the prior-art DRAM described before. In this manner, the sufficient quantity of charges is obtained without utilizing the inversion layer.

Fig. 3B illustrates the case where holes in the accumulation region are principally utilized as charges which are stored as information. This corresponds to a case of forming a very shallow p^+-type ion implantation region, not to the case of forming the deep p^+-type semiconductor region as in Figs. 2A and 2B. That is, it exemplifies the case where boron ions are ion-implanted shallowly so as to function as surface charges apparently. The same parts as in Fig. 3A are indicated by identical symbols, and are thus omitted from the description.

Curves (f) and (g) are approximate to curves which are respectively obtained by shifting the curves (a) and

(b) in the positive direction of the voltage V_p (rightward in the figure) by fixed values. Specifically, the flatband voltage is raised to V_{FBA} = +5.2 [V] from V_{FBI} = −0.9 [V] in the prior art. To this end, surface charges are increased by implanting boron ions to be very shallow. The ranges of the voltages V_p to establish the accumulation region h, the depletion region k and the inversion region m change similarly by the variation of the flatband voltage.

As thus far described, the holes in the accumulated state are permitted to be effectively utilized by changing the relationship between V_p and Q_{SC}. More specifically, when the first conductive plate 7 being the capacitor electrode has V_p = 0 V or 5.2 [V] applied thereto in correspondence with information, the quantity of charges as the information to be stored changes in accordance with the curves (f) and (g). That is, the inversion layer is not utilized. The quantity of charges Q_{AL} is stored at V_p = 0 [V], and the quantity of charges Q_{AH} at V_p = 5 [V]. By way of example, the quantity of charges Q_{AL} corresponds to a signal "0", and that Q_{AH} a signal "1". The difference between the two quantities of charges, $\Delta Q_A = \Delta Q_{AL} - \Delta Q_{AH}$ is greater than the quantity of charges ΔQ_I in the prior art. In this manner, the sufficient quantity of charges is obtained without utilizing the inversion layer. The quantity of charges Q_{AL} is held

by the holes in the stored state, and the quantity of charges Q_{AH} by the space charges in the depletion region. The charges of Q_{AH} are opposite in sign to those of Q_{AL}, but this forms no inconvenience, and the difference of the quantities of charges is indicated by ΔQ_A. In addition, at $V_p = 5$ [V], the quantity of charges Q_{AH} is held by the holes in the stored state located on the left side of V_{FBA} in Fig. 3B. The curves (f) and (g) can be controlled by the dose of impurity ions. In this example, the dose is equal to that in the case of Fig. 3A.

Besides the principles illustrated in Figs. 3A and 3B, a DRAM which uses the two in combination is also possible. It is possible to increase the quantity of surface charges by any method and to simultaneously increase the quantity of space charges in a depletion layer. Further, a case of employing an n-type semiconductor substrate is similar. In this case, charges to serve as information are space charges which consist of electrons in an accumulation layer or donors in a depleted state.

There will now be described a practicable method of manufacturing the first embodiment of the present invention.

First, in order to construct a DRAM, a p^--type semiconductor substrate 1 made of single crystal silicon

(Si) is prepared. As shown in Figs. 4A and 4B, the semiconductor substrate 1 is partly covered with a thick field oxide film (SiO_2 film) 2 for electrically isolating predetermined memory cells which adjoin each other or semiconductor elements (not shown) which constitute a peripheral circuit, for example, an addressing circuit, a reading circuit or a writing circuit. The field oxide film 2 may be formed by the well-known technique in which the silicon substrate is thermally oxidized locally by employing a silicon nitride film as a mask. A p^+-type region as a channel stopper may well be arranged under the field oxide film 2.

After the steps illustrated in Figs. 4A and 4B, an insulator film 3 is formed on the whole surface in order to construct a storage capacitor. Used as the insulator film 3 is a silicon nitride (Si_3N_4) film which is formed by CVD, the relative dielectric constant of which is as high as 7 - 8 and which has a thickness of, e. g., approximately 150 [Å]. In order to relieve the stress between the silicon nitride film and the semiconductor substrate 1, a first silicon dioxide (SiO_2) film having a thickness of, e. g., approximately 80 [Å] is arranged under the silicon nitride film. In order to eliminate the pinholes of the silicon nitride film, a second silicon dioxide film having a thickness of, e. g.,

approximately 30 [Å] is arranged over the silicon nitride film. The first and second SiO_2 films may be formed by thermally oxidizing the surfaces of the semiconductor substrate and the silicon nitride film, respectively. Thereafter, as illustrated in Figs. 5A and 5B, a p^+-type semiconductor region 4 to serve as the second conductive plates of storage capacitors is locally formed in the vicinity of the surface of the semiconductor substrate 1 in an area for forming the storage capacitors of memory cells, in particular, unitarily with the storage capacitors adjacent in the row direction. As explained with reference to Figs. 3A and 3B, the semiconductor region 4 is formed in the storage capacitor forming area for the purpcse of producing a larger quantity of charges of holes or in a depletion layer, to be stored in the storage capacitor and to become a larger quantity of information, or for the purpose of attaining a threshold voltage (V_{th}) higher than an operating voltage which is applied to a first conductive plate to be described later. By way of example, boron ions on the order of 5×10^{13} [atoms/cm^2] are introduced as impurities by the ion implantation at an energy level of about 30 [keV]. In order to utilize the principle stated in conjunction with Fig. 3A, the introduced impurities may be subjected to the drive-in diffusion. The depth of the semiconductor region 4

in that case is rendered 0.3 [μm] or so. On the other hand, in the case of utilizing the principle stated in conjunction with Fig. 3B, the drive-in diffusion is not carried out. In this case, it is desirable to still lower the ion implantation energy or to introduce the impurities into a very shallow position of the substrate through another insulator film. This measure is intended to cause the ion-implanted impurities to apparently function as surface charges.

Fig. 5C shows a part of memory cell arrays which are formed with the p^+-type semiconductor regions 4. The field oxide film 2 is provided for electrical isolation between the memory cells adjoining each other in the column direction, namely, in the direction in which a word line is to extend (vertical direction in the figure). The field oxide film 2 is not arranged between the memory cells adjoining each other in the row direction, namely, in the direction in which a bit line is to extend (lateral direction in the figure). In one memory cell array, the field oxide film 2 is arranged in the shape of a belt meandering from one end part to the other end part thereof. The semiconductor region 4 is arranged as a region which is common to the two capacitors adjoining each other in the row direction. A region 20 is a region which is provided so as to surround the memory cell arrays

and which serves as a guard ring. The region 20 has n-type impurities introduced thereinto later simultaneously with the formation of MISFETs Q, to be turned into an n^+-type region. A section along a cutting-plane line B - B in the figure is shown in Fig. 5B. The insulator film 3 is omitted.

After the steps illustrated in Figs. 5A and 5B, in the electrical connection part between the first conductive plate to be formed by a later step and one semiconductor region to constitute the MISFET, the insulator film 3 is locally removed to form a contact hole 5. The contact hole 5 is provided in a manner to be spaced from the semiconductor region 4. Thereafter, a polycrystalline silicon film to become the first conductive plates is formed on the whole surface by the CVD. The polycrystalline silicon film may have a thickness of approximately 1500 - 3000 [Å] by way of example. In order to render the polycrystalline silicon film low in resistivity, the processing of diffusing phosphorus is performed, or arsenic (As) ions at a dose of approximately 5×10^{14} [atoms/cm^2] are ion-implanted at an energy level of approximately 30 [keV], whereupon a heat treatment is executed. By this treatment, the impurities are diffused into the surface part of the semiconductor substrate 1 corresponding to the contact hole 5, to form the n^+-type

semiconductor region 6 constituting the MISFET which is formed by the later step. The depth of the semiconductor region 6 becomes approximately 0.2[μm]. Thereafter, the polycrystalline silicon film is locally patterned, to form the first conductive plate 7 which is electrically connected with the semiconductor region 6 as shown in Figs. 6A and 6B. Thus, the storage capacitor C of the memory cell is formed.

After the steps illustrated in Figs. 6A and 6B, using principally the silicon nitride film of the exposed insulator film 3 as a mask against a heat treatment, an insulator film (SiO_2 film) 8 which covers the first conductive plate 7 is formed by the thermal oxidation. This SiO_2 film 8 may have its thickness rendered, for example, approximately 2000 - 3000 [Å] so that the first conductive plate 7 and the word line to be formed by a later step can be electrically isolated. Thereafter, the exposed insulator film 3 is locally removed, whereupon as illustrated in Figs. 7A and 7B, an insulator film (SiO_2 film) 9 serving principally to construct a gate insulator film is formed in the removed part of the insulator film 3 by the thermal oxidation of the exposed surface of the semiconductor substrate 1. This insulator film 9 has a thickness of, for example, approximately 200 [Å].

After the steps illustrated in Figs. 7A and 7B, a polycrystalline silicon film is formed on the whole surface in order to form the gate electrodes of the MISFETs, the word lines, and the semiconductor elements of peripheral circuits. This polycrystalline silicon film is subjected to the same treatment as in the foregoing, to have its resistivity lowered. Thereafter, the polycrystalline silicon film is locally patterned, to form the gate electrode 10, the word line (WL) 11 and the gate electrode (not shown) of the MISFET of the peripheral circuit. The gate electrode 10 is electrically connected with the gate electrode 10 of the other of the memory cells adjacent in the column direction, and it constructs the word line 11 extending in the column direction. As the gate electrode 10 or the word line (WL) 11, it is also allowed to use, for example, a layer of a refractory metal such as molybdenum (Mo), tungsten (W) or titanium (Ti); a layer of any silicide which is the compound of the refractory metal and silicon; or a double-layer structure which consists of a polycrystalline silicon layer and a refractory metal layer or a refractory metal silicide layer overlying the former. Thereafter, in the MISFET forming area, using the gate electrode 10 as a mask against impurity introduction, impurities of the n^+-type are introduced in self-alignment fashion

in order to form the source region and drain region of the MISFET in the vicinities of the surface of the semiconductor substrate 1 through the insulator film 9 intervening between them and the gate electrode. The introduced impurities are subjected to the drive-in diffusion, whereby the n^+-type semiconductor regions 12 to serve as the source region and the drain region are formed as shown in Figs. 8A and 8B. The semiconductor region 6 is electrically connected with one of the semiconductor regions 12. Thus, the switching transistor (MISFET) Q of the memory cell is formed. In addition, arsenic ion impurities may be used as the n^+-type impurities and may be introduced by the ion implantation permitting them to permeate through the insulator film 9. The depth of the n^+-type region is as small as 0.2 μm.

After the steps illustrated in Figs. 8A and 8B, an insulator film 13 is formed on the whole surface for the purpose of electrically isolating the gate electrode 10 as well as the word line (WL) 11 and the bit line to be formed by a later step. As this insulator film 13, a phosphosilicate glass (PSG) film may be used which relieves the undulations of the surface and which can trap sodium (Na) ions affecting the electrical performance of the DRAM. Subsequently, in order to connect the other semiconductor region 12 and the bit line to be

formed by the later step, the insulator films 9 and 13 on this semiconductor region 12 are locally removed to form a contact hole 14. The bit line (BL) 15 is formed which is electrically connected with the semiconductor region 12 through the contact hole 14 and which extends in the row direction. This bit line (BL) 15 may be formed of, e.g. aluminium (Al). The resulting state is illustrated in Figures 2A and 2B. Thereafter, a PSG film and a silicon nitride film by the plasma CVD are formed as a final passivation film.

The operation of the first embodiment of the DRAM memory cell will now be described with reference to Figures 2A and 2B.

First, the case of writing information into the memory cell will be explained. A voltage is selectively applied to the gate electrode 10 constituting the MISFET Q of the memory cell, to turn "on" this MISFET Q. A voltage to serve as the information is applied to the bit line (BL) 15 which is electrically connected with the semiconductor region 12 through the contact hole 14. Thus, the voltage of the bit line (BL) 15 corresponding

to the information is applied to the first conductive plate 7 through the MISFET Q. The semiconductor region 4 serving as the second conductive plate is electrically connected with the semiconductor substrate 1, and is held at the fixed potential V_{SS} as predetermined. If there is a potential difference between the potential of the second conductive plate and the voltage as the information applied to the first conductive plate 7, charges to serve as information are stored in the insulator film 3 which is the intervening portion between the conductive plates, that is, they are written into the storage capacitor C of the memory cell in the normal way.

In the case of holding the information in the memory cell, the MISFET Q may be turned "off" in the state in which the information has been written into the storage capacitor C of the memory cell.

Besides, in the case of reading out the information from the memory cell, an operation reverse to the writing operation may be performed.

According to the present embodiment, in a DRAM wherein a series circuit consisting of a storage capacitor and a MISFET is employed as a memory cell, a first conductive plate which constitutes the storage capacitor is formed on a semiconductor substrate and is arranged so as to be electrically connected with one semiconductor region

of the MISFET, and a semiconductor region which has an impurity concentration higher than that of the semiconductor substrate is arranged as a second conductive plate which constitutes the storage capacitor through an insulator film, whereby charges serving as information can be stored in the storage capacitor by holes. Thus, electrons stored in an inversion layer need not be used as the charges serving as the information, so that the influence of unnecessary minority carriers attributed to α-particles or the injection thereof from a peripheral circuit portion can be prevented.

Moreover, since the storage capacitor need not take into consideration the degree of influence by the unnecessary minority carriers attributed to the α-particles or the injection from the peripheral circuit portion, the occupying area thereof can be reduced. This makes it possible to integrate the DRAM at a higher packing density.

Further, the storage capacitor can be electrically isolated from another storage capacitor adjoining it in a row direction, by the semiconductor region being the second conductive plate, so that a field oxide film of large occupying area becomes unnecessary to realize the integration of the DRAM at a higher packing density.

A second embodiment of the present invention will

be described with reference to Figure 9A to Figure 12B.

In all the figures of the present embodiment, parts having the same functions as in the first embodiment are assigned the same symbols, and they shall not be repeatedly explained.

In Fiugres 9A and 9B, the DRAM memory cell includes an insulator film 18 which is formed so as to cover at least a first conductive plate 7 and which serves to construct a storage capacitor. The insulator film 18 forms the capacitor along with the first conductive plate 7 and a third electrode to be described later (hereinafter termed the "third conductive plate"), and is provided to store charges serving as information. The insulator film 18 is also provided to electrically isolate the first conductive plates 7 of adjacent memory cells. The third conductive plate 16 is located on the insulator film 18 outside an area for forming a MISFET Q, and which serves to construct the storage capacitor. A fixed potential, for example, the same potential as that of a substrate 1 is applied to the third conductive plate 16. The third conductive plate 16 is provided as an electrode common to the whole of one memory cell array in which a plurality of memory cells are arranged in the shape of a matrix.

The third conductive plate 16 is windowed in a part for arranging the MISFET Q. The storage capacitor of the memory cell is principally constructed of a parallel circuit connection consisting of a capacitance C which is composed of the first conductive plate 7, a semiconductor region 4 being a second conductive plate and an insulator film 3, and a capacitance C_1 which is composed of the first conductive plate 7, the third conductive plate 16 and the insulator film 18. An insulator film 19 is arranged so as to cover the third conductive plate 16, and which serves to electrically isolate the third conductive plate 16 and a word line (WL) 11. Semiconductor regions 4 and 6 are spaced from each other.

When practicable memory cell arrays are constructed by the use of such memory cells shown in Figures 9A and 9B, they become as illustrated in Figure 10. In order to clarify the drawing, insulator films to be arranged between respective conductive layers, contact holes 5 and the semiconductor regions 4 are omitted from the illustration. The shapes and positional relations of the contact holes 5, the semiconductor regions 4 and other regions will be apparent from Figure 9A.

Excepting the third conductive plate 16, the second embodiment is exactly the same as in the first embodiment.

A practicable method of manufacturing the second embodiment is shown in Figures 11A, 11B, 12A and 12B.

After the steps of the first embodiment illustrated in Figures 6A and 6B, an insulator film 18 is formed on the whole surface in order to construct a storage capacitor. Likewise to the foregoing insulator film 3, this insulator film 18 may be constructed of a silicon dioxide film a silicon nitride film and another silicon dioxide film. Thereafter, a polycrystalline silicon film to become a third conductive plate is formed on the whole surface by the CVD. The polycrystalline silicon film may have a thickness of, for example, approximately 3000 [Å]. In order to render this poly-crystalline silicon film low in resistivity, phosphorus or arsenic is introduced

by the same method as in the foregoing. Subsequently, the polycrystalline silicon film is locally patterned, to form the third conductive plate 16 common to a plurality of memory cells outside a MISFET forming area as shown in Figs. 11A and 11B. Thus, the storage capacitor C_1 of the memory cell is formed.

After the steps illustrated in Figs. 11A and 11B, using principally the silicon nitride film of the exposed insulator film 18 as a mask against a heat treatment, the polycrystalline silicon layer being the third conductive plate is thermally oxidized, thereby to form an insulator film (SiO_2 film) 19 which covers the third conductive plate 16. Thereafter, the exposed insulator film 18 and the underlying insulator film 3 are locally removed. As in the first embodiment, a gate insulator film 9 is formed in the removed area as shown in Figs. 12A and 12B. Further, a gate electrode 10, a word line (WL) 11 and semiconductor regions 12 are formed.

After the steps illustrated in Figs. 12A and 12B, an insulator film 13, a contact hole 14 and a bit line (BL) 15 are formed as in the first embodiment. Then, the resultant structure becomes as shown in Figs. 9A and 9B. Thereafter, a PSG film and a silicon nitride film by the plasma CVD are formed as a final passivation film.

The operation of the second embodiment will be explained with reference to Figures 9A and 9B.

First, the case of writing information into the memory cell will be explained. A voltage is selectively applied to the gate electrode 10 constituting the MISFET Q of the memory cell, to turn "on" this MISFET Q. A voltage corresponding to the information is applied to the bit line (BL) 15 which is electrically connected with the semiconductor region 12 through the contact hole 14. Thus, the voltage of the bit line (BL) 15 to serve as the information is applied to the first conductive plate 7 through the MISFET Q. The semiconductor region 4 serving as the second conductive plate is electrically connected with the semiconductor substrate 1, and is held at the fixed potential V_{SS} as predetermined. Also the third conductive plate 16 is held at the fixed potential V_{SS} by way of example. If there is a potential difference between the potentials of the second conductive plate and the third conductive plate 16 equal to each other and the voltage as the information applied to the first

conductive plate 7, charges to serve as information are stored in the insulator film 3 and the insulator film 18 which are the intervening portions between the conductive plates, that is, they are written into the storage capacitor C and C_1 of the memory cell in the normal way.

In the case of holding the information in the memory cell, the MISFET Q may be turned "off" in the state in which the information has been written into the storage capacitor C and C_1 of the memory cell.

Besides, in the case of reading out the information of the memory cell, an operation reverse to the writing operation may be performed.

According to the present embodiment, effects similar to those of the first embodiment are achieved.

Furthermore, by arranging a third conductive plate on a first conductive plate through an insulator film, the quantity of charges to be stored by the first conductive plate and the second conductive plate and the quantity of charges by the first conductive plate and the third conductive plate can be stored in a storage capacitor. Thus, when the second embodiment is compared with the first embodiment, the quantity of charge storage of the storage capacitor per unit area can be increased to approximately double, and the integration of the DRAM

at a higher packing density can be realized.

It should be noted that, when the potential of a substrate or a p^+-type semiconductor region 4 is a substrate bias potential V_{BB} = −3.0 V and the potential of a polycrystalline silicon layer 16 is at earth potential V_{SS} = 0 V, the quantity of charge storage becomes about 1.5 times that in the absence of the polycrystalline silicon layer 16.

In addition, by arranging the third conductive plate 16 of fixed potential on the first conductive plate, a word line WL to which a control voltage of fluctuating magnitude is applied can be prevented from affecting the first conductive plate 7, so that the quantity of charges to be stored in the storage capacitor can be stabilized. Thus, the writing and reading operations of the DRAM can be stabilized, and the reliability of the DRAM can be enhanced.

A third embodiment is an example wherein, in the second embodiment, the thick field oxide film 2 which isolates the memory cells is not formed at all. The plane and sectional shapes of the third embodiment become identical to those of Figs. 9A and 9B and Fig. 10 from which the field oxide film 2 has been omitted. For this reason, the plane and sectional shapes of the DRAM of the third embodiment shall not be explained, and a practicable method of manufacturing the embodiment will be described,

along with the brief description of the structure thereof, with reference to Figures 13, 14 and 15. In these figures, parts having the same functions as in the first and second embodiments are assigned the same symbols, so that they are not repeatedly described.

First, excepting a memory cell array portion, a semiconductor substrate 1 is partly covered with a field oxide film in order to electrically isolate the semiconductor elements (not shown) of a peripheral circuit. As in the first and second embodiments, an insulator film 3 is formed on the whole surface. Thereafter, a mask 17 for impurity introduction made of, e.g. a silicon nitride film is formed selectively on the insulator film 3 in an area in which the MISFET of a switching transistor is to be formed by a later step. An area outside the memory cell array, namely, an area to form the peripheral circuit therein is covered with the mask 17. Subsequently, using the mask 17, p-type impurities are introduced into the part of the semiconductor substrate 1 other than the mask 17, to form a p^+-type semiconductor region 4 which becomes the second conductive plate of a storage capacitor and which serves to electrically isolate memory cells

adjacent in row and column directions, as illustrated in Fig. 13. That is, the p^+-type semiconductor region 4 is formed on the whole surface of the memory cell array except for the area in which the MISFETs are to be provided.

After the steps illustrated in Fig. 13, the mask 17 is removed, whereupon in the electrical connection part between a first conductive plate to be formed by a later step and one semiconductor region to constitute the MISFET, the insulator film 3 is locally removed to form a contact hole 5. The contact hole 5 and the semiconductor region 4 are spaced.

Thereafter, a polycrystalline silicon film to become the first conductive plate is formed on the whole surface, and it is implanted with As ions to lower its resistivity and simultaneously to locally form an n^+-type semiconductor region 6. Subsequently, the polycrystalline silicon film is locally patterned to form the first conductive plate 7 as shown in Fig. 14.

After the steps illustrated in Fig. 14, as in the second embodiment, an insulator film 18 and a third conductive plate 16 are formed thereby to construct a storage capacitor C_1. After forming insulator films 19 and 9, a gate electrode 10 and a word line (WL) 11 are formed. By forming semiconductor regions 12, the

MISFET Q is constructed. After forming an insulator film 13 and a contact hole 14, a bit line (BL) 15 is formed as shown in Fig. 15. In Fig. 15, insulator films to be provided between respective conductive layers are omitted in order to simplify the drawing.

As in the first embodiment, the MISFETs Q may well be formed to finish up the DRAM, without forming the storage capacitors C_1.

The DRAM of the third embodiment is finished up by these series of manufacturing steps. Thereafter, a final passivation film is formed as in the first or second embodiment.

According to the present embodiment, effects similar to those of the second embodiment are achieved.

Furthermore, the memory cell of the DRAM can be electrically isolated from other memory cells adjoining it in row and column directions, by a semiconductor region being a second conductive plate which constitutes a storage capacitor. Accordingly, a field oxide film in a memory cell array becomes unnecessary, and the integration of the DRAM at a higher packing density can be realized.

A fourth embodiment will be described with reference to Figs. 16A to 23B. The fourth embodiment is an example wherein a trench (groove) is added to the first embodiment

in order to increase the quantity of charges which can be stored in a capacitor. Throughout the drawings of the fourth embodiment, parts having the same functions as in the first embodiment are assigned the same symbols, and they are not repeatedly explained.

In Figs. 16A and 16B, the DRAM memory cell includes a field oxide film 2. Memory cells are shaped by the field oxide films 2 so that the pattern of one pair of the memory cells may be repeated in a row direction as shown in Fig. 19. Within a memory cell array, the field oxide film 2 is located principally between the memory cells adjacent in a column direction. This is the same as in the first or second embodiment.

A trench 21 (groove) is provided in a semiconductor substrate 1 in an area for forming a storage capacitor therein, and which serves to construct the storage capacitor. This trench 21 increases the quantity of charges as information per unit area in the storage capacitor.

A p^+-type semiconductor region 4 serving as a second conductive plate is arranged in the main surface of the semiconductor substrate 1 in the storage capacitor forming area and the surface of the substrate 1 within the trench 21, and is provided unitarily with the storage capacitors adjacent in the row direction. The situation

of such p^+-type semiconductor regions 4 is shown in Fig. 19.

Now, a method of manufacturing the fourth embodiment will be described.

First, a field oxide film (SiO_2 film) 2 and p^+-type semiconductor regions 4 are formed by the same method as that of the first embodiment illustrated in Figs. 4A, 4B, 5A and 5B.

After the step illustrated in Figs. 5A and 5B, an insulator film 22A, an insulator film 22B and an insulator film 22C are formed on the whole surface of a semiconductor substrate 1 in order to form a trench and a second conductive plate. The insulator film 22C is a mask against etching for forming the trench, and a silicon dioxide (SiO_2) film may be employed by way of example. The insulator film 22B is a mask against impurity introduction for forming the second conductive plate, and a silicon nitride (Si_3N_4) film may be employed by way of example. The insulator film 22A serves to relieve the stress between the semiconductor substrate 1 and the silicon nitride film 22B, and a silicon dioxide film may be employed by way of example. The insulator film 22A may be formed by the thermal oxidation of the surface of the substrate 1. The insulator films 22B and 22C may be formed by the CVD. The insulator film 22C in a storage capacitor forming area

is locally patterned, to form a first mask for forming the trench. Anisotropic dry etching is performed using the first mask, whereby the insulator films 22B and 22C are locally removed to form a second mask out of the insulator film 22B, and further, a predetermined part of the semiconductor substrate 1 is locally removed to form the trench 21 as shown in Figs. 17A and 17B. The widthwise dimension W of the trench 21 may be approximately 1 - 1.5 [μm], and the depth thereof from the surface of the semiconductor substrate 1 may be approximately 2 - 4 [μm].

After the steps illustrated in Figs. 17A and 17B, the insulator film 22C having served as the first mask is removed, and the insulator film 22B to serve as the second mask is exposed. Using this second mask, impurities are introduced into the vicinity of the surface of the semiconductor substrate 1 exposed inside the trench 21, whereby a p^+-type semiconductor region 4 to become the second conductive plate is formed as shown in Figs. 18A and 18B. By way of example, the semiconductor region 4 is formed in such a way that boron (B) ions at a concentration of approximately 1×10^{18} [atoms/cm^3] or above are introduced by thermal diffusion at approximately 900 - 1000 [°C]. In this case, the depth of the semiconductor region 4 taken from the surface

of the semiconductor substrate 1 inwardly thereof is made approximately 0.3 [μm].

The state of memory cell arrays after the formation of the semiconductor regions 4 is shown in Fig. 19. The insulator films 22A and 22B are omitted in Fig. 19. A section along a cutting-plane line B - B in Fig. 19 is shown in Fig. 18B.

After removing the insulator films 22B and 22A, the same insulator film 3 as in the first embodiment for forming the storage capacitor is formed as shown in Figs. 20A and 20B.

After the step illustrated in Figs. 20A and 20B, a contact hole 5, an n^+-type semiconductor region 6 and a first conductive plate 7 are formed as shown in Figs. 21A and 21B by the same method as that illustrated in Figs. 6A and 6B. The trench 21 may well be buried with polycrystalline silicon for the first conductive plate 7 so as to flatten the surface thereof.

After the steps illustrated in Figs. 21A and 21B, using principally the silicon nitride film of the exposed insulator film 3 as a mask against a heat treatment, an insulator film (SiO_2 film) 8 which covers the first conductive plate 7 is formed by the thermal oxidation. The insulator film 8 may have its thickness made, e. g., approximately 2000 - 3000 [Å] so that the first conductive

plate 7 and a word line to be formed by a later step can be electrically isolated. Thus, in the case where the portion of the trench 21 is not buried, the interior of the groove needs to be buried by the use of a burying material, for example, a polycrystalline silicon film or an insulator film. The polycrystalline silicon needs to be turned into an insulator by oxidation. Thereafter, the exposed insulator film 3 is locally removed, whereby the same insulator film 9 as in the first embodiment is formed as shown in Figs. 22A and 22B.

After the steps illustrated in Figs. 22A and 22B, a MISFET Q and a word line WL are formed as shown in Figs. 23A and 23B. These are the same as those of the first embodiment shown in Figs. 8A and 8B.

Thereafter, an insulator film 13, a bit line BL, etc. are formed as in the first embodiment. Then, the resultant structure becomes as shown in Figs. 16A and 16B.

Thereafter, a PSG film and a silicon nitride film by the CVD are formed as a final passivation film.

Operations in the cases of writing information into the memory cell of the fourth embodiment, holding the information and reading out the information are the same as in the first embodiment.

According to the fourth embodiment, the same effects as in the first embodiment are achieved.

In addition, the variation of the quantity of charge storage ascribable to minority carriers and the coupling of the depletion layer of one trench with that of another trench in the deep parts of the trenches 21 can be prevented. Accordingly, the trenches 21 can be formed deep. The distance between adjacent trenches, namely, the distance D_1 indicated in Fig. 17A can also be shortened.

Furthermore, since all regions for forming capacitors are p^+-type semiconductor regions, the distance D_2 between a trench and a field oxide film as indicated in Fig. 17A can be shortened.

A fifth embodiment will be described with reference to Figs. 24A, 24B and 25. Since the manufacturing method thereof is substantially similar to that of the fourth embodiment, it shall not be explained. The fifth embodiment is an example wherein the first conductive plate of the fourth embodiment is further overlaid with a third conductive plate to which a fixed potential is applied, so as to increase and stabilize a capacitance.

In the drawings of the fifth embodiment, parts having the same functions as in the fourth embodiment are assigned the same symbols, and so are not repeatedly explained.

In Figs. 24A and 24B, the DRAM memory cell includes an insulator film 18, similar in construction to the foregoing insulator film 3, which is located so as to cover at least a first conductive plate 7 and which serves to construct a storage capacitor C_1. This insulator film 18 stores charges owing to the first conductive plate 7 and a third electrode to be described later (hereinafter, termed "third conductive plate"). It electrically isolates the first conductive plates 7 of adjacent memory cells. The third conductive plate 16 for constructing the storage capacitor, is located on the insulator film 18 outside an area for forming a MISFET Q therein and which is connected and provided unitarily with the third conductive plate of the other memory cell in an identical memory cell array. A fixed potential, for example, the same potential as that of a substrate is applied to this third conductive plate 16. The storage capacitor of the memory cell is principally constructed of a parallel connection consisting of a capacitance C which is composed of the first conductive plate 7, a semiconductor region 4 being a second conductive plate and the insulator film 3, and a capacitance C_1 which is composed of the first conductive plate 7, the third conductive plate 16 and the insulator film 18. An insulator film 19 is arranged

so as to cover the third conductive plate 16, and serves to electrically isolate the third conductive plate 16 and a word line (WL) 11.

When practicable memory cell arrays are constructed by the use of the memory cells as shown in Figures 24A and 24B, they become as illustrated in Figure 25. In order to simplify the drawing, the insulator films to be located between respective conductive layers are not illustrated.

A figure obtained by omitting the third conductive plates 16 in Figure 25 is identical to the plan view of the fourth embodiment.

The operation of the fifth embodiment is the same as that of the second embodiment.

According to the fifth embodiment, effects similar to those of the second and fourth embodiments are achieved.

A sixth embodiment will be described with reference to Figures 26, 27 and 28. The sixth embodiment is an example wherein, in the fifth embodiment, the field oxide film 2 which electrically isolates the memory cells adjacent in the column direction is omitted and no field oxide film is provided within the memory

cell array.

In the drawings of the sixth embodiment, parts having the same functions as in the third and fourth embodiments are assigned the same symbols, and so they are not repeatedly explained.

First, excepting a memory cell array portion, a semiconductor substrate 1 is partly covered with a field oxide film by the local thermal oxidation of the substrate 1 in order to electrically isolate the semiconductor elements (not shown) of a peripheral circuit. A trench 21 and the insulator film 3 are formed. Thereafter, a p^+-type semiconductor region 4 is formed in the whole area of the memory cell array except for an area covered with a mask 17, by the same method as shown in Figure 13.

After the steps illustrated in Figure 26, a contact hole 5, an n^+-type semiconductor region 6 and a first conductive plate 7 are formed by the same method as shown in Figure 14. A section of Figure 27 is identical to Figure 21B in which the field oxide film 2 is replaced with the p^+-type semiconductor region 4.

After the steps illustrated in Fig. 27, as in the third embodiment, an insulator film 18 and a third conductive plate 16 are formed, thereby to construct a storage capacitor C_1. After forming insulator films 19 and 9, a gate electrode 10 and a word line (WL) 11 are formed, and semiconductor regions 12 are formed, thereby to form a MISFET Q. After forming an insulator film 13 and a contact hole 14, a bit line (BL) 15 is formed as shown in Fig. 28. In Fig. 28, in order to simplify the drawing, insulator films to be provided between respective conductive layers are not shown. In addition, a section of Fig. 28 is equal to Fig. 24B in which the field oxide film 2 is replaced with the p^+-type semiconductor region.

Thereafter, the processing of a protective film etc. is performed as in the first embodiment.

In the sixth embodiment, the p^+-type semiconductor region 4 and the n^+-type semiconductor region 6 need to be provided in spaced relation as in the other embodiments.

The operation of the sixth embodiment is the same as that of the second embodiment.

According to the sixth embodiment, effects similar to those of the third and fifth embodiments are achieved.

In the sixth embodiment, it is needless to say that the formation of the third conductive plate 16

may well be omitted. This is identical to the relation between the third embodiment and the first embodiment. The plan and section of the memory cells of the DRAM in this case and the sections thereof in the course of the manufacturing steps will be apparent from the description of the third and fourth embodiments.

The present embodiment brings forth the following effects:

A storage capacitor is constructed of an insulator film which is located on the surface of a semiconductor substrate, a first conductive plate one end part of which is located on the insulator film and the other end part of which is arranged so as to be electrically connected with one semiconductor region of a MISFET, and a semiconductor region to serve as a second conductive plate, which is arranged in a predetermined surface part of the semiconductor substrate. This eliminates the coupling between the depletion layers of the adjacent storage capacitors, and the leakage of charges between them.

Since the leakage of the charges is eliminated, the retention time of charges in the storage capacitor is enhanced, and the frequency of refreshing operations is lowered. Accordingly, the operating speed of the DRAM is enhanced.

As charges to be stored in a storage capacitor,

charges in an accumulation layer or a narrow depletion layer are used. Accordingly, it becomes unnecessary to use electrons which are stored in a wide depletion layer or an inversion layer, so that the DRAM is not affected by minority carriers.

Since the degree of influence of minority carriers on a storage capacitor need not be considered, the occupying area of the storage capacitor can be reduced. Thus, the integration of the DRAM at a higher packing density is realized.

Since charges can be stored between a first conductive plate and a second conductive plate and between the first conductive plate and a third conductive plate, the quantity of charge storage of a storage capacitor per unit area increases.

A memory cell is electrically isolated from another memory cell adjoining it in a row direction or/and a column direction, by a semiconductor region being a second conductive plate which constitutes a storage capacitor. An isolation region made of an insulator film becomes unnecessary, and the integration of the DRAM at a higher packing density is permitted.

The occupying area of a memory cell can be markedly reduced, and the integration of the DRAM at a still higher packing density is permitted.

By providing a third conductive plate of fixed potential on a first conductive plate, the influence of a word line on the first conductive plate is eliminated, and the quantity of charges to be stored in a storage capacitor is stabilized. The writing and reading operations of the DRAM are also stabilized.

Since a semiconductor region of a first conductivity type constituting the capacitance of a memory cell and a semiconductor region of a second conductivity type connected with the MISFET of the memory cell are arranged spaced from each other, the reverse breakdown voltage of a junction is not deteriorated.

In a modified embodiment from those described above, a p-type well region is formed in an n-type semiconductor substrate and the memory cells of a DRAM are formed within the well region. In addition, it is possible to employ an n-type semiconductor substrate and to use an n-type semiconductor region as a second conductive plate so as to store charges for information. Furthermore, it is possible to form an n-type well region in a p-type semiconductor substrate and to form the memory cells of a DRAM within the well region.

In the fourth to sixth embodiments, an ion implantation process may well be employed as a method of forming a semiconductor region which is a second conductive plate. In this case, the ion implantation is performed in the state shown in Figure 18B. The implanted impurity element, for example, boron is introduced into the bottom of a trench 21. The boron is diffused by subsequent annealing, to form a semiconductor region in the bottom of the trench 21 and to rise along the side wall of the trench toward the surface of a substrate. Therefore, the semiconductor region is formed also in a part of the side wall of the trench. The semiconductor region extending along the side wall does not reach the vicinity of the substrate surface (a region where a semiconductor region 6 of the opposite conductivity type is formed). With this measure, the capacitance of a memory cell decreases to some extent, but a mask registration margin for spacedly arranging the semiconductor regions 4 and 6 of the conductivity types opposite to each other can be dispensed with.

CLAIMS.

1. A semiconductor memory device having memory cell arrays in which memory cells are arranged in the shape of a matrix, said each memory cell comprising a switching element and a first capacitor which is formed on a main surface of a semiconductor substrate of a first conductivity type and which is connected with said switching element, wherein:-

(a) said capacitor comprises a first insulator film which is formed on the main surface of said semiconductor substrate, a first electrode a part of which is electrically connected with said switching element and which is formed on said first insulator film, said first electrode being independent for said each memory cell, and a semiconductor region to serve as a second electrode, which is formed in said semiconductor substrate under said first insulator film and which has the first conductivity type and an impurity concentration higher than that of said semiconductor substrate; and

(b) the semiconductor regions of one memory cell and at least one of the memory cells which adjoin said one memory cell within the identical memory cell array are formed commonly.

2. A semiconductor memory device according to claim 1, wherein said capacitor is formed within a groove, said groove being formed by removing said semiconductor substrate from said main surface thereof

inwardly, and said semiconductor region is formed in said main surface of said semiconductor substrate and a surface of said groove.

3. A semiconductor memory device according to claim 1, wherein said at least one memory cell is connected to a bit line identical to that of said one memory cell and also to a word line adjacent to that of said one memory cell.

4. A semiconductor memory device according to claim 1, including a second capacitor which is formed on said first capacitor, wherein said second capacitor comprises the first electrode, a second insulator film which is formed on at least said first electrode, and a third electrode which is formed on at least said second insulator film.

5. A semiconductor memory device according to claim 4, wherein said third electrode is an electrode common to all the memory cells of the identical memory cell array, and it is formed unitarily within one memory cell array.

6. A semiconductor memory device according to claim 5, wherein said second insulator film is formed under the whole third electrode.

7. A semiconductor memory device according to claim 5, wherein said third electrode is connected to earth potential of said semiconductor memory device.

8. A semiconductor memory device according to claim 4, wherein said capacitors are formed within a groove, said groove being formed by removing said semiconductor substrate from said main surface thereof inwardly, and said semiconductor region is formed in said main surface of said semiconductor substrate and a surface of said trench.

9. A semiconductor memory device according to claim 4, wherein said at least one memory cell is connected to a bit line identical to that of said one memory cell and also to a word line adjacent to that of said one memory cell.

10. A semiconductor memory device according to claim 4, wherein said substrate is p^- type and said semiconductor region constituting the second electrode of the first capacitor is of the p^+ type.

11. A semiconductor memory device according to claim 4, wherein said substrate is n^- type and said semiconductor region constituting the second electrode of the first capacitor is of the n^+ type.

12. A semiconductor memory device according to claim 4, wherein an insulator film is applied over the flat surface of the third electrode above where it projects into the central zone of said groove.

13. A semiconductor memory device according to claim 12, wherein word lines are formed over the insulator film.

14. A semicondcutor memory device according to claim 13, wherein a further insulator film is provided over all the elements which form the stack of semiconductor layers.

15. A semiconductor memory device according to claim 14, wherein a bit line is formed over said last mentioned insulator film, said bit line making contact with the drain or source region of the memory cell, opposite to that source or drain region which is in contact with the first electrode through a contact hole.

16. A semiconductor memory device constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.