WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a cell array including a plurality of DRAM cells to store data; and

refresh control logic configured to refresh the plurality of DRAM cells according to access scenario information provided from an external source,

wherein the refresh control logic is configured to determine a refresh time of the plurality of DRAM cells with reference to the access scenario information and a retention characteristic of the plurality of DRAM cells, and is configured to refresh the plurality of DRAM cells according to the determined refresh time, and

wherein the access scenario information includes:

a data retention time indicating a duration that the data should be retained in the plurality of DRAM cells; and

a total refresh time comprising the total duration of at least one non-operation period within the data retention time where external access to the plurality of DRAM cells is not permitted.

2. The semiconductor memory device of claim 1, wherein the refresh control logic divides a portion of the total refresh time corresponding to a refresh window by a number of rows of the cell array to be refreshed to calculate the refresh time.

3. The semiconductor memory device of claim 1 or claim 2, wherein, if the determined refresh time is shorter than predetermined value, the refresh control logic outputs refresh-unavailable information to an external device.

4. The semiconductor memory device of any one of claims 1 to 3, further comprising a refresh mode register in communication with the refresh control logic

including a refresh time register configured to store the total refresh time; and

a fail bit mode register configured to store a value indicative of an acceptable number of fail bits.

5. The semiconductor memory device of claim 4, wherein the refresh control logic further includes:

a refresh clock controller configured to adjust a frequency of a refresh clock in response to at least one of the total refresh time and the acceptable number of fail bits indicated by the refresh mode register.

6. The semiconductor memory device of any one of claims 1 to 5, wherein the refresh control logic is configured to initiate refresh operations of the plurality of DRAM cells in response to an externally received refresh enable signal.

7. The semiconductor memory device of any one of claims 1 to 6, further comprising:

a temperature sensor configured to sense an operating temperature of the semiconductor memory device and to provide the sensed operating temperature to the refresh control logic,

wherein the refresh control logic is configured to adjust the refresh time according to the sensed operating temperature.

8. The semiconductor memory device of any one of claims 1 to 3, further comprising:

a command decoder configured to decode a command received from an external source and to generate an internal control signal in response to the decoded command,

wherein the command decoder is not configured to decode a refresh command to initiate a refresh operation.

9. The semiconductor memory device of claim 8, further comprising a refresh mode register configured to store the access scenario information.

10. A memory system comprising:

a host configured to record and read data in a buffer during a data retention time depending on an access scenario; and

a DRAM in communication with the host to receive, store and send the data,

wherein the DRAM is provided as the buffer of the host and is configured to receive time information of the access scenario,

wherein the time information of the access scenario includes:

the data retention time indicating a duration that the data should be retained in the plurality of DRAM cells; and

a total refresh time comprising the total duration of at least one non-operation period within the data retention time where external access to the plurality of DRAM cells is not permitted;

wherein the DRAM is configured to perform self-refresh operations on a memory area where the data received from the host is stored during the non-operation period of the access scenario, and

wherein the host is configured to enable the self-refresh operation of the DRAM by providing a refresh enable signal to the DRAM.

11. The memory system of claim 10, wherein the host is an image processing device that uses the DRAM as a frame buffer to store frames of image data.

12. The memory system of claim 10 or claim 11, wherein the DRAM includes:

refresh control logic configured to calculate a refresh time corresponding to a time duration between initiating refresh of sequentially refreshed rows of the memory area by using at least one of the time information of the access scenario, an operating temperature of the DRAM, and a number of allowable fail bits of the DRAM.

13. The memory system of any one of claims 10 to 12, wherein the DRAM includes:

a first memory area that is configured to be accessed at a timing depending on the access scenario; and

a second memory area that is configured to be accessed at a timing dependent on receiving external commands outside of the access scenario.

14. The memory system of claim 13, wherein the host is configured to provide access area information to the DRAM and the DRAM is configured to select a self-refresh mode for the first memory area but not the second memory area based on the access area information.

15. The memory system of claim 14, wherein the DRAM is configured to perform refresh operations of the second memory area as auto refresh operations in response to receiving corresponding auto refresh commands provided by the host.

16. A refresh method of a semiconductor memory device in which data are written and read based on a scenario, the method comprising:

receiving a data retention time according to an access scenario and a length of a non-operation period included in the data retention time from an external source;

calculating a refresh time of a memory area where the data are written using the length of the non-operation period and a characteristic parameter of memory cells; and

refreshing the memory area at a timing depending on the calculated refresh time during the non-operation period,

wherein the data retention time according to the access scenario indicates a duration that the data should be retained in a plurality of DRAM cells, and

wherein a total refresh time comprises the total duration of at least the non-operation period within the data retention time where external access to the plurality of DRAM cells is not permitted.

17. The method of claim 16, wherein, in the calculating of the refresh time, the refresh time is determined with reference to a number of acceptable error bits within the data.

18. The method of claim 16 or claim 17, wherein, in the calculating of the refresh time, the refresh time is determined based upon an operation temperature of the semiconductor memory device.

19. The method of any one of claims 16 to 18, wherein, in the refreshing, the semiconductor memory device refreshes the memory area by initiating refresh operations when a refresh enable signal is activated during the non-operation period, wherein the timing of the initiation of the refresh operations does not correspond to receipt of any externally received refresh commands.