CLAIMS

1. A defect locating system comprising:

a marking tool configured to physically mark a surface of a wafer at one or more locations near a defect buried in a vertically stacked semiconductor structure fabricated on the wafer; and

an optical inspection tool comprising:

an illumination source configured to generate an amount of illumination light;

an illumination subsystem configured to focus the amount of illumination light at a vertically stacked semiconductor structure disposed on a wafer;

a collection subsystem configured to collect light from the vertically stacked structure in response to the focused illumination light;

a detector configured to detect the light collected and generate one or more output signals indicative of the amount of collected light; and

a computing system configured to:

receive the one or more output signals;

determine a location of the buried defect based on the one or more output signals;

determine the locations of the one or more physical marks based on the one or more output signals; and

determine a distance between the location of the buried defect and the locations of the one or more physical marks in at least two dimensions parallel to the surface of the wafer.

2. The defect locating system of claim 1, further comprising:

a material removal tool configured to remove material from the surface of the wafer; and

a computing system configured to:

receive an indication of the locations of the one or more physical marks and the distance between the location of the buried defect and the locations of the one or more physical marks; and

communicate a command signal to the material removal tool that causes the material removal tool to remove material from the wafer at the location of the buried defect; and

a defect verification tool configured to image the buried defect after removal of the material.

3. The defect locating system of claim 2, wherein the material removal tool is a focused ion beam machining tool.

4. The defect locating system of claim 1, wherein the marking tool and the optical inspection tool are integrated into a single wafer processing tool.

5. The defect locating system of claim 1, wherein the marking tool includes any of a laser, a mechanical scribe, and an electron beam.

6. The defect locating system of claim 1, wherein the surface of the wafer is physically marked at two or more locations near the buried defect.

7. The defect locating system of claim 1, wherein each of the one or more physical marks are located within five micrometers of the location of the buried defect.

8. The defect locating system of claim 1, wherein the distance between the location of the buried defect and the locations of the one or more physical marks is determined with a precision of less than one hundred nanometers.

9. The defect locating system of claim 1, wherein the buried defect is located at least fifty nanometers below the surface of the wafer.

10. The defect locating system of claim 1, wherein the vertically stacked semiconductor structure is a three dimensional NAND memory device.

11. The defect locating system of claim 1, wherein the illumination source of the optical inspection system is a broadband laser sustained plasma light source.

12. A method comprising:

physically marking a surface of a wafer at one or more locations near a defect buried in a vertically stacked semiconductor structure fabricated on the wafer with a marking tool;

focusing an amount of illumination light generated by an illumination source of an optical inspection tool onto the vertically stacked semiconductor structure disposed on the wafer;

collecting light from the vertically stacked structure in response to the focused illumination light with a collection subsystem of the optical inspection tool;

detecting the light collected and generating one or more output signals indicative of the amount of collected light with a detector of the optical inspection tool;

determining a location of the buried defect based on the one or more output signals;

determining the locations of the one or more physical marks based on the one or more output signals; and

determining a distance between the location of the buried defect and the locations of the one or more physical marks in at least two dimensions parallel to the surface of the wafer, wherein the determining of the location of the buried defect, the determining of the locations of the one or more physical marks, and the determining of the distance are performed by a computing system.

13. The method of claim 12, further comprising:

removing material from the surface of the wafer at the location of the buried defect based at least in part on the distance between the location of the buried defect and the locations of the one or more physical marks.

14. The method of claim 13, further comprising:

imaging the buried defect with an defect verification tool after removal of the material.

15. The method of claim 12, wherein the marking of the surface of the wafer involves any of a laser, a mechanical scribe, and an electron beam.

16. The method of claim 12, wherein the surface of the wafer is physically marked at two or more locations near the buried defect.

17. The method of claim 12, wherein each of the one or more physical marks are located within five micrometers of the location of the buried defect.

18. The method of claim 12, wherein the distance between the location of the buried defect and the locations of the one or more physical marks is determined with a precision of less than one hundred nanometers.

19. The method of claim 12, wherein the vertically stacked semiconductor structure is at least three micrometers thick and the buried defect is located at least fifty nanometers below the surface of the wafer.

20. A defect locating system comprising:

a marking tool configured to physically mark a surface of a wafer at one or more locations near a defect buried in a vertically stacked semiconductor structure fabricated on the wafer; and

an optical inspection tool comprising:

an illumination source configured to generate an amount of illumination light;

an illumination subsystem configured to focus the amount of illumination light at a vertically stacked semiconductor structure disposed on a wafer;

a collection subsystem configured to collect light from the vertically stacked structure in response to the focused illumination light;

a detector configured to detect the light collected and generate one or more output signals indicative of the amount of collected light; and

a computing system comprising:

one or more processors; and

a non-transitory, computer-readable medium storing instructions, that when executed by the one or more processors, cause the defect locating system to:

receive the one or more output signals;

determine a location of the buried defect based on the one or more output signals;

determine the locations of the one or more physical marks based on the one or more output signals; and

determine a distance between the location of the buried defect and the locations of the one or more physical marks in at least two dimensions parallel to the surface of the wafer.

21. The defect locating system of claim 20, further comprising:

a material removal tool configured to remove material from the surface of the wafer, the non-transitory, computer-readable medium further storing instructions, that when executed by the one or more processors, cause the defect locating system to:

receive an indication of the locations of the one or more physical marks and the distance between the location of the buried defect and the locations of the one or more physical marks; and

communicate a command signal to the material removal tool that causes the material removal tool to remove material from the wafer at the location of the buried defect; and

a defect verification tool configured to image the buried defect after removal of the material.