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DRAWINGS ATTACHED

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(54) SIGNAL SEPARATION APPARATUS FOR STEREOPHONIC MULTIPLEX RECEIVERS

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to stereophonic multiplex radio receiver systems and, in particular, to a stereo multiplex detector or decoder circuit particularly adapted for fabrication by integrated circuit techniques.

In the system presently employed in the United States for stereophonic FM broadcasting, a main carrier wave is frequency modulated by the sum of two stereophonically related left (L) and right (R) audio frequency signals, the carrier wave being adapted for compatible reception by either monophonic or stereophonic FM radio receivers. The main carrier wave is modulated further with stereophonic information in the form of a suppressed subcarrier wave amplitude modulated with the difference of the two stereophonically related audio signasl (L—R), a continuous pilot signal for use in demodulating the suppressed subcarrier wave at the receiver and, in some instances, an additional commercial background music (SCA) frequency modulated subcarrier wave.

In a conventional stereophonic FM receiver, a composite signal is produced at the output of a frequency modulation detector, the composite signal comprising the sum (L+R) audio signal component usable either by monophonic or stereophonic FM receivers and extending within a frequency range of, for example, 0 to 15,000 Hertz (Hz), a 19 kilohertz (kHz) pilot signal and sidebands of a suppressed 38 kHz subcarrier representative of the difference (L−R) signal component extending within a frequency range of 23 to 53 kHz. The composite signal also may include a 67 kHz background music (SCA) frequency modulated subcarrier and its sidebands extending, for example, from 59 to 75 kHz. This "store-casting component generally is removed in home receivers by tuned filter circuits.

Relatively low level signals of the type described above which are encountered in stereophonic FM decoding circuits advantageously may be processed utilizing monolithic integrated circuit chips (i.e., solid state structures wherein a plurality of active semiconductor devices, such as transistors and diodes, and passive circuit components, such as capacitors and resistors, are simultaneously constructed and interconnected on a common substrate of semiconductor material). Such integrated circuit techniques offer size, weight, reliability and, in many instances, economic advantages when compared with the conventional assembly of circuit arrangements using discrete devices.

In the design of integrated circuits, as compared to circuits utilizing discrete devices, different economic ground rules are followed. For example, while discrete device circuit design places a premium on a minimum number of the relatively costly discrete active devices, such devices are not relatively costly in the integrated circuit domain. In the latter case, it is particularly desirable to perform functions on the chip with minimal resort to external or outboard components. Some of the advantages of integrated circuits are compromised, for example, where coils and/or transformers are interconnected with chips. In addition to the cost, size, weight and reliability factors suffering, one or more of the relatively few terminals available on a typical chip (e.g., sixteen terminals) will be required for interconnection with each inductive device. Furthermore, because of the relatively small physical dimensions of a chip (e.g., of the order of 0.1 inches by 0.1 inches square or less), and the consequent close spacing of leads for external devices, it is desirable to minimize the number of external leads which are required to carry alternating signal currents and thereby re-

duce problems associated with unwanted coupling between various sections of the chip.

The use of inductive components for such functions as the removal of SCA signals above 53 kHz prior to detection of the difference signal from the composite signal is undesirable, for the most part. The use of inductors will add to the difficulty of manufacturing receivers since they usually must be adjusted, thereby requiring complex electronic test equipment for the manufacture of the receivers. If the plurality of inductive components are used, they must be physically located one with respect to the others so as to minimize undesired interaction between their field patterns. Also, inductors for the ultrasonic frequency range of an impedance level suited to use with integrated circuits are bulky and costly.

In the stereophonic receiver, a composite signal is produced at the output of the frequency modulation detector, the composite signal comprising the sum (L+R) signal component useable either by monophonic or stereophonic frequency modulation receivers, a 19 kHz (kilohertz) pilot signal and sidebands of a suppressed 38 kHz subcarrier representative of the difference (L−R) signal component. Then, a 38 kHz signal is generated in the receiver in timed relation with the 19 kHz pilot signal to permit detection of the difference signal component. The detection of the composite signal in a synchronous detector providing an output signal balanced against its composite signal input and against its 38 kHz signal input removes the need for tuned filter circuits before the detector to remove SCA signals from the composite signal to prevent intermodulation products arising from the SCA signals from appearing in the detector output.

The present invention concerns electronic signal separation apparatus suitable for multiplex FM broadcast receivers. This apparatus separates first and second audio-frequency (a−f) signals multiplexed together in a composite signal having a subchannel in which information concerning the difference of said first and second a−f signals is contained in symmetrical sideband spectra about a subcarrier frequency, which subcarrier frequency may be suppressed. The composite signal also has signal spectra unrelated to this subcarrier frequency comprising at least in part the sum of the first and second a−f signals. A doubly balanced synchronous detector timed in response to timing signals containing the subcarrier frequency is used to recover the difference of the first and second a−f signals from the composite signal. The two outputs of this synchronous detector are in push-pull relationship to each other. This facilitates the subsequent summation of each of them with composite signal or portions thereof provided in one phasing only, which summations will recover the first and second a−f signals with substantially lessened admixtuer of one into the other. The summations of the signals as described above is done in two signal-adding circuits. By the use of a doubly balanced synchronous detector to recover the difference of the first and second a−f signals which detector has each of its outputs balanced against its composite signal and timing signal input signals, only signals with upper and lower sidebands symmetrically disposed about the subcarrier frequency will develop audio-frequency components of output. This for practical purposes removes the need for filtering the composite signal applied to the detector to prevent unwanted intermodulation products.

This method of recovering the first and second a−f signals is advantageous over prior art methods in which the subchannel is separated from the sum of the first and second a−f signals by a band-pass filter before the subchannel difference of first and second a−f signals information is recovered by detection. The band-pass filter unless very carefully designed and constructed will introduce frequency-dependent phase and amplitude variations into the recovered difference signals which will adversely affect the separation of the first and second signals obtained from the subsequent summing of the push-pull difference signals with the sub of the first and second signals. The first and second a−f signals are presumed in the remainder of this description to be stereophonically related left (L) and right (R) signals. Referring to the drawing, means are shown for detecting an audio diferenec signal (L−R) component of a composite stereophonic signal and for combining such component with an audio sum (L+R) signal component so as to produce stereophonically related left and right channel audio signals. The illustrated diference signal detector and combining (matrix amplifier) means are particularly adapted for fabrication using integrated circuit techniques.

An FM radio tuner-detector 100 which processes FM broadcast signals to provide composite stereophonic signals is coupled via a terminal T_1 of an integrated circuit chip 11 to a composite signal amplifier 12. The composite stereophonic signals comprise an audio frequency sum (L+R) signal in the case of reception of monophonic broadcast material or, in the case of reception of stereophonic broadcast material, the composite stereophonic signal comprises an audio sum signal (L+R) component, a pilot (19 KHz component) and a suppressed subcarrier amplitude modulated by a difference (L−R) signal component. In either case,

FM background (SCA) music components also may be coupled to terminal T_1.

Composite signal amplifier 12 is arranged to amplify, in a linear manner, signals in the range of approximately 10 Hz to 150 KHz so as to produce first and second substantially identical but 180° out of phase (i.e., push-pull) amplified composite signals for direct application to circuit elements within integrated circuit chip 11.

A specific configuration for amplifier 12, as well as for other circuit elements shown in block diagram form on chip 1, is described in our concurrently filed Patent Application No. 60162/70 (Serial No. 1,332,515).

The push-pull composite signal components, along with suitable substantially equal biasing voltages, are direct coupled from amplifier 12 to a difference signal detector indicated generally by the reference numeral 13. Difference signal detector 13 comprises a doubly balanced synchronous detector having first and second current source transistors 14 and 15. The base electrodes of transistors 14 and 15 are directly connected to separate ones of the push-pull composite signal outputs of the composite signal amplifier 12. The emitter electrodes of transistors 14 and 15 are individually returned to ground by resistors 16 and 17, respectively. The collector electrode of transistor 14 is directly connected to joined emitter electrodes of a first pair of switching transistors 18, 19 while the collector electrode of transistor 15 is directly connected to joined emitter electrodes of a second pair of switching transistors 20, 21. The base electrodes of both transistors 18 and 20 are connected to one of a pair of 38 KHz square wave outputs of a synchronized 38 KHz push-pull signal source 42 while the base electrodes of transistors 19 and 21 are connected to the other of the 38 KHz square wave outputs. Square wave signal source 42 is synchronized with respect to the 19 KHz pilot component of the composite posite signals provided by amplifier 12 by any of the many known techniques employed in FM multiplex stereophonic decoder systems. One particularly advantageous synchronizing system is set forth in our above-identified Patent Application.

A source of operating voltage (B+) is coupled to the collector electrodes of each of transistors 18 and 21 by means of an output resistor 2 and to the collector electrodes of each of transistors 19 and 20 by means of an output resistor 23 substantially equal to resistor 22.

Push-pull output signals including the demodulated difference signal components [(L−R) and−(L−R)] are developed across resistors 22 and 23 and are coupled, repectively, to emitter follower output transistors 24 and 25. Transistors 24 and 25 serve as voltage sources to produce the desired push-pull difference signal components across respective matrix resistors 26 and 27. The sum (L+R) signal information is also developed across resistors 26 and 27 by means of respective transistors 28 and 29, the collector electrodes of which are coupled to resistors 26 and 27 at their ends remote from transistors 24 and 25. The base electrodes of transistors 28 and 29 both are coupled to one of the push-pull outputs of composite signal amplifier 12. The emitter electrodes of transistors 28 and 29 are returned to ground by means of indiivdual resistors 30 and 31, respectively. Transistors 24 and 28 comprise a first matrix amplifier arrangement, the output of which (e.g., R) is coupled via a terminal T_{11} of chip 11 and a de-emphasis network 32 to audio reproducing means such as an amplifier and loudspeaker (not shown). Transistors 25 and 29 comprise a second matrix amplifier arrangement, the output of which (e.g., L) is coupled via a terminal T_{10} of chip 11 and a de-emphasis network 33 to audio reproducing means such as a second amplifier and loudspeaker (not shown).

It is to be noted that by this arrangement the de-emphasis time constants for both the (L+R) and the (L−R) components of the left output signal are determined by the same source resistance of the resistor 27 and by the shared de-emphasis network 32. These time constants, therefore, are identical, avoiding one source of frequency-dependent loss of separation. Similarly the de-emphasis time constants for both the (L+R) and−(L−R) components of the right output signal are the same, avoiding a frequency-dependent loss of separation.

In order to maintain the impedance at the emitters of follower transistors 24 and 25 substantially constant as conduction (and therefore the impedances) of transistors 28 and 29 vary with applied composite signals, a composite signal of opposite phase with respect to that of the signal applied to transistors 28 and 29 is applied from amplifier 12 to the base electrodes of compensating transistors 34 and 35. The collector electrodes of transistors 34 and 35 are directly connected, respectively, to the emitter electrodes of followers 24 and 25. The emitter electrodes of transistors 34 and 35 are returned to ground by separate resistors 36 and 37.

As the output signals produced by composite signal amplifier 12 vary, conduction of transistors 28 and 34 vary equally and oppositely (push-pull input signals). Therefore, the sum of the collector currents of transistors 28 and 34 (which load transistors 24) remains substantialy constant. Similarly, variations in the output of composite signal amplifier 12 do not produce variations

in the load on transistor 25 since the sum of the collector currents of transistors 29 and 35 remains substantialy constant as the output of composite signal amplifier 12 varies. Accurate matrixing of the sum and differenec signal components is therefore not compromised by variations in loading on voltage source transistors 24 and 25 as the composite signal varies.

In the operation of the difference signal detector 13 described above, the complementary 38 KHz square wave outputs of signal source 42 are provided in predetermined time relationship with respect to the received 19 KHz pilot signal component (and therefore with respect to the suppressed 38 KHz subcarrier) to provide synchronous detection of the difference signal components (L−R) of the amplitude modulated suppressed subcarrier component coupled from amplifier 12 to transistors 14 and 15. That is, the average axis crossings of the 38 KHz square waves coincide in time with average axis crossings of the pilot signal component. The balanced synchronous detector 13 comprising transistors 14, 18, 19 and transistors 15, 20, 21 responds to the combination of the complementary 38 KHz square waves and the push-pull composite signals to produce complementary signals including the difference signal components [(L−R) and−(L−R)] across resistors 22 and 23. The output voltages produced across resistors 22 and 23, including the complementary difference signal components, are coupled via transistors 24 and 25 to resistors 26 and 27. Transistors 24 and 25, along with resistors 22 and 23, therefore serve as differenec signal voltage sources with respect to resistors 26 and 27.

The composite signals provided by amplifier 12, including the audio-frequency sum component (L+R), govern current flows through the collector resistors 26 and 27 of transistors 28 and 29 to develop voltage drops thereacross. These voltage drops added to the voltages having difference signal [(L−R) and−(L−R)] audio-frequency components appearing at the emitters of transistors 24 and 25 produce signals having the desired left (L) and right (R) audio-frequency components at terminals T_{10} and T_{11}. The low-pass characteristics of the de-emphasis networks 32, 33 remove components (e.g. pilot and 38 kHz sidebands generated in the synchronous detection process) from the de-emphasized left and right audio-frequency signals appearing across the output filter capacitors of networks 32 and 33.

Correct matrixing of the sum and difference signal components is dependent in part upon matching of the currents supplied by the source transistors 14, 15, 28 and 29. In the integrated circuit environment, such matching is relatively easily accomplished by constructing substantially identical transistors 14, 15, 28 and 29 and substantially identical associated emitter resistors 16, 17, 30 and 31 in close proximity on the chip 11. Matching the currents provided by the source transistors 14, 15, 28 and 29 permits predistortion of the composite signals supplied by the composite signal amplifier 12 to compensate for distortions of the composite signal in each of the source transistors 14, 15, 28 and 29.

Correct matrixing is also dependent upon the ratios of resistors 22 and 23 to resistors 26 and 27, respectively. In the illustrated doubly-balanced synchronous detector arrangement, the switching transistors 18, 19, 20, 21 are supplied with 38 kHz symmetrical square waves of correct phasing so that full wave detection of the 38 kHz difference signal subcarrier signal is obtained. The resultant peak to peak amplitude of the audio frequency components of the detected difference signal is related to the peak amplitude of the rectified difference signal carrier wave at the output of the detector 13 by a factor of $2/\pi$. For the left only or a right only audio signal, the peak amplitude of the modulated difference signal carrier wave component of the composite signal is set by the standards for stereophonic broadcasting as equal to the peak amplitude of the sum signal component. To obtain proper matrixing the sum and difference signals, in the case where the currents of the source transistors 14, 15, 28 and 29 are matched, therefore, resistors 22 and 23—across which the difference signals are developed—are selected $\pi/2$ times as large as the resistors 26 and 27 across which the sum signal components are developed.

Normally the tolerances upon integrated resistors such as 26 and 27 are considerably looser than those of discrete resistors and capacitors, such as those contained in de-emphasis networks 32 and 33. The discrete resistors which are effectively in series with resistors 26 and 27 for de-emphasis purposes are selected to have resistances larger than that of resistors 26 and 27 by a certain factor. This factor is greater than the ratio of the expected deviations from nominal resistance value of the integrated resistors to the expected deviations from nominal resistance value of the discrete resistors. This procedure will permit the overall de-emphasis characteristics at the left and the right outputs to be maintained to a tolerance no larger than that determined by said discrete components.

The synchronous difference signal detector 13 further comprises means for automatically disabling operation of the difference signal detection circuits, for example, either when the prolonged absence of pilot

signal greater than a predetermined amplitude indicates that non-stereophonic (monophonic) program material is being received or when the signal-to-noise ratio of the received signal is judged too poor for satisfactory stereophonic reproduction. Such means for disabling operation of the difference signal detection circuits is described and claimed in our concurrently filed Patent Application No. 60161/70 (Serial No. 1,332,514). One system for producing a "stereo-mono" switching signal is described in the above-identified Application 60162/70 (Serial No. 1,332,515). For purposes of the present discussion it is sufficient to recognize that such a switching signal is produced for either of the above-noted conditions.

In the apparatus shown in the drawing, stereophonic-monophonic switching signals are supplied by a stereo switching signal source 38 to an amplifier comprising a first transistor 39 having a collector electrode connected to a source of operating voltage (B+), a base electrode coupled to stereo switching signal source 38 and an emitter electrode coupled via a resistor 40 to the base electrode of a switching transistor 41. The emitter electrode of transistor 41 is connected to ground and an output switching signal is derived at the collector electrode thereof across a resistor 42 coupled to the source of operating voltage. The output of switching transistor 41 is coupled to a muliple V_{BE} bias supply of the type described in our Patent No. 1,229,274.

As used herein, the term V_{BE} is defined as the forward voltage drop across the base-emitter junction of anormally conducting transistor (e.g., approximately 0.65 to 0.7 volts for silicon transistors such as are fabricated in integrated circuits). Reference voltage suplies (usualy internal to the integrated circuit) which provide one or more integral multiples of V_{BE} above ground potential at a low impedance are designated as "multiple V_{BE} supplies".

In the present case, the multiple V_{BE} supply comprises a common collector transistor 44 and a common emitter transistor 45 coupled together in a negative feedback arrangement. The collector electrode of transistor 44 is coupled to the source of operating voltage while a plurality of resistors 46, 47, 48 are coupled in series relation between the emitter electrode of transistor 44 and ground. The junction of resistors 47 and 48 is connected to the base electrode of transistor 45. The emitter electrode of transistor 45 is connected to ground; its collector electrode is directly connected to the base electrode of transistor 44 and coupled by resistor 43 to the source of operating voltage. When transistors 44 and 45 are conducting, a voltage equal to V_{BE} exists across resistor 48. Resistor 48 is selected smaller than the base-emitter impedance of transistor 45 and the additonal resistors 46, 47 are selected smaller than the input impedances of the respective circuits to which they are coupled. In that case, voltages are developed across each of the series connected resistors 46, and 47 equal to the product of V_{BE} and the ratio between the particular resistor (46 or 47) and resitisor 48. Specifically, voltages of 7 V_{BE} and 4 V_{BE} are developed at the emitter electrode of transistor 44 and at the junction of resistors 46 and 47, respectively.

The junction of resistors 46 and 47 is coupled to the base electrodes of a pair of stereo switching or stereo killer transistors 49 and 50. The emitter electrodes of transistors 49 and 50 are coupled, respectively, to the joined emitter electrodes of switching transistors 18, 19 and the joined emitter electrodes of switching transistors 20, 21. The collector electrodes of transistors 49 and 50 are directly joined together and this collector junction is connected to the emitter electrodes of respective current splitter transistors 51 and 52 via separate emitter resistors 53 and 54. The base electrodes of current splitter transistors 51 and 52 are directly connected to the emitter electrode of transistor 49 (7 V_{BE} when the multiple V_{BE} supply is operating). The collector electrodes of splitter transistors 51 and 52 are connected to resistors 22 and 23, respectively.

A feedback circuit is coupled between the input and output of the switched multiple V_{BE} supply to increase the rate at which the system switches from stereophonic to monophonic mode. This circuit comprises a transistor 55 having a collector electrode coupled via a resistor 56 to the base electrode of transistor 41, a base electrode coupled via a resistor 57 to the emitter electrode of transistor 44 and an emitter electrode connected to ground.

In operation, upon the loss of stereophonic information suitable for reproduction or when the detected signal is too noisy for satisfactory reproduction as is explained in Application No. 60162/70 (Serial No. 1,332,515), the voltage at the base electrode of transistor 39 falls below a predetermined level (e.g., one volt) and transistors 39 and 41 begin to switch to an off or non-conductive conditon. The voltage at the base electrode of transistor 44 increases positively causing transistor 44 and then transistor 45 to conduct so that the multiple V_{BE} supply switches on. This switching action is aided by the presence of transisstor 55 which commences conduction along with transistors 44 and 45. Transistor 55 serves to switch transistor 41 off rapidly once the switching operation begins. A positive volt-

age (4 V_{BE}) provided at the junction of resistors 46 and 47 causes killer transistors 49 and 50 to conduct. Similarly, a positive voltage (7 V_{BE}) provided at the emitter electrode of transistor 44 causes splitter transistors 51 and 52 to conduct.

When killer transistors 49 and 50 conduct, a sufficiently positive voltage (3 V_{BE}) is coupled to the joined emitter electrodes of switching transistors 18 and 19 and to the joined emitter electrodes of switching transistors 20, 21 to reverse bias such switching transistors and thereby disable the difference signal detector 13. The push-pull composite signals supplied via current source transistors 14 and 15 are then diverted through killer transistors 49 and 50 and cancel each other at the joined collector electrodes of transistors 49, 50. The joined collector electrodes of transistors 49 and 50 also serve to combine the direct current components of the outputs of current source transistors 14 and 15. The combined direct current components are then split into equal components by means of resistors 53, 54 and transistors 51, 52 and the equal components are coupled to load resistors 22 and 23. The direct bias voltage coupled to matrix transistors 24 and 25 is therefore maintained substantially equal for either stereophonic or monophonic reproduction modes. If such direct bias voltage was allowed to change when the operating mode of the system changed, a thump would be heard in the associated loudspeakers. The above-described arrangement precludes production of such an undesirable sound.

The difference signal detector is maintained in an inoperative or bypassed condition until an input to transistor 39 representative of, for example, the presence of adequate pilot signal is provided to switch transistors 39 and 41 on and to thereby switch the multiple V_{BE} supply, and the killer and splitter stages off.

As noted above, an input signal greater than approximately one volt (low current V_{BE} of transistor 39 plus normal current V_{BE} of transistor 41) is sufficient to maintain conduction of transistors 39 and 41 (and therefore maintain operation in the stereophonic mode). However, when transistors 39 and 41 are switched off and transistor 55 is on (i.e., monophonic operating mode), a positive voltage greater than one volt is required at the base of transistor 39 to reinitiate stereophonic operation since resistors 40 and 56 are then coupled via transistor 55 as a voltage divider across the input (base emitter) terminals of transistor 41. An input voltage of approximately 3 V_{BE} (approximately two volts) is thus required at the base of transistor 39 to switch to stereophonic mode. The difference between the levels required at the base of transistor 39 to initiate and to remain in stereophonic mode provides a desirable hysteresis characteristic whereby once stereophonic reproduction is initiated it will be maintained even though momentary fluctuations occur either in the received pilot signal level or in signal-to-noise ratio of the detected signal.

When stereophonic information suitable for reproduction is received and processed by the associated receiver, a sufficiently positive input voltage is supplied to the base of transistor 39 to render it conductive. Transistor 41 also conducts, so that the input to transistor 44 is not sufficiently positive to produce conduction in transistor 44. The multiple V_{BE} supply comprising transistors 44 and 45 is therefore switched "off" and each of transistors 49, 50, 51 and 52 is switched "off". Under these conditions, the difference signal detector circuits 13 operate to produce (L−R) and −(L−R) signals in the manner previously described. It should also be noted that transistor 55 is off under these conditions.

The above-described matrix amplifier-automatic switching arrangement also provides the advantage that, should the output terminals T_{10} and T_{11} accidentally be shorted to ground, the resistors 26 and 27 serve to limit current in the associated transistors. Such short circuit protection is particularly desirable in connection with a complex integrated circuit chip which has a significant cost as in the presently described case.

WHAT WE CLAIM IS:—

1. Electronic signal separation apparatus suitable for stereophonic multiplex FM receivers to separate first and second audio-frequency signals multiplexed together in a composite signal, said composite signal having a sub-channel containing information concerning the difference of said first and second audio-frequency signals in symmetrical sideband spectra about a subcarrier frequency, which subcarrier frequency may be suppressed, and having signal spectra unrelated to said subcarrier frequency comprising at least in part a component representing the sum of said first and second audio-frequency signals, said signal separation apparatus comprising a doubly balanced synchronous detector having first and second inputs for receiving, respectively, said composite signal and a timing signal recurrent at said subcarrier frequency, and first and second outputs for respectively providing first and second detected signals in response to said composite and timing signals, said first and second detected signals being in push-pull relationship to each other and each balanced against said composite signal and said timing signal; a first signal-adding circuit responsive to said first detector out-

age (4 V_{BE}) provided at the junction of resistors 46 and 47 causes killer transistors 49 and 50 to conduct. Similarly, a positive voltage (7 V_{BE}) provided at the emitter electrode of transistor 44 causes splitter transistors 51 and 52 to conduct.

When killer transistors 49 and 50 conduct, a sufficiently positive voltage (3 V_{BE}) is coupled to the joined emitter electrodes of switching transistors 18 and 19 and to the joined emitter electrodes of switching transistors 20, 21 to reverse bias such switching transistors and thereby disable the difference signal detector 13. The push-pull composite signals supplied via current source transistors 14 and 15 are then diverted through killer transistors 49 and 50 and cancel each other at the joined collector electrodes of transistors 49, 50. The joined collector electrodes of transistors 49 and 50 also serve to combine the direct current components of the outputs of current source transistors 14 and 15. The combined direct current components are then split into equal components by means of resistors 53, 54 and transistors 51, 52 and the equal components are coupled to load resistors 22 and 23. The direct bias voltage coupled to matrix transistors 24 and 25 is therefore maintained substantially equal for either stereophonic or monophonic reproduction modes. If such direct bias voltage was allowed to change when the operating mode of the system changed, a thump would be heard in the associated loudspeakers. The above-described arrangement precludes production of such an undesirable sound.

The difference signal detector is maintained in an inoperative or bypassed condition until an input to transistor 39 representative of, for example, the presence of adequate pilot signal is provided to switch transistors 39 and 41 on and to thereby switch the multiple V_{BE} supply, and the killer and splitter stages off.

As noted above, an input signal greater than approximately one volt (low current V_{BE} of transistor 39 plus normal current V_{BE} of transistor 41) is sufficient to maintain conduction of transistors 39 and 41 (and therefore maintain operation in the stereophonic mode). However, when transistors 39 and 41 are switched off and transistor 55 is on (i.e., monophonic operating mode), a positive voltage greater than one volt is required at the base of transistor 39 to reinitiate stereophonic operation since resistors 40 and 56 are then coupled via transistor 55 as a voltage divider across the input (base emitter) terminals of transistor 41. An input voltage of approximately 3 V_{BE} (approximately two volts) is thus required at the base of transistor 39 to switch to stereophonic mode. The difference between the levels required at the base of transistor 39 to initiate and to remain in stereophonic mode provides a desirable hysteresis characteristic whereby once stereophonic reproduction is initiated it will be maintained even though momentary fluctuations occur either in the received pilot signal level or in signal-to-noise ratio of the detected signal.

When stereophonic information suitable for reproduction is received and processed by the associated receiver, a sufficiently positive input voltage is supplied to the base of transistor 39 to render it conductive. Transistor 41 also conducts, so that the input to transistor 44 is not sufficiently positive to produce conduction in transistor 44. The multiple V_{BE} supply comprising transistors 44 and 45 is therefore switched "off" and each of transistors 49, 50, 51 and 52 is switched "off". Under these conditions, the difference signal detector circuits 13 operate to produce (L−R) and −(L−R) signals in the manner previously described. It should also be noted that transistor 55 is off under these conditions.

The above-described matrix amplifier-automatic switching arrangement also provides the advantage that, should the output terminals T_{10} and T_{11} accidentally be shorted to ground, the resistors 26 and 27 serve to limit current in the associated transistors. Such short circuit protection is particularly desirable in connection with a complex integrated circuit chip which has a significant cost as in the presently described case.

WHAT WE CLAIM IS:—

1. Electronic signal separation apparatus suitable for stereophonic multiplex FM receivers to separate first and second audio-frequency signals multiplexed together in a composite signal, said composite signal having a sub-channel containing information concerning the difference of said first and second audio-frequency signals in symmetrical sideband spectra about a subcarrier frequency, which subcarrier frequency may be suppressed, and having signal spectra unrelated to said subcarrier frequency comprising at least in part a component representing the sum of said first and second audio-frequency signals, said signal separation apparatus comprising a doubly balanced synchronous detector having first and second inputs for receiving, respectively, said composite signal and a timing signal recurrent at said subcarrier frequency, and first and second outputs for respectively providing first and second detected signals in response to said composite and timing signals, said first and second detected signals being in push-pull relationship to each other and each balanced against said composite signal and said timing signal; a first signal-adding circuit responsive to said first detector out-

put and said sum component of said composite signal for providing a recovered version of said first audio-frequency signal; and a second signal-adding circuit responsive to said second detector output and to said sum component of said composite signal for providing a recovered version of said second audio-frequency signal.

2. Electronic signal separation apparatus as claimed in Claim 1, in which said synchronous detector includes first and second current sources providing push-pull versions of said composite signal current, first and second transistors having their emitter electrodes coupled to said first current source, and third and fourth transistors having their emitter electrodes coupled to said second current source, said source of timing signals being a signal voltage source coupling the intercoupled base electrodes of said first and third transistors to the intercoupled base electrodes of said second and fourth transistors, and said first and second detector outputs being respectively at the interconnected collector electrodes of said first and fourth transistors and at the interconnected collector electrodes of said second and third transistors.

3. Electronic signal separation apparatus as claimed in Claim 2, comprising first and second resistors each coupling a different one of said detector outputs to a source of energizing potential and having push-pull detected voltages developed respectively thereacross, third and fourth resistors, third and fourth current sources having composite signal components phased similarly to a composite signal component provided from said first current source and phased oppositely to a composite signal component provided from said second current source, a first buffer amplifier having an input from said first detector output and having an output coupled to said third current source through said third resistor to develop said recovered first audio-frequency signal at a first output terminal located at the end of said third resistor remote from its end coupled to said first buffer amplifier, and a second buffer amplifier having an input from said second detector output and having an output coupled to said fourth current source through said fourth resistor to develop said recovered second audio-frequency signal at a second output terminal located at the end of said fourth resistor remote from its end coupled to said second buffer amplifier.

4. Electronic signal separation apparatus as claimed in Claim 3, in which said third and fourth resistors have resistance values substantially $\frac{2}{\pi}$ — that of said first and second resistors, which are equal valued, said first and second buffer amplifiers each have a gain with a magnitude of substantially unity, and the magnitudes of the composite signal component provided by said first, second, third and fourth current sources are substantially identical.

5. Electronic signal separation apparatus as claimed in Claim 3 or 4, comprising a fifth current source having composite signal components equal in instantaneous amplitude with but opposite in instantaneous polarity to those of said third current source coupled to the output of said buffer amplifier to lessen the variation of the loading upon said first buffer amplifier and a sixth current source having composite signal components equal in instantaneous amplitude with but opposite in instaneous polarity to said fourth current source coupled to the output of said second buffer amplifier to lessen the variation of the loading upon said second buffer amplifier.

6. Elecetronic signal separation apparsatus as claimed in any of Claims 3—5, in which each of said buffer amplifiers is a common-collector transistor amplifier stage.

7. Electronic signal separation apparatus as claimed in any of Claims 3—6, in which all of said transistors, resistors and buffer amplifiers are constructed within the confines of a single monolithic integrated circuit.

8. Electronic signal separation apparatus as claimed in any of Claims 3—7, in which each of said first and said second output terminals is coupled to a frequency-selective component forming part of a filter effective to attenuate signal components above the audio-frequency range.

9. Electronic signal separation apparatus as claimed in any of Claims 3—7, in which each of said first and said second output terminals is coupled to a frequency-selective component forming part of a filter effective to de-emphasize higher audio-frequency signal components and to attenuate signal components above the audio-frequency range.

10. Electronic signal apparatus as claimed in Claims 7 and 9, in which said first output terminal is coupled by a fifth discrete resistor to a first discrete capacitor across which a recovered first audio-frequency signal with de-emphasized higher audio-frequency components is developed, said second output terminal is coupled by a sixth discrete resistor to a second discrete capacitor across which a recovered second audio-frequency with de-emphasized higher audio-frequency components is developed, said third and fourth resistors have the same nominal resistance R, said first and second capacitors have the same nominal capacitance C, and said fifth and sixth discrete resistors have the same nominal resistance

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which is appreciably R times the ratio of the expected percentage of deviation of said resistance of said third and fourth resistors from its nominal value R to the expected percentage of deviation of the resistance of said fifth and said sixth resistors from their nominal value, or greater so that the attenuation characteristics of said filters are maintained to a toleranec no larger than that determined by said discrete components.

11. Electronic signal separation apparatus as claimed in any of Claims 1—10 comprising conditional means to render said difference signal ineffective while said sum signal passes through to both the two recovered AF outputs.

12. Electronic signal separation apparatus substantially as hereinbefore described in conjunction with the accompanying drawings.

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