WHAT IS CLAIMED IS:

1. A memory system, including:

a memory device coupled with a host; and

a memory controller comprising a second interface communicated with a first interface of the host;

wherein the memory controller is coupled with the memory device and configured to:

receive, through the second interface from the first interface of the host, an identifier indicating a peak power capability supported by the host, and

determine a peak power management policy matches the peak power capability according to the identifier,

wherein the peak power capability is greater than an operating power of the memory device.

2. The memory system of claim 1, wherein the identifier includes at least one of:

a first identifier representing a first current magnitude that a power management unit of the host is capable of providing to the memory device at a first voltage; and

a second identifier representing a second current magnitude that the power management unit of the host is capable of providing to the memory controller at a second voltage.

3. The memory system of claim 1, wherein the memory controller is further configured to:

replacing a default peak power management policy preset in the memory controller with the determined peak power management policy.

4. The memory system of claim 3, wherein the memory controller is further configured to:

in response to determining that the host fails to send the identifier, maintain the default peak power management policy; and

in response to failing to determine the peak power management policy matches the peak power capability according to the identifier, maintain the default peak power management policy.

5. The memory system of claim 1, wherein the determined peak power management policy includes one or more parameters of controlling the memory system.

6. The memory system of claim 5, wherein:

the one or more parameters include at least one of a clock frequency, parallelism of the memory device, and an operation latency of an I/O request.

7. The memory system of claim 1, wherein:

the memory system includes a flash universal storage (UFS) memory system; and

each of the first interface and the second interface includes a UFS interface.

8. The memory system of claim 7, wherein the identifier is carried in an extended field of a UFS data packet.

9. The memory system of claim 2, wherein the power management unit includes a power management integrated circuit (PMIC).

10. The memory system of claim 1, wherein the memory controller is further configured to:

send, through the second interface to the first interface of the host, a response message indicating that the identifier has been received by the memory controller.

11. The memory system of claim 1, wherein

the memory controller is further configured to:

receive, through the second interface from the first interface of the host, an input/output (I/O) request; and

control the memory device to process the I/O request according to the determined peak power management policy.

12. An electronic device, including:

a host comprising:

a power management unit, and

a first interface configured to send an identifier indicating a peak power capability supported by the power management unit; and

a memory system comprising:

a memory device; and

a memory controller comprising a second interface communicated with the first interface and configured to receive the identifier,

wherein the memory controller is configured to determine a peak power management policy matches the peak power capability according to the identifier,

wherein the peak power capability is greater than an operating power of the memory device.

13. The electronic device of claim 12, wherein the identifier includes at least one of:

a first identifier representing a first current magnitude that a power management unit of the host is capable of providing to the memory device at a first voltage; and

a second identifier representing a second current magnitude that the power management unit of the host is capable of providing to the memory controller at a second voltage.

14. The electronic device of claim 12, wherein the memory controller is further configured to:

replacing a default peak power management policy preset in the memory controller with the determined peak power management policy;

in response to determining that the host fails to send the identifier, maintain the default peak power management policy; and

in response to failing to determine the peak power management policy matches the peak power capability according to the identifier, maintain the default peak power management policy.

15. The electronic device of claim 12, wherein:

the determined peak power management policy includes one or more parameters of controlling the memory system; and

the one or more control parameters include at least one of a clock frequency, parallelism of the memory device, and an operation latency of an I/O request.

16. The electronic device of claim 12, wherein:

the memory system includes a flash universal storage (UFS) memory system;

each of the first interface and the second interface includes a UFS interface;

the identifier is carried in an extended field of a UFS data packet; and

the power management unit includes a power management integrated circuit (PMIC).

17. The electronic device of claim 12, wherein the memory controller is further configured to:

send, through the second interface to the first interface of the host, a response message indicating that the identifier has been received by the memory controller;

receive, through the second interface from the first interface of the host, an input/output (I/O) request; and

control the memory device to process the I/O request according to the determined peak power management policy.

18. A power controlling method, comprising:

sending, through a first interface of a host, an identifier indicating a peak power capability supported by the host;

receiving, by a second interface of a memory controller of a memory system communicated with the first interface, the identifier;

determining, by the memory controller of the memory system, a peak power management policy matches the peak power capability according to the identifier; and

applying, by the memory controller, the peak power management policy to control the memory system,

wherein the peak power capability is greater than an operating power of a memory device in the memory system.

19. The method of claim 18, wherein the identifier includes at least one of:

a first identifier representing a first current magnitude that a power management unit of the host is capable of providing to the memory device at a first voltage; and

a second identifier representing a second current magnitude that the power management unit of the host is capable of providing to the memory controller at a second voltage.

20. The method of claim 18, further comprising:

replacing, by the memory controller, a default peak power management policy with the determined peak power management policy.