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10 METHOD FOR PREVENTING JUNCTION LEAKAGE
IN FIELD EMISSION DISPLAYS

15 This invention relates generally to field emission displays (FEDs) and more particularly to a method for preventing junction leakage in FEDs.

20 Flat panel displays have recently been developed for visually displaying information generated by computers and other electronic devices. Typically, these displays are lighter and utilize less power than conventional cathode ray tube displays. One type of flat panel display is known as a cold cathode field emission display (FED).

25 A cold cathode FED uses electron emissions to illuminate a cathodoluminescent screen and generate a visual image. An individual field emission cell typically includes one or more emitter sites formed on a baseplate. 30 The baseplate typically contains the active semiconductor devices that control electron emission from the emitter sites. The emitter sites may be formed directly on a baseplate formed of a material such as silicon or on an interlevel conductive layer (e.g., polysilicon) or 35 interlevel insulating layer (e.g., silicon dioxide, silicon nitride) formed on the baseplate. A gate electrode structure, or grid, is typically associated with the emitter sites. The emitter sites and grid are connected to an electrical source for establishing a voltage

differential to cause a Fowler-Nordheim electron emission from the emitter sites. These electrons strike a display screen having a phosphor coating. This releases the photons that illuminate the screen. A single pixel of the display screen is typically illuminated by one or several emitter sites.

In a gated FED, the grid is separated from the base by an insulating layer. This insulating layer provides support for the grid and prevents the breakdown of the voltage differential between the grid and the baseplate. Individual field emission cells are sometimes referred to as vacuum microelectronic triodes. The triode elements include the cathode (field emitter site), the anode (cathodoluminescent element) and the gate (grid). U.S. Patent No. 5,210,472 to Stephen L. Casper and Tyler A. Lowrey entitled "Flat Panel Display In Which Low-Voltage Row and Column Address Signals Control A Much Higher Pixel Activation Voltage", describes a flat panel display that utilizes FEDs.

In flat panel displays that utilize FEDs, the quality and sharpness of an illuminated pixel site of the display screen is dependent on the precise control of the electron emission from the emitter sites that illuminate a particular pixel site. In forming a visual image, such as a number or letter, different groups of emitter sites must be cycled on or off to illuminate the appropriate pixel sites on the display screen. To form a desired image, electron emission may be initiated in the emitter sites for certain pixel sites while the adjacent pixel sites are held in an off condition. For a sharp image, it is important that those pixel sites that are required to be isolated remain in an off condition.

One factor that may cause an emitter site to emit electrons unexpectedly is the response of semiconductor junctions in the FED to photons generated by the luminescent display screen and photons present in the environment (e.g., lights, sunshine). In an FED, P/N junctions can be used to electrically isolate each pixel site and to construct row-column drive circuitry and current regulation circuitry for the pixel operation. During operation of the FED, some of the photons generated at a display screen as well as photons from the environment, may strike the semiconductor junctions on the substrate. This may affect the junctions by changing their electrical characteristics. In some cases this may cause an unwanted current to pass across the junction. This is one type of junction leakage in a FED that may adversely affect the address or activation of pixel sites and cause stray emission and a degraded image quality.

One possible situation is shown in Figure 1. Figure 1 illustrates a pixel site 10 of a field emission display FED) 13 and portions of adjacent pixel sites 10' on either side. The FED 13 includes a baseplate 11 having a substrate 12 formed of a material such as single crystal P-type silicon. A plurality of emitter sites 14 are formed on an N-type conductivity region 30 of the substrate 12. The P-type substrate 12 and N-type conductivity region 30 form a P/N junction. This type of junction can be combined with other circuit elements to form electrical devices, such as FETs, for activating and regulating current flow to the pixel sites 10 and 10'.

The emitter sites 14 are adapted to emit electrons 28 that are directed at a cathodoluminescent display screen 18 coated with a phosphor material 19. A gate electrode or grid 20, separated from the substrate 12 by an insulating layer 22, surrounds each emitter site 14. Support

structures 24, also referred to as spacers, are located between the baseplate 11 and the display screen 18.

5 An electrical source 26 establishes a voltage differential between the emitter sites 14 and the grid 20 and display screen 18. The electrons 28 from activated emitter sites 14 generate the emission of photons from the phosphor material contained in a corresponding pixel site 10 of the display screen 18. To form a particular image,
10 it may be necessary to illuminate pixel site 10 while adjacent pixel sites 10' on either side remain dark.

A problem may occur however, when photons 32 (i.e., light) generated by a light source 33, sunlight or other
15 environmental factors, strike the semiconductor junctions formed in the substrate 12. In addition, photons 32 from an illuminated pixel site 10 may strike the junctions formed at the N-type conductivity regions 30 on the adjacent pixel sites 10'. The photons 32 are capable of
20 passing through the spacers 24, grid 20 and insulating layer 22 of the FED 13, because often these layers are formed of materials that are translucent to most wave lengths of light. As an example, the spacers 24 may be formed of a translucent polyimide, such as kapton or silicon
25 nitride. The insulative layer 22 may be formed of translucent silicon dioxide, silicon nitride or silicon oxynitride. The grid 20 may be formed of translucent polysilicon.

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The exposure to photons from the display screen 18 and environment may change the properties of some junctions on the substrate 12 associated with the emitter sites 14. This in turn may cause current flow and initiate electron
35 emission from the emitter sites 14 on the adjacent pixel sites 10'. The electron emission may cause the adjacent

pixel sites 10' to illuminate when a dark background may be required. This will cause a degraded or blurry image. Besides isolation and activation problems, light from the environment and display screen 18 striking junctions on the substrate 12, may cause other problems in addressing and regulating current flow to the emitter sites 14 of the FED cell 13.

In experiments conducted by the inventors, junction leakage currents have been measured in the laboratory as a function of different lighting conditions at the junction. At a voltage of about 50 volts and depending on the intensity of light directed at a junction, junction leakage may be on the order of picoamps (i.e., 10^{-12} amps) for dark conditions to microamps (i.e., 10^{-6} amps) for well lit conditions. For a FED, even relatively small leakage currents (i.e., picoamps) will adversely affect the image quality. The treatise entitled "Physics of Semiconducting Devices" by S. M. Sze, copyright 1981 by John Wiley and Sons, Inc., at paragraphs 1.6.1 to 1.6.3, briefly describes the effect of photon energy on semiconductor junctions.

In the construction of screens for cathode ray tubes, screen aluminizing processes are used to form with a mirror like finish on the inside surface of the screen. This layer of aluminum reflects light towards the viewer and away from the rear of the tube. In U.S. Patent No. 3,814,968 to Nathanson et al., a similar process is utilized in field emitter cathodes to prevent radiation emitted at the screen from being directed back onto the photocathode and emitter sites. One problem with this prior art approach is that with field emission displays (FEDs), cathode voltages are relatively low (e.g., 200 volts). However, an aluminum layer formed on the inside surface of the display screen cannot be easily penetrated by electron emitted at these low voltages. Therefore this

approach is not entirely suitable in a FED for preventing junction leakage caused by screen and environment photon emission.

5 It is also known in the art to construct FEDs with circuit traces formed of an opaque material, such as chromium, that overlie the semiconductor junctions contained in the FED baseplate. As an example, U.S. Patent No. 3,970,887 to Smith et al., describes such a structure
10 (see Figure 8). However, these circuit traces are constructed to conduct signals, and are not specifically adapted for isolating the semiconductor junctions from photon bombardment. Accordingly, most of the junction areas are left exposed to photon emission and the resultant
15 junction leakage.

 In view of the foregoing, there is a need in the art for improved methods for preventing junction leakage in FEDs. It is therefore an object of the present invention
20 to provide an improved method of constructing a FED with a light blocking element that prevents photons generated in the environment and by a display screen of the FED from effecting semiconductor junctions on a baseplate of the FED. It is a still further object of the present invention
25 to provide an improved method of constructing FEDs using an opaque layer that protects semiconductor junctions on a baseplate from light and which may also perform other circuit functions. It is a still further object of the present invention to provide a FED with improved junction
30 leakage characteristics using techniques that are compatible with large scale semiconductor manufacture.

 In accordance with the present invention, an improved method of constructing FEDs for flat panel displays and
35 other electronic equipment is provided. The method, generally stated, comprises the formation of a light

blocking element between a cathodoluminescent display screen and baseplate of the FED. The light blocking element protects semiconductor junctions on a substrate of the FED from photons generated in the environment and by the display screen. The light blocking element may be formed as an opaque layer adapted to absorb or reflect light. In addition to protecting the semiconductor junctions from the effects of photons, the opaque layer may serve other circuit functions. The opaque layer, for example, may be patterned to form interlevel connecting lines for circuit components of the FED.

In an illustrative embodiment, the light blocking element is formed as an opaque light absorbing material deposited on a baseplate for the FED. As an example, a metal such as titanium that tends to absorb light can be deposited on the baseplate of a FED. Other suitable opaque materials include insulative light absorbing materials such as carbon black impregnated polyimide, manganese oxide and manganese dioxide. Moreover, such a light absorbing layer may be patterned to cover only the areas of the baseplate that contain semiconductor junctions. The light blocking element may also be formed of a layer of a material, such as aluminum, adapted to reflect rather than absorb light.

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Other objects, advantages and capabilities of the present invention will become more apparent as the description proceeds.

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Figure 1 is a cross-sectional schematic view of a prior art FED showing a pixel site and portions of adjacent pixel sites; and

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Figure 2 is a cross-sectional schematic view of an emitter site for a FED having a light blocking element formed in accordance with the invention.

Referring now to Figure 2, an emitter site 40 of a FED is illustrated schematically. The emitter site 40 can be formed with one or more sharpened tips as shown or with one or more sharpened cones, apexes or knife edges. The emitter site 40 is formed on a substrate 36. In the illustrative embodiment, the substrate 36 is single crystal P-type silicon. Alternately the emitter site 40 may be formed on another substrate material or on an intermediate layer formed of a glass layer or an insulator-glass composite. In the illustrative embodiment, the emitter site 40 is formed on an N-type conductivity region 58 of the substrate 36. The N-type conductivity region may be part of a source or drain of an FET transistor that controls the emitter site 40. The N-type conductivity region 58 and P-type substrate 36 form a semiconductor P/N junction.

Surrounding the emitter site 40 is a gate structure or grid 42. The grid 42 is separated from the substrate 36 by an insulating layer 44. The insulating layer 44 includes an etched opening 52 for the emitter site 40. The grid 42 is connected to conductive lines 60 formed on an interlevel insulating layer 62. The conductive lines 60 are embedded in an insulating and/or passivation layer 66 and are used to control operation of the grid 42 or other circuit components.

A display screen 48 is aligned with the emitter site 40 and includes a phosphor coating 50 in the path of electrons 54 emitted by the emitter site 40. An electrical source 46 is connected directly or indirectly to the emitter site 40 which functions as a cathode. The electrical source 46 is also connected to the grid 42 and to the display screen 48 which function as an anode.

When a voltage differential is generated by the source 46 between the emitter site 40, the grid 42 and the, display screen 48, electrons 54 are emitted at the emitter site 40. These electrons 54 strike the phosphor coating 50 on the display screen 48. This produces the photons 56 that illuminate the display screen 48.

For all of the circuit elements described thus far, fabrication processes that are known in the art can be utilized. As an example, U.S. Patent No. 5,186,670 to Doan et al., describes suitable processes for forming the substrate 36, emitter site 40 and grid 42.

The substrate 36 and grid 42 and their associated circuitry form the baseplate 70 of the FED. The silicon substrate 36 contains semiconductor devices that control the operation of the emitter site 40. These devices are combined to form row-column drive circuitry, current regulation circuitry, and circuitry for electrically activating or isolating the emitter site 40. As an example, the previously cited U.S. Patent No. 5,210,472 to Casper et al. describes pairs of MOSFETs formed on a silicon substrate and connected in series to emitter sites. One of the series connected MOSFETs is gated by a signal on the row line. The other MOSFET is gated by a signal on the column line.

In accordance with the present invention, a light blocking layer 64 is formed on the baseplate 70. The light blocking layer 64 prevents light from the environment and light generated at the display screen 48 from striking semiconductor junctions, such as the junction formed by the N-type conductivity region 58, on the substrate 36. A passivation layer 72 is formed over the light blocking layer 64.

The light blocking layer 64 is formed of a material that is opaque to light. The light blocking layer 64 may be either a conductive or an insulative material. In addition, the light blocking layer 64 may be either light absorptive or light reflective. Suitable materials include metals such as titanium that tend to absorb light, or a highly reflective metal such as aluminum. Other suitable conductive materials include aluminum-copper alloys, refractory metals and refractory metal silicides. In addition, suitable insulative materials include manganese oxide, manganese dioxide or a chemical polymer such as carbon black impregnated polyimide. These insulative materials tend to absorb light and can be deposited in a relatively thick layer.

For a light blocking layer 64 formed of metal, a deposition technique such as CVD, sputtering or electron beam deposition (EBD) may be used. For a light blocking layer 64 formed of an insulative material or chemical polymer, liquid deposition and cure processes can be used to form a layer having a desired thickness.

The light blocking layer 64 may be blanket deposited to cover substantially all of the baseplate 70 or it may be patterned using a photolithography process to protect predetermined areas on the substrate 36 (i.e., areas occupied by junctions). Furthermore, the light blocking layer 64 may be constructed to serve other circuit function as long as the area occupied by semiconductor junctions is substantially protected. As an example, the light blocking layer 64 may be patterned to function as an interlevel connector.

A process sequence for forming an emitter site 40 with the light blocking layer 64 is as follows:

1. Form electron emitter sites 40 as protuberances, tips, wedges, cones or knife edges by masking and etching the silicon substrate 36.

5 2. Form n-type conductivity regions 58 for the emitter sites 40 by patterning and doping a single crystal silicon substrate 36.

10 3. Oxidation sharpen the emitter sites 40 using a suitable oxidation process.

15 4. Form the insulating layer 44 by the conformal deposition of a layer of silicon dioxide. Other insulating materials such as silicon nitride and silicon oxynitride may also be used.

20 5. Form the grid 42 by deposition of doped polysilicon followed by chemical mechanical planarization (CMP) for self aligning the grid and emitter site 40. Such a process is detailed in U.S. Patent No. 5,229,331 to Rolfson et al. In place of polysilicon, other conductive materials such as chromium, molybdenum and other metals may also be used.

25 6. Photopattern and dry etch the grid 42.

30 7. Form interlevel insulating layer 62 on grid 42. Form contacts through the insulating layer 62 by photopatterning and etching.

35 8. Form metal conductive lines 60 for grid connections and other circuitry. Form passivation layer 66.

35 9. Form the light blocking layer 64. For a light blocking layer formed of titanium or other metal, the light

blocking layer may be deposited to a thickness of between 2000 Å to 4000 Å. Other materials may be deposited to a thickness suitable for that particular material.

5 10. Photopattern and dry etch the light blocking layer 64, passivation layer 66 and insulating layer 62 to open emitter and bond pad connection areas.

10 11. Form passivation layer 72 on light blocking layer 64.

12. Form openings through the passivation layer 72 for the emitter sites 40.

15 13. Etch the insulating layer 44 to open the cavity 52 for the emitter sites 40. This may be accomplished using photopatterning and wet etching. For silicon emitter sites 40 oxidation sharpened with a layer of silicon dioxide, one suitable wet etchant is diluted HF acid.

20 14. Continue processing to form spacers and display screen.

25 Thus the invention provides a method for preventing junction leakage in a FED utilizing a light blocking element formed on the baseplate of the FED. It is understood that the above process sequence is merely exemplary and may be varied depending upon differences in the baseplate, emitter site and grid materials and their associated formation technology.

30 While the method of the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

All of the cited U.S. Patents and technical articles are hereby incorporated by reference as if set forth in their entirety.



THIS SHEET HAS BEEN
REPLACED

CLAIMS

1. In a field emission display having a baseplate, emitter sites and semiconductor junctions, a method for
5 reducing junction leakage from the semiconductor junctions, said method comprising:

forming a light blocking element on the baseplate
between the semiconductor junctions and the
display screen in order to protect the
10 semiconductor junctions from photon bombardment from the display screen and from an environment of the field emission display.

2. The method as recited in claim 1 and wherein the
15 light blocking element comprises a light absorbing material.

3. The method as recited in claim 1 and wherein the
light blocking element comprises a light reflecting
20 material.

4. The method as recited in claim 1 and wherein the
light blocking element comprises a layer of material
blanket deposited over the baseplate of the field emission
25 display.

5. The method as recited in claim 1 and wherein the
light blocking element comprises a layer of material



deposited and patterned to protect predetermined areas of the baseplate.

6. The method as recited in claim 1 and wherein the
5 light blocking element comprises a layer of a conductive material deposited and patterned to protect the semiconductor junctions and to conduct electrical signals within the field emission display.

10 7. A method for forming a field emission display, comprising:

providing a baseplate having semiconductor junctions;
forming emitter sites on the baseplate electrically
connected to the semiconductor junctions and to
15 an electrical source said emitter sites aligned with a display screen having a phosphor coating;
forming a conductive grid for the emitter sites said
conductive grid connected to the source and
separated from the baseplate by an insulating
20 layer and adapted to establish a voltage differential to generate an electron emission from the emitter sites and photon emission from the display screen; and

forming an opaque light blocking element on the
25 baseplate for blocking photons directed at the semiconductor junctions in order to protect the junctions from junction leakage caused by the



photons and improve an image at the display screen.

8. The method of fabricating a field emission display as recited in claim 7 and wherein the light blocking element is formed of a material selected from the group of materials consisting of metal, a polyimide impregnated with carbon black, manganese dioxide and manganese oxide.

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9. A method for forming a field emission display, comprising:

forming emitter sites on a baseplate;

forming semiconductor junctions on the baseplate with the emitter tips electrically connected to the semiconductor junctions and to an electrical source;

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forming conductive gate elements for the emitter sites with the gate elements connected to the source and separated from the baseplate by an insulating layer said gate elements adapted to establish a voltage differential to generate an electron emission from selected emitter sites;

20

forming an opaque light blocking element on the baseplate for blocking photons directed at the semiconductor junctions said opaque light

25



blocking element formed as a layer of material deposited on the baseplate; and forming a display screen with a phosphor coating said display screen spaced from the baseplate and aligned with one or more emitter sites for receiving electrons emitted by the emitter sites to generate photons for lighting the display screen.

10 10. The method as recited in claim 9 and wherein the light blocking element is patterned layer for protecting predetermined areas of the baseplate.

15 11. The method as recited in claim 9 and wherein the light blocking element is a light absorbing material.

12. The method as recited in claim 9 and wherein the light blocking element is a light reflecting material.