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MEMORY CONTROLLER WHICH EXECUTES READ AND WRITE COMMANDS OUT OF ORDER

Abstract of the Disclosure

A memory subsystem includes a posted write buffer for dynamic random access memories (DRAMs). The posted write buffer includes read around logic to enable read accesses to be processed in advance of posted writes. Data are transferred from the posted write buffer to the DRAMs on a general first-in/first out basis; however, in order to take advantage of page mode operation, posted writes having the same row address as a current memory access are given priority over other posted writes such that the posted writes may be written out of order. In addition, comparisons are made between addresses of incoming read accesses and addresses of posted writes in order to expedite the transfer of posted writes having the same row addresses to memory in order to service the incoming read access on a timely basis. An improved write access buffer permits posted writes to be transferred to the DRAMs out of order without losing track of the skipped posted writes.

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