## CLAIMS

We claim:

1. A computer program product for detecting a Decimal Floating Point Quantum exception, the computer program product comprising:

computer readable storage medium having program code embodied therewith, the program code readable by a computer processor to perform a method comprising:

executing, by the processor, an instruction, the executing comprising:

obtaining, by at least one processor of a processing environment, at least one Decimal Floating Point Operand;

performing a decimal floating point operation on the at least one decimal floating point operand to produce a decimal floating point result having a quantum;

determining a preferred quantum based upon the operation and on the at least one decimal floating point operand;

based on the determining that the quantum of the decimal floating point result is different from the preferred quantum, providing an output indicating a quantum exception; and

based on the determining that the quantum of the decimal floating point result is the same as the preferred quantum, providing an output without a quantum exception.

2. The computer program product of claim 1, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control Register (FPC) is zero.

3. The computer program product of claim 2 further comprising writing the output to a result register and continuing with normal operation.

4. The computer program product of claim 1, wherein indicating a quantum exception comprises a trap action, the trap action occurring when the quantum exception is recognized and the quantum exception mask bit in the FPC register is one.

5. The computer program product of claim 1, further comprising writing the output to a result register; setting an exception code; and taking a program interrupt handler.

6. The computer program product of claim 1 wherein providing an output without a quantum exception further comprises: writing the result to a register; not setting a flag; not setting an exception code; and continuing with normal operation.

7. A computer system for detecting a Decimal Floating Point Quantum exception, the system comprising:

a memory; and

a processor configured to communicate with the memory, wherein the computer system is configured to perform a method, the method comprising:

executing, by the processor, an instruction, the executing comprising:

obtaining, by at least one processor of a processing environment at least one Decimal Floating Point Operand;

performing a decimal floating point operation on the at least one decimal floating point operand to produce a decimal floating point result having a quantum;

determining a preferred quantum based upon the operation and on the at least one decimal floating point operand;

based on the determining that the quantum of the decimal floating point result is different from the preferred quantum, providing an output indicating a quantum exception; and

based on the determining that the quantum of the decimal floating point result is the same as the preferred quantum, providing an output without a quantum exception.

8. The system of claim 7, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control Register (FPC) is zero.

9. The system of claim 8 further comprising writing the output to a result register and continuing with normal operation.

10. The system of claim 7, wherein indicating a quantum exception comprises a trap action, the trap action occurring when the quantum exception is recognized and the quantum exception mask bit in the FPC register is one.

11. The system of claim 7, further comprising: writing the output to a result register; setting an exception code; and taking a program interrupt handler.

12. The system of claim 7, wherein providing an output without a quantum exception further comprises: writing the result to a register; not setting a flag; not setting an exception code; and continuing with normal operation.

13. A method for executing a machine instruction in a central processing unit, the machine instruction being defined for computer execution according to a computer architecture, said method comprising:

obtaining, by at least one processor of a processing environment, at least one Decimal Floating Point Operand;

performing a decimal floating point operation on the at least one decimal floating point operand to produce a decimal floating point result having a quantum;

determining a preferred quantum based upon the operation and on the at least one decimal floating point operand;

based on the determining that the quantum of the decimal floating point result is different from the preferred quantum, providing an output indicating a quantum exception; and

based on the determining that the quantum of the decimal floating point result is the same as the preferred quantum, providing an output without a quantum exception.

14. The method of claim 13, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control Register (FPC) is zero.

15. The method of claim 14 further comprising writing the output to a result register and continuing with normal operation.

16. The method of claim 13, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control Register (FPC) is zero. The method of claim 10, wherein indicating a quantum exception comprises a trap action, the trap

action occurring when the quantum exception is recognized and the quantum exception mask bit in the FPC register is one.

17. The method of claim 13, further comprising: writing the output to a result register; setting an exception code; and taking a program interrupt handler.

18. The method of claim 13, wherein providing an output without a quantum exception further comprises: writing the result to a register; not setting a flag; not setting an exception code; and continuing with normal operation.

## CLAIMS

We claim:

1. A computer program product for detecting a Decimal Floating Point Quantum exception, the computer program product comprising:

a computer readable storage medium having program code embodied therewith, the program code readable by a computer processor to perform a method comprising:

executing, by the processor, an instruction, the executing comprising:

obtaining, by at least one processor of a processing environment, at least one decimal floating point operand;

performing a decimal floating point operation on the at least one decimal floating point operand to produce a decimal floating point result having a quantum;

determining a preferred quantum based upon the operation and on the at least one decimal floating point operand;

based on determining that the quantum of the decimal floating point result is different from the preferred quantum, providing an output indicating a quantum exception,

wherein providing an output indicating a quantum exception comprises:

determining whether a quantum exception mask bit is set;

based on determining that the quantum exception mask bit is not set, storing the decimal floating point result and setting a quantum exception flag bit; and

based on determining that the quantum exception mask bit is set, storing the decimal floating point result and performing a trap operation; and

based on determining that the quantum of the decimal floating point result is the same as the preferred quantum, providing an output without a quantum exception.

2. The computer program product of claim 1, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control (FPC) register is zero.

3. The computer program product of claim 2, the executing further comprising writing the output to a result register and continuing with normal operation.

4. The computer program product of claim 1, wherein indicating a quantum exception comprises a trap action, the trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control (FPC) register is one.

5. The computer program product of claim 1, the executing further comprising:
writing the output to a result register; setting an exception code; and
trapping to a program interrupt handler.

6. The computer program product of claim 1, wherein providing an output without a quantum exception further comprises:
writing the result to a register; not setting a flag; not setting an exception code; and
continuing with normal operation.

7. A computer system for detecting a Decimal Floating Point Quantum exception, the system comprising:
a memory; and
a processor configured to communicate with the memory, wherein the computer system is configured to perform a method, the method comprising:
executing, by the processor, an instruction, the executing comprising:
obtaining, by at least one processor of a processing environment at least one decimal floating point operand;
performing a decimal floating point operation on the at least one decimal floating point operand to produce a decimal floating point result having a quantum;

determining a preferred quantum based upon the operation and on the at least one decimal floating point operand;

based on determining that the quantum of the decimal floating point result is different from the preferred quantum, providing an output indicating a quantum exception, wherein providing an output indicating a quantum exception comprises:

determining whether a quantum exception mask bit is set;

based on determining that the quantum exception mask bit is not set, storing the decimal floating point result and setting a quantum exception flag bit; and

based on determining that the quantum exception mask bit is set, storing the decimal floating point result and performing a trap operation; and

based on determining that the quantum of the decimal floating point result is the same as the preferred quantum, providing an output without a quantum exception.

8. The system of claim 7, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control (FPC) register is zero.

9. The system of claim 8, the executing further comprising writing the output to a result register and continuing with normal operation.

10. The system of claim 7, wherein indicating a quantum exception comprises a trap action, the trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control (FPC) register is one.

11. The system of claim 7, the executing further comprising: writing the output to a result register; setting an exception code; and trapping to a program interrupt handler.

12. The system of claim 7, wherein providing an output without a quantum exception further comprises: writing the result to a register; not setting a flag; not setting an exception code; and continuing with normal operation.

13. A method for executing a machine instruction in a central processing unit, the machine instruction being defined for computer execution according to a computer architecture, said method comprising:

obtaining, by at least one processor of a processing environment, at least one decimal floating point operand;

performing a decimal floating point operation on the at least one decimal floating point operand to produce a decimal floating point result having a quantum;

determining a preferred quantum based upon the operation and on the at least one decimal floating point operand;

based on determining that the quantum of the decimal floating point result is different from the preferred quantum, providing an output indicating a quantum exception,

wherein providing an output indicating a quantum exception comprises:

determining whether a quantum exception mask bit is set;

based on determining that the quantum exception mask bit is not set, storing the decimal floating point result and setting a quantum exception flag bit; and

based on determining that the quantum exception mask bit is set, storing the decimal floating point result and performing a trap operation; and

based on determining that the quantum of the decimal floating point result is the same as the preferred quantum, providing an output without a quantum exception.

14. The method of claim 13, wherein indicating a quantum exception comprises a non trap action, the non trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control (FPC) register is zero.

15. The method of claim 14, further comprising writing the output to a result register and continuing with normal operation.

16. The method of claim 13, wherein indicating a quantum exception comprises a trap action, the trap action occurring when the quantum exception is recognized and a quantum exception mask bit in a Floating Point Control (FPC) register is one.

17. The method of claim 13, further comprising: writing the output to a result register; setting an exception code; and trapping to a program interrupt handler.

18. The method of claim 13, wherein providing an output without a quantum exception further comprises: writing the result to a register; not setting a flag; not setting an exception code; and continuing with normal operation.

19. The computer program product of claim 1, the method further comprising:
determining whether the quantum exception flag bit is set; and
based on determining that the quantum exception flag bit is set, processing a previously detected quantum exception.

20. The system of claim 7, the method further comprising:
determining whether the quantum exception flag bit is set; and
based on determining that the quantum exception flag bit is set, processing a previously detected quantum exception.

21. The method of claim 13, further comprising:
determining whether the quantum exception flag bit is set; and
based on determining that the quantum exception flag bit is set, processing a previously detected quantum exception.