METHODS OF FORMING RECESSED ACCESS DEVICES

TECHNICAL FIELD

[0001] This invention pertains to methods of forming recessed access devices associated with semiconductor constructions.

BACKGROUND OF THE INVENTION

[0002] A semiconductor transistor device is a device comprising a gate which interconnects a pair of source/drain regions with one another through a channel controlled by the gate. Transistor devices are common circuit devices of semiconductor constructions. For instance transistor devices can be incorporated into memory structures, including, for example, dynamic random access memory (DRAM) and static random access memory (SRAM).

[0003] A continuing goal in semiconductor fabrication is to increase a level of integration, and thus decrease the amount of semiconductor real-estate consumed by devices. Decreasing the size of transistor devices, however, leads to numerous difficulties. For instance, as the channel-length of a transistor device is decreased, numerous problems occur in attempting to control electron flow between source/drain regions on opposing sides of the channel. These problems are generically referred to as short-channel effects.

[0004] One approach that may have utility for overcoming short-channel problems is to recess transistor devices within a substrate so that the devices consume less real-estate than if they were non-recessed, and yet have relatively long channels. A non-recessed transistor device is shown in Fig. 1, and a recessed device is shown in Fig. 2 for comparison to the non-recessed device.

[0005] Referring initially to Fig. 1, a semiconductor construction 10 is illustrated to comprise a substrate 12. The substrate 12 can comprise, for example, monocrystalline silicon lightly-doped with background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in

assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0006] A transistor device 14 is supported by the substrate. The transistor device includes a gate 16 spaced from substrate 12 by a dielectric material 18; includes sidewall spacers 24 along sidewalls of the gate; includes a pair of source/drain regions 20 on opposing sides of the gate; and includes a channel region 22 between the source/drain regions.

[0007] The gate 16 can comprise various electrically conductive materials, including, for example, various metals, metal compositions, and/or conductively-doped silicon or other conductively-doped semiconductor material. Dielectric material 18 can comprise any suitable material or combination of materials, and typically will comprise, consist essentially of, or consist of silicon dioxide. Sidewall spacers 24 can comprise any suitable compositions or combination of compositions, and typically will comprise one or both of silicon nitride and silicon dioxide. Source/drain regions 20 can comprise conductively-doped regions within monocrystalline substrate 12, and can comprise heavily-doped regions with lightly-doped extensions. For instance, the source/drain regions 20 can comprise either heavily n-type doped regions or heavily p-type doped regions, and can comprise lightly-doped portions extending under sidewalls 24. Channel region 22 is doped with a threshold voltage implant, and operably interconnects the source/drain regions 20 with one another when sufficient current passes through gate 16.

[0008] Fig. 2 shows a construction 30 comprising a semiconductor substrate 32 and a transistor 34 supported by the substrate. The transistor comprises a gate 36 extending within the substrate, a dielectric material 38 between the gate and the substrate, source/drain regions 40 within the substrate proximate the gate, and a channel region 42 extending around a lowermost portion of the gate and interconnecting the source/drain regions 40 with one another. Although not shown, sidewall spacers can be provided proximate gate 36 similar to the spacers 24 discussed above with reference to Fig. 1.

[0009] The substrate 32, dielectric material 38, gate 36 and source/drain regions 40 can comprise identical materials to those discussed above regarding the substrate 12, gate

16, dielectric material 18 and source/drain regions 20 of Fig. 1. Also, a threshold voltage implant can be provided within channel region 42 similar to the threshold voltage implant provided within region 22 of Fig. 1.

[0010] A difference between the recessed device construction of Fig. 2 relative to the non-recessed device construction of Fig. 1 is that the channel region 42 of the device of Fig. 2 is lengthened by virtue of the channel region extending around a recessed portion of the gate 36. Such can reduce short-channel effects for the transistor device 34 of Fig. 2 relative to the device 14 of Fig. 1.

[0011] Although recessed access devices have advantages relative to non-recessed devices in terms of the packing density that can be achieved while avoiding short-channel effects, there are various problems encountered in large-scale fabrication of recessed access devices which are to be addressed if recessed access devices are to become commercially feasible. Accordingly, it is desired to develop new methodology for large-scale fabrication of recessed access devices. One application for recessed access devices is in memory arrays, such as, for example, DRAM arrays. Accordingly, it would be further desirable if methodologies developed for large-scale fabrication of recessed access devices were applicable to fabrication of memory arrays.

SUMMARY OF THE INVENTION

[0012] In one aspect, the invention includes a method of forming recessed access devices. A semiconductor substrate is provided. Recessed access device trenches are formed within the substrate. A pair of the recessed access device trenches are adjacent one another. Electrically conductive gate material is formed within the recessed access device trenches. Source/drain regions are formed proximate the conductive gate material. The conductive gate material and source/drain regions together form an adjacent pair of recessed access devices (specifically, a pair of recessed access transistors). After the recessed access device trenches are formed within the substrate, an isolation region trench is formed between the adjacent recessed access devices. The isolation region trench is filled with electrically insulative material to form a trenched isolation region.

[0013] In one aspect, the invention includes another method of forming recessed access devices. A semiconductor construction is provided, and recessed access device

trenches are formed within the substrate. The recessed access device trenches are filled with a first electrically insulative material. The first electrically insulative material is patterned into a mask defining a plurality of access device regions. The access device regions are islands surrounded by isolation regions. The access device regions comprise only portions of the recessed access device trenches. The substrate is etched within the isolation regions to recess the substrate of the isolation regions. The recessed substrate is covered with a second electrically insulative material to cover the isolation regions. At least a majority of the first electrically insulative material is removed while leaving at least a majority of the second electrically insulative material. Subsequently, gate material is formed within the portions of the recessed access device trenches comprised by the access device regions.

[0014] In one aspect, the invention includes yet another method of forming recessed access devices. A semiconductor substrate is provided, and a first patterned mask is formed over the substrate. The first patterned mask has openings extending therethrough defining first locations for trenches of recessed access devices. The substrate is etched in the first locations to form recessed access device trenches extending into the substrate. The recessed access device trenches are filled with a gate material. A first electrically insulative material is formed over the first patterned mask and over the gate material. The first electrically insulative material is patterned into a mask defining a plurality of access device regions. The access device regions are islands surrounded by isolation regions. The access device regions comprise only portions of the recessed access device trenches. The substrate is etched to recess the substrate of said isolation regions. The recessed substrate is covered with a second electrically insulative material. The first electrically insulative material is removed. Subsequently, a plurality of conductive lines are formed. Individual conductive lines extend across multiple access device regions and electrically interconnect gate material of the multiple access device regions with one another.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0016] Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment illustrating a prior art transistor device.

[0017] Fig. 2 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment illustrating another prior art transistor device.

[0018] Figs. 3 and 4 are a diagrammatic top view and diagrammatic cross-sectional side view of a semiconductor wafer fragment illustrated at a preliminary processing stage of an exemplary aspect of the present invention. The cross-section of Fig. 4 is along the line 4-4 of Fig. 3.

[0019] Figs. 5 and 6 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 3 and 4. The cross-section of Fig. 6 is along the line 6-6 of Fig. 5.

[0020] Figs. 7 and 8 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 5 and 6. The cross-section of Fig. 8 is along the line 8-8 of Fig. 7.

[0021] Figs. 9 and 10 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 7 and 8. The cross-section of Fig. 10 is along the line 10-10 of Fig. 9.

[0022] Figs. 11 and 12 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 9 and 10. The cross-section of Fig. 12 is along the line 12-12 of Fig. 11.

[0023] Figs. 13 and 14 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 11 and 12. The cross-section of Fig. 14 is along the line 14-14 of Fig. 13.

[0024] Figs. 15 and 16 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 13 and 14. The cross-section of Fig. 16 is along the line 16-16 of Fig. 15.

[0025] Figs. 17 and 18 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 15 and 16. The cross-section of Fig. 18 is along the line 18-18 of Fig. 17.

[0026] Figs. 19 and 20 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 17 and 18. The cross-section of Fig. 20 is along the line 20-20 of Fig. 19.

[0027] Figs. 21 and 22 illustrate the fragments of Figs. 3 and 4, respectively, at a processing stage subsequent to that of Figs. 19 and 20. The cross-section of Fig. 22 is along the line 22-22 of Fig. 21.

[0028] Figs. 23 and 24 are a diagrammatic top view and diagrammatic cross-sectional side view of a semiconductor wafer fragment shown at a preliminary processing stage of an exemplary aspect of a second embodiment of the present invention. The cross-section of Fig. 24 is along the line 24-24 of Fig. 23.

[0029] Figs. 25 and 26 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 23 and 24. The cross-sectional view of Fig. 26 is along the line 26-26 of Fig. 25.

[0030] Figs. 27 and 28 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 25 and 26. The cross-section of Fig. 28 is along the line 28-28 of Fig. 27.

[0031] Figs. 29 and 30 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 27 and 28. The cross-section of Fig. 30 is along the line 30-30 of Fig. 29.

[0032] Figs. 31 and 32 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 29 and 30. The cross-section of Fig. 32 is along the line 32-32 of Fig. 31.

[0033] Figs. 33 and 34 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 31 and 32. The cross-section of Fig. 34 is along the line 34-34 of Fig. 33.

[0034] Figs. 35 and 36 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 33 and 34. The cross-section of Fig. 36 is along the line 36-36 of Fig. 35.

[0035] Figs. 37 and 38 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 35 and 36. The cross-section of Fig. 38 is along the line 38-38 of Fig. 37.

[0036] Figs. 39 and 40 illustrate the fragments of Figs. 23 and 24, respectively, at a processing stage subsequent to that of Figs. 37 and 38. The cross-section of Fig. 40 is along the line 40-40 of Fig. 39.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] The invention includes various methods for forming recessed access devices associated with semiconductor constructions. In particular aspects, structures are formed which contain recessed access devices and shallow trench isolation regions to electrically separate adjacent devices. Accordingly, recessed access device gate trenches and shallow trench isolation region trenches are fabricated. In contrast to prior art processes which form shallow trench isolation region trenches prior to formation of recessed access device gate trenches, some methods of the present invention form recessed access device gate trenches prior to forming shallow trench isolation region trenches. Although the recessed access device gate trenches are formed prior to the shallow trench isolation region trenches, gate material can be formed within the recessed access device gate trenches either prior to, or after, formation of the shallow trench isolation region trenches.

[0038] Exemplary aspects of the invention are described with reference to Figs. 3-40, with Figs. 3-22 pertaining to a first embodiment aspect of the invention, and Figs. 23-40 pertaining to a second embodiment aspect of the invention.

[0039] Referring initially to Figs. 3 and 4, a semiconductor construction 100 is illustrated at a preliminary processing stage of the first embodiment aspect of the present invention. Construction 100 comprises a substrate 102 which can, for example, comprise, consist essentially of, or consist of monocrystalline silicon lightly background-doped with p-type dopant.

[0040] A patterned mask 104 is formed over the substrate. The shown patterned mask comprises a first layer 106 comprising, consisting essentially of, or consisting of silicon dioxide; and a second layer 108 comprising, consisting essentially of, or consisting of silicon nitride. The mask 104 can be formed into the shown pattern by providing a photolithographically patterned photoresist (not shown) over mask 104, transferring a pattern from the photoresist to the materials of mask 104, and subsequently removing the photoresist.

[0041] The patterned mask 104 has openings 110 extending therethrough, with such openings defining locations for trenches of recessed access devices. The locations of openings 110 can be referred to as first locations in the discussion that follows.

[0042] Substrate 102 is etched through the first locations defined by mask 104 to form recessed access device trenches extending into substrate 102. In particular aspects, such trenches will extend into monocrystalline silicon of substrate 102. The trenches are shown having bottom peripheries 111 and a depth "D" from an uppermost surface of substrate 102 to the bottom peripheries. Such depth can be, for example, from about 100Å to about 2000Å.

[0043] In exemplary aspects of the invention, the substrate 102 can comprise monocrystalline silicon having p-well and/or n-well implants therein at the processing stage of Figs. 3 and 4. The layer 106 can be formed by oxidizing an uppermost surface of the monocrystalline silicon to form the layer 106 to consist essentially of, or consist of silicon dioxide, and to have a thickness of from about 50Å to about 100Å. The nitride cap 108 can comprise a thickness of from about 200Å to about 500Å, and typically will comprise a thickness of from about 300Å to about 500Å.

[0044] In some aspects (not shown) a critical dimension of the openings 110 can be shrunk with a two-step process. First, the masking layer 104 is etched to form the shown openings 110. Subsequently, nitride spacers are formed along sidewalls of the openings 110 by providing a silicon nitride layer extending along the sidewalls and within the openings, and subsequently subjecting such layer to anisotropic etching to form the spacers. The openings can then be extended into substrate 102 after forming such spacers, so that the openings have a smaller critical dimension than the dimension initially formed with photolithographic processing.

[0045] Referring next to Figs. 5 and 6, mask 104 (Figs. 3 and 4) is removed and a layer 112 is formed over substrate 102 and within trenches 110. The layer 112 can, for example, comprise, consist essentially of, or consist of silicon dioxide. In such aspects, layer 112 can be formed by thermally oxidizing an exposed upper surface of a monocrystalline substrate 102.

[0046] Referring next to Figs. 7 and 8, a layer 114 comprising, consisting essentially of, or consisting of silicon nitride is formed over layer 112. It is to be understood that the

compositions of layers 112 and 114 provided herein are exemplary compositions, and that the layers can comprise any suitable compositions. Layers 112 and 114 can together be referred to as a first insulative material provided to fill trenches 110. The trenches 110 are shown in dashed-line view in Fig. 7 to indicate the locations of the trenches beneath insulative material 114.

[0047] Referring next to Figs. 9 and 10, photolithographically patterned photoresist 116 is provided over the layer 114. The photoresist defines a pattern which is to be transferred into the first insulative material comprising layers 112 and 114. Subsequently, such pattern is transferred to layers 112 and 114 with a suitable etch, which patterns layers 112 and 114 into a mask. The mask defines a plurality of access device regions 120, 122, 124 and 126. The access device regions are islands surrounded by an isolation region 130. The access device regions 120, 122, 124 and 126 comprise only portions of the recessed access device trenches 110 that had been initially formed (i.e., the trenches of Figs. 7 and 8), with remaining portions of the trenches being within isolation region 130.

[0048] The shown access device regions 120, 122, 124 and 126 are substantially elliptical in the view of Fig. 9. The substantially elliptical access device regions have primary longitudinal elliptical axes, with an exemplary primary longitudinal elliptical axis being shown as an axis 121 within region 120. It is noted that the trenches 110 can be considered to comprise primary length axes extending along their lengths, with an exemplary length axis being illustrated as an axis 123 in Fig. 9. In the application illustrated in Fig. 9, the primary longitudinal elliptical axis 121 is canted relative to axis 123, and accordingly is not substantially orthogonal to the primary length axis 123. It is to be understood, however, that the invention also encompasses aspects (such as, for example, an aspect described with reference to Figs. 31 and 32 below) in which the primary longitudinal elliptical axis of an access device region is substantially orthogonal to the primary length axis of a recessed access device trench.

[0049] Referring next to Figs. 11 and 12, the substrate of isolation regions 130 is recessed with an etch. The etch removes portions of trenches 110 between recessed access device regions 120, 122, 124 and 126.

[0050] After the etch, the recessed substrate of isolation region 130 is at a depth "E" beneath an uppermost surface of substrate 102. In particular aspects, the substrate can be

recessed to a level beneath a lowestmost level of recessed access device trenches 110 such that depth "E" is at least about two-fold greater than the depth "D" of Fig. 4. Depth "E" can correspond to a depth of a shallow trench isolation region, and in particular aspects can be from about 500Å to about 3500Å.

[0051] Two of the trenches 110 of Fig. 12 can be considered to be adjacent to one another, and the isolation region 130 can be considered to be formed between such adjacent trenches. For instance, one of the adjacent trenches can be a trench labeled 131, and the other can be a trench labeled 133, and such trenches can be considered to be on opposing sides of a deep trench formed between them in isolation region 130. In the shown processing of the present invention, the adjacent recessed access device trenches 131 and 133 have been formed prior to formation of the deep trench between them.

[0052] Referring next to Figs. 13 and 14, photoresist 116 (Figs. 11 and 12) is removed, and subsequently an electrically insulative material 136 is formed over the recessed substrate of isolation region 130, as well as over layer 114 of the access device regions 120, 122, 124 and 126. The access device regions 120, 122, 124 and 126 are shown in dashed-line view in Fig. 13 to indicate the locations of such regions, but it is to be understood that the regions are beneath insulative material 136 at the processing stage of Fig. 13.

[0053] Material 136 can comprise any suitable composition or combination of compositions. In particular aspects, material 136 can correspond to a so-called shallow trench stack, and accordingly can comprise a thin layer of silicon dioxide along substrate 102, a thin silicon nitride liner over the silicon dioxide, and a thick silicon dioxide fill within the liner. In other words, insulative material 136 can primarily comprise silicon dioxide, with the bulk silicon dioxide of the material being separated from substrate 102 by a thin silicon nitride liner and a thin silicon dioxide liner. The bulk insulative composition of material 136 can, in some aspects, be a spin-on-dielectric.

[0054] In the view of Fig. 14, the dielectric-filled deep region 130 can be considered to comprise a trenched isolation region provided between recessed access device trenches 131 and 133.

[0055] Referring next to Figs. 15 and 16, material 136 is subjected to planarization (such as, for example, chemical-mechanical planarization) to remove the material from over

the layer 114, and to form a planarized upper surface 137 extending across material 136 and layer 114. The planarization of Figs. 15 and 16 can be considered to remove insulative material 136 from over layer 114, while leaving the insulative material 136 over the recessed substrate of isolation region 130.

[0056] Referring next to Figs. 17 and 18, layers 112 and 114 are removed from over substrate 102, while leaving the electrically insulative material 136. In some aspects, layers 112 and 114 can be together considered to comprise a first electrically insulative material, and it can be considered that at least the majority of such first electrically insulative material is removed while leaving at least a majority of a second electrically insulative material corresponding to the material 136. In the shown aspect, an entirety of the first electrically insulative material corresponding to layers 112 and 114 has been removed, but it is to be understood that the invention encompasses other aspects in which less than an entirety of such material is removed. For instance, if material 112 comprises silicon dioxide, the material 112 can be left to correspond to a gate oxide in subsequent processing. However, it can be advantageous if material 112 is removed, regardless of whether material 112 comprises silicon dioxide or not, in that such can allow a surface of substrate 102 to be cleaned prior to formation of the actual gate dielectric material. Accordingly, the material of layers 112 and 114 will typically correspond to sacrificial materials.

[0057] Dopant can be provided within substrate 102 at the processing stage of Figs. 17 and 18 if it is desired to form dopant wells, such as, for example, p-wells or n-wells.

[0058] Referring next to Figs. 19 and 20, gate dielectric material 140 is formed within recessed access device trenches 110, and subsequently conductive gate material 142 is formed over the gate dielectric material and within the trenches to fill the trenches. In the shown aspect of the invention, conductive gate material 142 comprises a first layer 144 and a second layer 146. The layers 144 and 146 join at an interface 147. Layer 144 can, for example, comprise, consist essentially of, or consist of conductively-doped silicon; and layer 146 can, for example, comprise, consist essentially of, or consist of one or more metal-containing compositions. The metal-containing compositions can be pure metal and/or metal-containing compounds. In particular aspects, layer 146 can comprise a stack of tungsten/tungsten silicide/titanium nitride, in descending order in the view of Fig. 20.

[0059] The shown gate material 142 not only fills the trenches 110, but also extends outside of such trenches. Further, the interface between the metal-containing compositions of layer 146 and the conductively-doped silicon of layer 144 (i.e., the interface 147) is outside of the trenches.

[0060] An electrically insulative cap 150 is formed over conductive gate material 142. Cap 150 can comprise any suitable composition or combination of compositions, and in particular aspects will comprise, consist essentially of, or consist of one or both silicon dioxide and silicon nitride.

[0061] The access device regions 120, 122, 124 and 126 are shown in dashed-line view in Fig. 19 to indicate that the regions are beneath insulative cap 150.

[0062] Referring next to Figs. 21 and 22, materials 140, 144, 146 and 150 are patterned into conductive lines extending across access device regions 120, 122, 124 and 126. More specifically, the materials 140, 144, 146 and 150 are patterned into a plurality of lines 160, 162, 164 and 166, with each of the lines extending across multiple access device regions and electrically connecting gates associated with different access device regions with one another.

[0063] Source/drain regions 170, 172, 174, 176, 178 and 180 are formed within substrate 102 and proximate the electrically conductive gate material 144. The source/drain regions can be doped to any suitable dopant type, and can comprise any suitable dopants. The source/drain regions can be formed by implanting dopant into substrate 102 to an appropriate depth. The conductive gate material and source/drain regions together form a plurality of transistor devices 180, 182, 184 and 186 supported by substrate 102. Such transistor devices correspond to recessed access devices having gates extending within the recessed access device trenches 110.

[0064] Each of transistor devices 180, 182, 184 and 186 can be considered to comprise a gate electrically connecting a pair of source/drain regions with one another. For instance, transistor device 180 can be considered to comprise a gate electrically connecting source/drain regions 170 and 172 with one another; device 182 can be considered to comprise a gate electrically connecting source/drain regions 172 and 174 with one another; device 184 can be considered to comprise a gate electrically connecting source/drain

regions 176 and 178 with one another; and device 186 can be considered to comprise a gate connecting source/drain regions 178 and 180 with one another.

[0065] The transistor devices can be incorporated into a dynamic random access memory (DRAM) array by connecting some of the paired source/drain regions to bitline contacts and others to storage node contacts (i.e. to capacitor storage nodes). In the shown aspect of the invention, source/drain regions 170, 174, 176 and 180 are connected to capacitor storage nodes 190, 192, 194 and 196, respectively; and source/drain regions 172 and 178 are connected to bitlines 198 and 200, respectively. Thus, the shown construction can be incorporated into a DRAM array.

[0066] Referring next to Figs. 23 and 24, such illustrate a semiconductor construction 300 at a preliminary processing stage of a second embodiment aspect of the present invention. In referring to the drawings associated with the second aspect embodiment of the invention, similar numbering will be used as was used above in describing the first aspect embodiment of the invention, where appropriate.

[0067] Construction 300 comprises the substrate 102, patterned mask 104 of layers 106 and 108, and trenches 110 described previously with reference to Figs. 3 and 4, and thus corresponds identically to the construction discussed above with reference to Figs. 3 and 4.

[0068] Referring next to Figs. 25 and 26, gate dielectric material 302 is formed to line the bottom of trenches 110, and subsequently gate material 304 is formed within the trenches and over the dielectric material 302.

[0069] Dielectric material 302 can, for example, comprise, consist essentially of, or consist of silicon dioxide. In such aspect, material 302 can be deposited, or can be formed by oxidizing exposed silicon from substrate 102 within trenches 110. Dielectric material 302 can be formed in two steps, if so desired, with one of the steps being to initially form a first silicon dioxide material within trenches 110, and the other step being to strip the first dielectric material from within the trench and form another dielectric material within the trench which can be a better quality silicon dioxide dielectric than that initially provided.

[0070] Gate material 304 can comprise, consist essentially of, or consist of silicon. The silicon can be conductively-doped as-deposited, or can be deposited in an non-

conductively-doped form and subsequently doped with an appropriate implant at a later processing stage.

[0071] The construction of Fig. 26 is shown to comprise a planarized upper surface 305 extending across gate material 304 and across insulative material 108. Such can be formed by initially providing gate material 304 to cover material 108 as well as to fill the trenches, and subsequently subjecting material 304 to planarization (such as, for example, chemical-mechanical polishing), to remove material 304 from over material 108 and form the planarized upper surface 305.

[0072] An enhancement implant and/or threshold voltage implant can be provided within substrate 102 prior to formation of gate material 304 within trenches 110, if desired.

[0073] Although gate material 304 is shown having a planarized surface coextensive with an uppermost surface of layer 108, it is to be understood that the gate material can also have a surface recessed below the elevational level of the uppermost surface of layer 108. In some aspects, it can be preferred that silicon-containing material 304 be recessed below the uppermost surface of layer 108.

[0074] Referring next to Figs. 27 and 28, uppermost surfaces of material 304 and layer 108 are subjected to oxidation to form an oxide 310 over layer 108, and an oxide 312 over layer 304. In particular aspects of the invention, layer 108 will comprise, consist essentially of, or consist of silicon nitride, and accordingly oxide 310 will comprise, consist essentially of, or consist of silicon oxynitride; and layer 304 will comprise, consist essentially of, or consist of silicon, and accordingly oxide 312 will comprise, consist essentially of, or consist of silicon dioxide. The oxides 310 and 312 can be formed to be from about 30Å thick to about 60Å thick.

[0075] Referring next to Figs. 29 and 30, an electrically insulative material 314 is provided over oxides 310 and 312. Layer 314 can, for example, comprise, consist essentially of, or consist of silicon nitride, and can be deposited to a thickness of from about 300Å to about 500Å. In some aspects of the invention, the compositions 310, 312 and 314 can be together considered to form an insulative material 316 provided over the first patterned mask 104 and gate material 304.

[0076] Trenches 110 are shown in dashed-line view in Fig. 29 to indicate the locations of the trenches.

[0077] Referring next to Figs. 31 and 32, material 316 is patterned into a mask defining a plurality of access device regions 320, 324, 326, 328, 330, 332, 334 and 336; and defining an isolation region 340 surrounding the access device regions. Patterning of material 316 can be accomplished by providing a photolithographically patterned photoresist mask (not shown) over material 316, transferring a pattern from the photoresist mask to material 316, and subsequently removing the photoresist mask.

[0078] After material 316 is patterned, substrate 102 is etched within isolation region 340 to recess the substrate of such isolation region. The recessed substrate of the isolation region is at an elevational level below the lowestmost elevational level of trenches 110, and in some aspects is at least two-fold deeper than the elevational level of trenches 110.

[0079] The etching within isolation region 340 removes gate material 304 from within the isolation region, while leaving the gate material within the access device regions 320, 324, 326, 328, 330, 332, 334 and 336. The etching within isolation region 340 can be accomplished with, for example, a reactive ion etch.

[0080] An oxide 342 and a nitride liner 344 are provided within the etched isolation region 340, and in the shown aspect also extend over material 314. Oxide 342 can, for example, comprise, consist essentially of, or consist of silicon dioxide along substrate 102; and nitride 344 can, for example, comprise, consist essentially of, or consist of silicon nitride. The oxide can be formed by oxidation of exposed materials of construction 300, and accordingly can comprise a different composition along substrate 102 than along materials 108 and 314; or alternatively can be formed by deposition. Oxidation can be preferred, in that such can repair plasma-induced damages that may have occurred during the reactive ion etch, and can also encroach into gate-dielectric at interfacial surfaces to provide low leakage between gate polysilicon and the bulk silicon of substrate 102. The oxide is preferably formed to a thickness of from about 30Å to about 80Å. The nitride liner 344 can be deposited over the oxide layer 342, and ultimately can function as a protective layer for a subsequent spin-on glass deposition process.

[0081] It is noted that the access device regions of Fig. 31 are shown to be elliptical similar to the access device regions of Fig. 9. However, unlike the access device regions of Fig. 9, the access device regions of Fig. 31 have primarily longitudinal elliptical axes which

are substantially orthogonal to primary length axes of recessed access device trenches 110.

[0082] Referring next to Figs. 33 and 34, dielectric material 350 is provided to fill recessed isolation region 340. Dielectric material 350 can be a spin-on glass. Dielectric material 350 can initially be formed to cover insulative material 316, as well as to fill recessed isolation region 340, and subsequently planarization (such as, for example, chemical-mechanical polishing) can be utilized to remove the dielectric material from over insulative material 316 and form the shown planarized surface 351 extending over dielectric material 350 and layer 314. In some aspects, insulative material 316 (comprising materials 314, 310 and 312) can be referred to as a first insulative material, and insulative material 350 can be referred to as a second insulative material.

[0083] Referring next to Figs. 35 and 36, layer 314 (Fig. 34) is removed. Such can be accomplished with a wet oxide etch to slightly recess the spin-on glass below the nitride of material 314, followed with a wet nitride strip to remove material 314. The wet nitride strip can selectively stop at the oxide materials 310 and 312.

[0084] Referring next to Figs. 37 and 38, a plurality of lines 370, 372, 374 and 376 are formed to extend across access device regions 320, 324, 326, 328, 330, 332, 334 and 336. The lines comprise a conductive material 380 and an insulative cap 382. Conductive material 380 can comprise, for example, a stack of titanium nitride/tungsten silicide/tungsten (in ascending order in the view of Fig. 38), and cap 382 comprise, consist essentially of, or consist of silicon nitride.

[0085] The lines can be formed by initially depositing suitable materials of layers 380 and 382 entirely across the uppermost surface of construction 300, and subsequently patterning the materials by: forming photolithographically patterned photoresist over the layers 380 and 382, transferring a pattern from the photoresist to the underlying layers 380 and 382, and subsequently removing the photoresist.

[0086] The construction of Figs. 37 and 38 can be incorporated into a DRAM array similarly to the construction of Figs. 21 and 22. Specifically, appropriate conductively-doped diffusion regions can be formed proximate transistor gates comprised by conductive gate material 144, and capacitor constructions and bitline constructions can be electrically coupled with the source/drain regions.

[0087] Figs. 39 and 40 illustrate an alternative aspect relative to that of Figs. 37 and 38. Specifically, construction 300 can be subjected to planarization prior to formation of lines 370, 372, 374 and 376. Such planarization removes layer 108 (Figs. 35 and 36), and forms the shown planarized surface 390. Planarized surface 390 is shown on material 106, but it is to be understood that the planarization can also extend through material 106. If the planarization extends through material 106, another dielectric material can be formed over substrate 102 in place of the material 106 prior to formation of the lines. The construction of Fig. 40 can be incorporated into a memory array in a manner similar to that discussed above regarding the construction of Fig. 39.

CLAIMS:

1. A method of forming recessed access devices associated with a semiconductor construction, comprising:

providing a semiconductor substrate;

forming recessed access device trenches within the substrate;

filling the recessed access device trenches with a first electrically insulative material;

patterning the first electrically insulative material into a mask defining a plurality of access device regions, the access device regions being islands surrounded by an isolation region; the access device regions comprising only portions of the recessed access device trenches;

etching into the substrate of said isolation region to recess the substrate of said isolation region;

covering the recessed substrate with a second electrically insulative material to cover the isolation region with the second electrically insulative material;

removing at least the majority of the first electrically insulative material while leaving at least the majority of the second electrically insulative material; and

after removing at least the majority of the first electrically insulative material, forming gate material within the portions of the recessed access device trenches comprised by the access device regions.

2. The method of claim 1 wherein the substrate comprises monocrystalline silicon, and wherein the recessed access device trenches extend into the monocrystalline silicon of the substrate.

3. The method of claim 1 wherein the first electrically insulative material comprises a silicon-nitride-containing layer over a silicon-dioxide-containing layer.

4. The method of claim 3 wherein the removing at least the majority of the first electrically insulative material removes both the silicon-nitride-containing layer and the silicon-dioxide-containing layer.

5. The method of claim 1 wherein the access device regions are substantially elliptical; wherein the substantially elliptical access device regions have primary longitudinal elliptical axes; wherein the recessed access device trenches have primary length axes; and wherein the primary longitudinal elliptical axes of the substantially elliptical access device regions are substantially orthogonal to the primary length axes of the recessed access device trenches.

6. The method of claim 1 wherein the access device regions are substantially elliptical; wherein the substantially elliptical access device regions have primary longitudinal elliptical axes; wherein the recessed access device trenches have primary length axes; and wherein the primary longitudinal elliptical axes of the substantially elliptical access device regions are not substantially orthogonal to the primary length axes of the recessed access device trenches.

7. The method of claim 1 wherein the covering the recessed substrate with a second electrically insulative material is accomplished by:

forming the second electrically insulative material over the first electrically insulative material and over the recessed substrate of the isolation region; and

planarizing the second electrically insulative material to remove the second electrically insulative material from over the first electrically insulative material while leaving the second electrically insulative material over the recessed substrate of the isolation region.

8. The method of claim 1 wherein the forming the gate material includes:

forming the gate material within said portions of the recessed access device trenches and over the second electrically insulative material; and

patterning the gate material to form lines of the gate material; individual lines extending across multiple of the access device regions.

9. The method of claim 8 further comprising forming the gate material as part of a stack of silicon, metal-containing material, and insulative capping material; and wherein the patterning simultaneously patterns the silicon, metal-containing material, and insulative capping material.

10. The method of claim 8 further comprising forming source/drain regions associated with gate material of the recessed device regions, the gate material comprising gates which electrically interconnect pairs of source/drain regions with one another; at least some of the paired source/drain regions comprising a bitline contact and a storage node contact and being incorporated into DRAM devices.

11. A method of forming recessed access devices associated with a semiconductor construction, comprising:

providing a semiconductor substrate;

forming a first patterned mask over the substrate, the first patterned mask having openings extending therethrough defining first locations for trenches of recessed access devices;

etching the substrate through said first locations to form recessed access device trenches extending into the substrate;

filling the recessed access device trenches with a gate material;

forming a first electrically insulative material over the first patterned mask and over the gate material;

patterning the first electrically insulative material into a mask defining a plurality of access device regions, the access device regions being islands surrounded by an isolation region; the access device regions comprising only portions of the recessed access device trenches;

etching into the substrate of said isolation region to recess the substrate of said isolation region, the etching also removing the gate material from between the access device regions while leaving the gate material within the access device regions;

covering the recessed substrate with a second electrically insulative material to cover the isolation region with the second electrically insulative material;

removing the first electrically insulative material; and

after removing the first electrically insulative material, forming a plurality of conductive lines, individual conductive lines extending across multiple access device regions and electrically interconnecting gate material of the multiple access device regions with one another.

12. The method of claim 11 wherein the first patterned mask comprises a siliconnitride-containing layer over a silicon-dioxide-containing layer.

13. The method of claim 11 wherein the filling the recessed access device trenches with gate material comprises:

forming the gate material to cover the first patterned mask and to be within the trenches; and

planarizing the gate material to remove the gate material from over the first patterned mask while leaving the gate material within the recessed access device trenches.

14. The method of claim 13 wherein the gate material comprises silicon and is conductively-doped prior to the planarizing.

15. The method of claim 13 wherein the gate material comprises silicon and is not conductively-doped prior to the planarizing.

16. The method of claim 13 wherein the first insulative material comprises oxide and silicon nitride; wherein the planarizing forms a planarized surface extending across the first patterned mask and the gate material, and wherein the forming the first electrically insulative material comprises:

oxidizing the planarized surface to form the oxide of the first insulative material extending across the first patterned mask and the gate material; and

forming the silicon nitride of the first insulative material over the oxide of the first insulative material.

17. The method of claim 16 wherein the planarized surface comprises silicon nitride along the first patterned mask and comprises conductively-doped silicon along the gate material; and wherein the oxide comprises silicon oxynitride over the first patterned mask and comprises silicon dioxide over the gate material.

18. The method of claim 11 wherein:

the substrate comprises monocrystalline silicon;

the etching into the first locations to form the recessed access device trenches etches into the monocrystalline silicon to a first depth; and

the etching into the substrate of said isolation region etches into the monocrystalline of the substrate to a second depth that is at least two-fold greater than the first depth.

19. The method of claim 11 wherein the forming the second electrically insulative material comprises:

forming the second electrically insulative material to cover the first electrically insulative material and recessed substrate; and

planarizing the second electrically insulative material to remove the second electrically insulative material from over the first electrically insulative while leaving the second electrically insulative material to cover the recessed substrate of the isolation region.

20. The method of claim 11 further comprising removing at least substantially all of the first electrically insulative material prior to forming the conductive lines.