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DATA RECORDING DEVICE

This invention relates in general to data recording devices and, more particularly, to the measurement of and compensation for non-linear bitshift in data recording devices.

It is well known that when recording closely spaced data bits (such as dibits) on a non-linear communication medium, such as a magnetic disk or an optical disk, the position of the bits may be shifted. This shift, which is called non-linear bitshift, degrades the performance of known data detection schemes such as the PRML (partial-response-maximum-likelihood) detection scheme, since these detection schemes are based on the assumption of a linear channel response.

It is possible to compensate the non-linear bitshift effect by shifting the data bit positions during data writing. However, to design a compensation scheme, the magnitude of the non-linear bitshift must be known. Unfortunately, measuring the non-linear bitshift has proven difficult; the prior art has accomplished such measurement only by means of sophisticated and expensive equipment.

Several methods requiring such equipment have been proposed for measuring non-linear bitshift. One is to compare the data bit response with isolated transitions to identify the non-linear bitshift. A second uses a specially designed pseudo-random sequence to determine an impulse response. The non-linear bitshift is then measured as an echo at a known position. A third uses a Volterra modelling technique for characterizing non-linear distortion in magnetic recording channels. All these methods require complicated data manipulation and high precision waveform recording. Thus, all are complex and costly when

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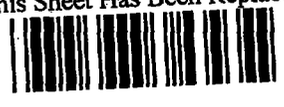
used to provide routine measurement of non-linear bitshift such as that required in a manufacturing or operational environment.

According to a first aspect of the present invention there is provided a data recording device comprising: data READ/WRITE means for writing data to and reading data from a data storage surface; amplitude detector means, responsive to a predetermined periodic data pattern recorded on the data storage surface, the predetermined data pattern comprising a plurality of pulses having spacings such that at least one harmonic of the data pattern has zero amplitude, to measure the magnitude of the data pattern at said harmonic when the data pattern is readback from the data storage surface; and processor means for processing the data to compensate for non-linear bitshift in accordance with the measured amplitude.

A data recording device is provided with a system which measures and compensates non-linear bitshift. The system is based on the use of special complex data patterns. These data patterns have in common the property that when their data bits, or pulses, are written without non-linear bitshift, certain harmonics of the fundamental frequency of the chosen data pattern are nulled, or eliminated (i.e., they have zero amplitude). However, if some data pulses are shifted due to non-linear bitshift, the "eliminated" harmonics reappear and exhibit nonzero amplitude. The amplitudes of these harmonics are indicative of the magnitude of the non-linear bitshift. Once the magnitude of the non-linear bitshift is known, an offsetting adjustment is applied to the data recording device to eliminate its effect.

The complex data patterns created according to the present invention have two principal features. First, the patterns are generated so that they incorporate within themselves the particular bit environment (such as a dibit) for which non-linear bitshift is to be determined and eliminated. This feature allows application of the invention to relatively simple data patterns frequently encountered in the course of data transmissions. Second, the patterns can be made

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insensitive to sources of non-linear effects other than non-linear bitshift. This feature enables extraneous non-linear effects to be factored out of the non-linear bitshift elimination scheme.

Two alternative embodiments are provided for using the harmonic nulling patterns to eliminate non-linear bitshift from data streams. The first embodiment uses an empirical approach, placing a problematic bit pattern in a harmonic nulling data pattern, iteratively minimizing the amplitude of the "eliminated" harmonic by shifting relative to one another the bits comprising the problematic bit pattern, and then storing the best fit bit spacing for later use in pre-shifting data patterns to compensate for the expected non-linear bitshift. The second embodiment uses an analytical approach which applies in the case of a dibit recorded on a magnetic storage device, placing a dibit pattern in a harmonic nulling data pattern, determining the amount and direction of bitshift associated with the "eliminated" harmonic corresponding to the bit spacing of the dibit, then varying the spacing of the dibit, forming a new harmonic nulling data pattern, and repeating the determining step to form a compensation plot for later use in pre-shifting data patterns to compensate for the expected non-linear bitshift.

Viewed from another aspect, the invention provides a method of measurement of non-linear bitshift in a data recording device having a data storage surface, the method comprising the steps of: reading back a data pattern from said data storage surface, said data pattern, when recorded, comprising a plurality of pulses having a nulled harmonic frequency of zero amplitude; measuring the magnitude of the readback data pattern at said nulled frequency.

There is also provided a method of compensating for non-linear bitshift in such a data recording device, the method comprising measuring the non-linear bitshift as set out above and converting said measured magnitude into a compensation factor for use in non-linear bitshift compensation of subsequently recorded data.

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Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, wherein:

Fig. 1 is a graphical representation illustrating a periodic pulse train and its harmonics;

Fig. 2 is a graphical representation illustrating a symmetric pulse train and its harmonics;

Fig. 3 is a graphical representation illustrating a dibit pulse train and its harmonics;

Fig. 4 is a graphical representation illustrating a readback signal of a harmonic eliminating data pattern according to the present invention;

Fig. 5 is a block diagram illustrating a non-linear bitshift compensator embodying the present invention;

Fig. 6 is a block diagram illustrating a PRML recorded data detection scheme with compensation embodying the present invention.

I. Development of Harmonic Nulling Data Patterns and Determination of Nonlinear Bitshift

In order to appreciate the specific aspects of the invention as applied to a data recording device, it is helpful to understand the signal processing fundamentals underlying generation of harmonic nulling data patterns and determination of non-linear bitshift. The following description explains these signal processing fundamentals and the relationships derived from them that form a part of the present invention.

Figs. 1(a) and 1(b) illustrate in the time domain and the frequency domain, respectively, frequency components at integer multiples of w_o,

where $w_o = 2\pi/T$ is the fundamental frequency, P(t) represents the pulse train, and P(w) represents its frequency components.

A more complicated periodic data pattern can be viewed as sums of delayed pulses from Fig. 1(a). Fig. 2(a) illustrates a series of equally spaced transitions, in which a symmetric pulse train has a spectrum as represented by the illustration in Fig. 2(b), wherein

$$(1) \qquad X(w) = P(w)(1-e^{-jwT/2})$$

When w is an even harmonic of w_o, $e^{-jwT/2}$ is unity, and X(w) vanishes regardless of the magnitude of P.

Fig. 3(a) shows an example of a periodic data pattern known as a dibit sequence. The spacing between the two bits in each dibit is T/4. The spectrum of the dibit sequence is illustrated in Fig. 3(b), wherein

$$(2) \qquad D(w) = P(w)(1-e^{-jwT/4})$$

In this case, the 4th, 8th, ... 4nth harmonics will vanish.

In general, the spectrum of a given periodic data pattern can be expressed as:

$$(3) \qquad Y(w) = P(w)(1+a_2e^{-jwT_2} + a_3e^{-jwT_3} + \ldots + a_Ne^{-jwT_N})$$

where $a_n = +1$ or -1, representing the polarity of the pulse, $T_2<T_3< \ldots <T_N$ and $T_2 \ldots T_N$ represent the time distances between the first pulse and the 2nd, the 3rd, ... the N-th pulse in the pattern. Various harmonics of the fundamental frequency may be eliminated by choosing $T_2 \ldots T_N$ so that Y(w) vanishes, as illustrated by the above examples. In this case the above general expression takes on the form:

$$(4) \qquad 1 + a_2e^{-jwT_2} + a_3e^{-jwT_3} + \ldots + a_Ne^{-jwT_N} = 0$$

or

$$(5) \qquad 1 + \sum_{n=2}^{N} a_n e^{-jwT_n} = 0$$

where n runs from 2 to some chosen limit N and w is the frequency at which the value of function Y in equation (8) is zero. It should be noted that many harmonic eliminating patterns are possible.

In the case where the recording medium is a magnetic storage device, the alternating polarity of the data pulses dictates alternating values for a_n, and equations (3), (4) and (5) become, respectively,

$$(6) \qquad Y(w) = P(w)(1 - e^{-jwT_2} + e^{-jwT_3} - \ldots -(-1)^N e^{-jwT_N})$$

$$(7) \qquad 1 - e^{-jwT_2} + e^{-jwT_3} - \ldots -(-1)^N e^{-jwT_N} = 0$$

and

$$(8) \qquad 1 + \sum_{n=2}^{N} (-1)^{n+1} e^{-jwT_n} = 0$$

The general process for creating a data pattern having a nulled harmonic is as follows. A bit pattern is chosen, the bit pattern having N≥2, a user specified frequency w, and containing the bit environment (such as a dibit) for which it is desired to determine non-linear bitshift. The bit time spacings of this pattern are designated to be $T_2 \ldots T_N$, which in general are subject to a number of constraints due to the chosen bit environment and possible limitations on the ability to place transitions in specific locations, as would be readily appreciated by one of skill in the art. Then equation (8) is solved for $T_2 \ldots T_N$ to yield the spacings necessary to achieve a spectral null. Due to the

constraints $T_2 \ldots T_N$, equation (8) may or may not be solvable. If not, an extra bit (T_{N+1}) is added to the original pattern, and equation (8) is again solved for $T_2 \ldots T_{N+1}$. The process is repeated until enough bits are added to render the constraints compatible with equation (8). Finally, once an acceptable pattern is created, it is checked against other non-linear effects, such as hard transition shifts, positive/negative WRITE current asymmetry, and magneto-resistive head positive/negative READ asymmetry. If the pattern is found to be susceptible to any of these extraneous non-linear effects, it may be further modified by adding additional bits and again solving equation (8) for the bit time spacings.

II. Use of Harmonic Nulling Data Patterns to Eliminate Nonlinear Bitshift

In accordance with the present invention, two alternative schemes are provided for exploiting the harmonic nulling patterns to eliminate the non-linear bitshift effect. First, using an empirical approach, a measurement mode is provided wherein a problematic bit pattern (such as closely spaced dibit) is placed in a harmonic nulling data pattern and the test pattern thus formed is recorded on the data recording device. The amplitude of the "eliminated" harmonic is measured. Then the bits comprising the problematic pattern are shifted relative to one another and the amplitude of the "eliminated" harmonic is re-measured. The process is repeated until the amplitude of the "eliminated" harmonic is reduced to a tolerable level (or zero). The original spacing of the problematic bit pattern and the input bit pattern spacing necessary to achieve it are saved. Another problematic bit pattern spacing may then be chosen and its corresponding input bit pattern spacing determined, and so on until a correction table of problematic bit pattern spacings and corresponding input bit pattern spacings is formed.

When the measurement mode is thus completed, a compensation mode is provided wherein problematic patterns in a complex data pattern are first identified. The spacings of these patterns are then referenced

into the correction table described above and the corresponding input bit pattern spacings are extracted. Finally, the series of shifted input bit patterns, now pre-compensated for the non-linear bitshift effect, is recorded on the data recording device.

The alternative to the empirical approach is an analytical approach. The analytical approach applies in the case of a dibit recorded on a magnetic storage device, where only one bit (the second bit) shifts and that one bit can be clearly identified. In the measurement mode provided for the analytical approach, a dibit sequence is placed in a harmonic nulling data pattern and the test pattern thus formed is recorded on the data recording device. The amplitude of the "eliminated" harmonic is measured. The amount and direction of bitshift associated with the measured amplitude is determined and plotted as a compensation factor.

In general, for small bitshift δ, the amount of bitshift may be approximately determined according to an equation having the form

$$|Z(kw_o)| = kw_o \delta |X(kw_o)| \tag{9}$$

where kw_o is the k^{th} harmonic of the fundamental frequency of the data pattern, $|Z(kw_o)|$ is the amplitude of the k^{th} harmonic, which is to be eliminated, δ is the magnitude of the non-linear bitshift, and $|X(kw_o)|$ is the amplitude of the k^{th} harmonic of equally spaced transitions with frequency w_o. $X(kw_o)$ may be determined by separately writing equally spaced transitions (a simple periodic pattern as shown in Fig. 2), reading them back, and measuring the amplitude of the k^{th} harmonic. The direction of bitshift is determined by purposely shifting the data pulses by a known amount during writing. The non-linear bitshift either increases or decreases the known shift depending on the direction of non-linear bitshift.

Once the amount and direction of bitshift for one dibit spacing is determined, the bits comprising the dibit sequence are shifted relative to one another and the harmonic nulling data pattern adjusted to

maintain an "eliminated" harmonic, the test pattern recorded, and the amplitude of the "eliminated" harmonic measured again. The amount and direction of bitshift associated with the measured amplitude is once again determined and plotted as another compensation factor. The process is repeated until a graph of dibit spacings versus bitshift (compensation factor) is developed.

When measurement mode is thus completed, a compensation mode is provided wherein a complex data pattern is pre-compensated for expected non-linear bitshift. According to the compensation mode, the data pattern is analyzed to identify the first transition for which non-linear bitshift is expected, that is the first transition which is closely preceded by another transition. The spacing between the transitions is referenced into the graph of bit spacings versus bitshift and the appropriate pre-compensated bit spacing is determined therefrom. Then analysis of the data pattern proceeds to identify the next transition for which non-linear bitshift is expected. The appropriate pre-compensation is determined for this transition, and the process repeats until pre-compensation is completed for the entire data pattern. Finally, the pre-compensated data pattern is recorded on the data recording device.

The compensation mode further provides an offset for the effects of cumulative shifts caused by multiple nearby transitions in a complex data pattern. The data pattern is analyzed and each transition is pre-compensated substantially as described above with the additional step of summing the individual effects from all preceding nearby transitions to determine the proper cumulative pre-compensation. Thus, for example, if the data pattern contains four closely spaced transitions, then the compensation mode determines and pre-compensates the expected bitshift of the second transition caused by the presence of the first transition, the third transition caused by the presence of the first and second transitions, and the fourth transition caused by the presence of the first, second and third transitions. All the separate

shifts are determined by referencing the relevant transition spacing into the graph of bit spacings versus bitshift.

In addition to measurement mode and compensation mode, the analytical approach provides a check mode which evaluates and improves upon the predictive power of the equations discussed above by iterating on the measurement and compensation modes. In check mode, a pre-compensated dibit pattern is chosen and placed in a harmonic nulling data pattern such that the resultant spacing of the bit pattern within the harmonic nulling data pattern should produce an eliminated harmonic. The test pattern thus formed is recorded on the data recording device. The residual non-linear bitshift is determined as a function of the amplitude of the "eliminated" harmonic, and the graph of dibit spacings versus bitshift is adjusted accordingly. The process may be repeated to iteratively perfect the non-linear bitshift compensation scheme.

III. Description of the Preferred Embodiment

According to the preferred embodiment of the present invention, a magnetic storage device is chosen as the recording medium and a dibit is chosen as the problematic bit pattern. The class of harmonic eliminating data patterns calculated according to equation (8) with N=3 assumes the following general form:

1100 ... (m0's)100 ... (n0's)1100 ... (m0's)100 ... (n0's)

where bits are separated by one clock period, a "1" indicates a transition, a "0" indicates no transition, and m and n are integer multiples of 6 (m and n include the two zeros shown in the above pattern). The pattern consists of a dibit and a single bit spaced relatively far from the dibit. The number of 0's between bits determines which harmonic is eliminated. One full period of the pattern, containing 6 1's, is shown. Since the first half and the second half of the pattern are identical, the pattern is obtained by the sum of three delayed isolated transition pairs.

Fig. 4 shows a qualitative representation of a typical harmonic-eliminating pattern created according to the preferred embodiment. The spectrum for this pattern is:

$$(10) \qquad Y(kw_o) = X(kw_o)\left(1 - e^{-j\frac{(n+1)k\pi}{m+n+3}} + e^{-j\frac{(n+2)k\pi}{m+n+3}}\right)$$

where kw_o is the harmonic under consideration and $X(kw_o)$ is the amplitude of the kth harmonic of equally spaced transitions with frequency w_o as shown in Fig. 2. When both m and n are multiples of 6, i.e. $m = 6p$ and $n = 6q$, the $(2p + 2q + 1)$th harmonic is exactly zero.

The bit pattern of the preferred embodiment includes three particularly advantageous features. First, the pattern incorporates a dibit as the bit environment for which non-linear bitshift is to be eliminated. The dibit is an ideal starting point for a compensation scheme because it forms an atomic pattern with which more complicated patterns can be analyzed. Second, when the pattern is written onto a magnetic storage surface in the presence of non-linear bitshift, only the second bit of the dibit will undergo shifting relative to the first bit. This is advantageous because it means only one shifting bit must be dealt with in the atomic pattern. Third, the pattern is insensitive to sources of non-linear effects other than non-linear bitshift resulting from closely spaced databits, such as hard transition shifts, positive/negative WRITE current asymmetry, and magneto-resistive head positive/negative read asymmetry. This property is important because it enables the bit pattern to automatically remove extraneous non-linear effects from the non-linear bitshift elimination scheme.

As discussed in Section II, the present invention provides two alternative schemes for exploiting harmonic nulling patterns to eliminate non-linear bitshift: an empirical approach and an analytical approach. In accordance with the preferred embodiment, the empirical approach includes a measurement mode wherein a dibit is placed in a

harmonic nulling data pattern as described above and successive measurements of the "eliminated" harmonic are made corresponding to various spacings of the second bit of the dibit relative to the first bit until the harmonic to be eliminated is minimized. The process is repeated with the harmonic nulling data pattern built around a different initial dibit spacing to form a correction table of dibit spacings and corresponding input bit pattern spacings. When the measurement mode is completed, the compensation mode operates substantially as described in Section II, wherein the problematic patterns identified are dibits.

The analytical approach of the preferred embodiment includes a measurement mode wherein a dibit is placed in a harmonic nulling data pattern as described above and the amplitude of the "eliminated" harmonic is measured and used to approximately determine the magnitude and direction of non-linear bitshift according to equation (9) in the form

$$|Z(kw_o)| = kw_o\delta|X(kw_o)|.$$

The process is repeated with the harmonic nulling data pattern built around different dibit spacings to form a graph of dibit spacings versus bitshift. When the measurement mode is completed the compensation and check modes operate substantially as described in Section II.

Fig. 5 illustrates in block diagram form a non-linear bitshift compensator for use in the data channel of a magnetic disk according to the preferred embodiment analytical approach for the present invention. As shown, compensator 110 includes pattern generator 111, switch 112, switch 113, bandpass filter 115, amplitude detector 117, processor 119, memory 121, and compensation controller 123.

Compensator 110 performs non-linear bitshift measurement and pre-compensation adjustment. It has three modes at operation: MEASUREMENT, COMPENSATION, and CHECK. In MEASUREMENT mode, switch 112 connects pattern generator 111 to WRITE driver 130. Pattern

generator 111 creates a data pattern having an eliminated, or nulled frequency kw_o, as described above. The data pattern is then written onto and read back from a storage disk (not shown) via the normal READ/WRITE channel, including WRITE driver 130 and READ preamplifier 150. The readback data pattern is fed through bandpass filter 115, which passes the nulled frequency component and removes other frequency components. The filtered signal is then fed through amplitude detector 117, which measures the magnitude of the nulled frequency component. The result is then converted into a compensation factor by processor 119 according to the method and formula of either the empirical approach or the analytical approach discussed above, and stored in memory 121 for later use by compensation controller 123. In order to implement the analytical approach a separate write-read-measure operation is required, consisting of writing an isolated transition, reading it back, and measuring the amplitude of its k^{th} harmonic, $X(kw_o)$, for use in determining the magnitude of non-linear bitshift from the magnitude of the nulled frequency component.

It is to be noted that the compensation factor stored in memory 121 may include the table of numbers described above in connection with the empirical approach, a formulaic representation of the graphical curve described above in connection with the analytical approach, a set of tables or graphs, each member of the set applicable to a particular portion of the disk, or any other information format describing a compensation approach developed according to the above-described method and formulas. Also, the contents of memory 121 may be stored permanently on a reserved part of the disk until the next calibration is performed. Further, the disk may be split into a plurality of bands, with a compensation factor calculated and stored separately for each band. Depending on the stability of disk drive components, calibration may be repeated; it can be performed after the drive is built, every time the power is turned on, every few hours, when correctable error exceeds a predetermined limit, etc. Finally, bandpass filter 115 may be implemented according to any of a variety of techniques well known in the art, including a simple inductive-capacitive network, or may be

functionally combined with amplitude detector 117 in a heterodyne structure that converts the nulled frequency component to another frequency and then determines its magnitude.

In COMPENSATION mode, switch 112 connects compensation controller 123 to WRITE driver 130. Compensation controller 123 receives encoded WRITE data 125 from external circuitry. Compensation controller 123 applies the compensation factor stored in memory 121 to adjust the relative spacing of the data pulses, and then passes the data pulses to WRITE driver 130 for recording on the storage disk. The compensation provided by the spacing adjustment effectively cancels the non-linear bitshift effect. Thus, when the recorded data is read back from the storage disk, the detection scheme can correctly anticipate the locations of the data pulses.

CHECK mode is a combination of MEASUREMENT mode and COMPENSATION mode. In CHECK mode, switch 113 connects pattern generator 111 to compensation controller 123. A data pattern from pattern generator 111 having a nulled frequency is fed into compensation controller 123 as write data. Memory 121 supplies compensation controller 123 with a previously generated compensation factor to act on the data pattern. Switch 112 connects compensation controller 123 to WRITE driver 130, and the adjusted data pattern is recorded on the storage disk. The data pattern is then read back from the storage disk using READ preamplifier 150, and the residual non-linear bitshift is measured by bandpass filter 115, amplitude detector 117, and processor 119. The result may be used as described above, that is to indicate the effectiveness of the compensation factor and to provide further iterative modification for the compensation factor.

Fig. 6 illustrates in block diagram form a PRML recorded data detection scheme embodying the present invention. As shown, the system includes encoder 100, non-linear bitshift compensator 110, READ preamplifier 150, and equalizer/decoder 160.

In operation, encoder 100 receives WRITE data 101 from external circuitry and translates WRITE data 101 into a magnetically recordable pulse train. Nonlinear bitshift compensator 110 receives the encoded WRITE data and adjusts the internal spacing of the pulse train to compensate the non-linear bitshift effect, as described above. The adjusted encoded WRITE data is then received by WRITE driver 130, which converts it into a corresponding WRITE current. The WRITE current passes through a magnetic head within recording head and storage disk 140, where it is thereby recorded on the storage disk. When the recorded data is to be read back form the storage disk, READ preamplifier 150 receives and amplifies the readback signal from the magnetic head. Equalizer/decoder 160 receives the amplified signal, decodes (i.e. detects) the pulse train, and provides at its output READ data 161 for connection to external circuitry. Since the non-linear bitshift effect was compensated before the data was written to the storage disk, the pulses comprising the readback signal are detected at their expected locations, and the number of readback errors generated by equalizer/decoder 160 is reduced.

There has been described a method of measuring non-linear bitshift in a data recording device, comprising the steps of: generating a data pattern having a plurality of pulses with spacing described by the equation

$$1 + \sum_{n=2}^{N} (-1)^{n+1} e^{-jwT_n}$$

wherein

w represents a frequency whose component is to be eliminated,

N represents the number of pulses in one period of said data pattern, and

T_n represents the time distance between the n-th pulse and the first pulse in said data pattern in the absence of non-linear bitshift;

writing said data pattern onto a data storage surface;

reading back said data pattern from said data storage surface; and determining the magnitude of non-linear bitshift in the readback data pattern according to the equation

$$|Z(kw_o)| = kw_o\delta|X(kw_o)|$$

wherein

kw_o represents the kth harmonic of the fundamental frequency of said data pattern,

$|Z(kw_o)|$ represents the amplitude of the kth harmonic,

$|X(kw_o)|$ represents the amplitude of the k^{th} harmonic of equally spaced transitions with frequency w_o, and

δ represents the magnitude of non-linear bitshift.

The method can further comprise the steps of: shifting the spacing of said pulses by a known amount prior to said writing step; and determining the direction of non-linear bitshift in the readback data pattern according to the difference between the magnitude of non-linear bitshift and said known amount of shift.

There has also been described a magnetic recording device having compensation for non-linear bitshift, comprising: a magnetic storage surface; and means for recording a data pattern on said magnetic storage surface, said data pattern comprising a plurality of pulses having spacing according to the form

1100 ... (m0's)100 ... (n0's)1100 ... (m0's)100 ... (n0's)

wherein m and n are integer multiples of 6.

means for determining the magnitude of non-linear bitshift in the recorded data pattern according to the equation

$$|Z(kw_o)| = kw_o\delta|X(kw_o)|$$

wherein kw_o represents the k^{th} harmonic of the fundamental frequency of said data pattern,

$|Z(kw_o)|$ represents the amplitude of the k^{th} harmonic,

$|X(kw_o)|$ represents the amplitude of the k^{th} harmonic of equally spaced transitions with frequency w_o, and

δ represents the magnitude of non-linear bitshift.

While the invention has been particularly described and illustrated with reference to a preferred embodiment, it will be understood by those skilled in the art that changes in the description or illustrations may be made with respect to form or detail without departing from the scope of the invention. For instance, the non-linear communication medium to which non-linear bitshift measurement and compensation is applied need not be a magnetic disk or an optical disk; it may be an optical fiber network or a magnetic tape system or any other system subject to non-linear effects.

CLAIMS

1. A data recording device comprising:

data READ/WRITE means for writing data to and reading data from a data storage surface;

amplitude detector means responsive to a predetermined periodic data pattern recorded on the data storage surface, the predetermined data pattern comprising a plurality of pulses having spacings such that at lease one harmonic of the data pattern has zero amplitude to measure the magnitude of the data pattern at said harmonic when the data pattern is readback from the data storage surface; and

processor means for processing the data to compensate for non-linear bitshift in accordance with the measured amplitude.

2. A data recording device as claimed in Claim 1 comprising means for shifting the spacing of said pulses by a known amount and means for determining the direction of non-linear bitshift in the readback data pattern according to the difference between the magnitude of non-linear bitshift and said known amount of shift.

3. A data recording device as claimed in Claim 1 or Claim 2 further comprising:

memory means for storing said compensation factor; and

compensation controller means, responsive to said compensation factor, for receiving WRITE data, shifting the spacing of data pulses in said WRITE data in accordance with said compensation factor and transferring said compensated WRITE data to said data READ/WRITE means for recording onto said data storage surface.



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4. A method of measurement of non-linear bitshift in a data recording device having a data storage surface, the method comprising the steps of:

(1) reading back a data pattern from said data storage surface said data pattern, when recorded, comprising a plurality of pulses having a nulled harmonic frequency of zero amplitude;

(2) measuring the magnitude of the readback data pattern at said nulled frequency.

5. A method of compensating non-linear bitshift in a data recording device having a data storage surface, the method comprising measuring the non-linear bitshift using a method as claimed in Claim 4 and converting said measured magnitude into a compensation factor for use in processing data to be subsequently written to the disc surface to compensate for non-linear bitshift.

6. A method of compensating for non-linear bitshift as claimed in Claim 5, wherein said converting step includes:

(a) shifting the spacing of at least one of the pulses in said data pattern relative to the other pulses to form a shifted data pattern;

(b) writing said shifted data pattern onto said data storage surface;

(c) reading back said shifted data pattern from said data storage surface;

(d) measuring the magnitude of the readback data pattern at said nulled frequency;

(e) repeating steps (a) through (d) at least once; and retaining said data pattern and the one of said shifted data patterns having the smallest readback magnitude at said nulled frequency as said compensation factor.

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7. A method of compensating for non-linear bitshift as claimed in Claim 6, further comprising the steps of:

storing said compensation factor in a memory means;
receiving WRITE data from a WRITE data source; and
shifting the spacing of data pulses in said WRITE data in accordance with said compensation factor.

8. A method of compensating for non-linear bitshift as claimed in Claim 6, wherein:

steps (1) to (3) are performed repetitively, each repetition operating on a different data pattern;

said retaining step forms a compensation table comprising the compensation factors generated by the repetition of steps (1) to (3); and

further comprising the steps of:

storing said compensation table in a memory means;
receiving WRITE data from a WRITE data source; and
shifting the spacing of data pulses in said WRITE data in accordance with said compensation table.

9. A method of compensating for non-linear bitshift as claimed in Claim 8, wherein said shifting step further comprises the steps of:

subdividing said WRITE data into bit patterns having the form of a problematic pattern within said data pattern;

shifting the spacing of said bit patterns in accordance with said compensation table.

10. A method of compensating for non-linear bitshift as claimed in Claim 9,

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wherein said shifting step further comprises the steps of:

in said WRITE data identifying at least one shifting data pulse, where said at least one shifting data pulse is a data pulse which is closely preceded by at least one other data pulse;

for each said least one shifting data pulse, summing the individual effects from all preceding data pulses on said at least one shifting data pulse; and

shifting the spacing of said at least one shifting data pulse in accordance with said sum of individual effects and said compensation factors.



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