

Output Architecture for LCD Panel Column Driver

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ABSTRACT

In one embodiment consistent with the present invention, a digital to analog converter (DAC) circuit operates over an upper range and a lower range. An upper voltage node is designated AVDD; a middle voltage node is designated HVDD; and a lower voltage node designated ground. An upper DAC stage has at least one NMOS
10 transistors that produces an output to an upper range output node when the output is in the upper range. A lower DAC stage has at least one PMOS transistors that produces an output to a lower range output node when the output is in the lower range. A body bias control circuit couples the body of the upper NMOS transistor to a voltage source equal to HVDD-Vbe and connects the body of the lower PMOS transistor to voltage source
15 equal to HVDD+Vbe. This abstract is not to be considered limiting, since other embodiments may deviate from the features described in this abstract.

FIG. 1