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TITLE OF THE INVENTION

Moving Picture Processing Method

BACKGROUND OF THE INVENTION

This invention relates to a moving picture processing device for processing a moving picture containing a redundant picture. More particularly, it relates to a moving picture processing device for processing moving picture signals obtained on photo-electric conversion of a source of original pictures, such as a motion picture film.

For interconnecting plural devices handling moving pictures for providing a moving picture processing system, it is necessary to synchronize the moving pictures. In general, one of the devices of the system is used as a reference and the remaining devices are caused to follow up with the reference device. This reference device is termed a master and the remaining devices are termed slave deices. The master device is exemplified by a video camera, a VTR, a video disc or a computer, as a supply source for moving pictures, while the slave device is exemplified by an encoder, a VTR or a monitor designed to process the supplied moving pictures.

The synchronization signal supplied from the master device is supplied as a reference clock for a phase locked loop (PLL) of the system.

An illustrative moving picture encoding system is shown in Fig.1.

This moving picture encoding system has many clock sorts, such as clocks for an encoder 101, clocks for a local decoder 102, or display clocks. Of these, a picture synchronization input S2, supplied from a digital VTR 100 of a picture input device 10, as a supply source for the moving pictures, represent master clocks.

The encoding of the moving pictures is a technique recognized to be indispensable for reducing transmission costs at the time of digital transmission of moving pictures.

For example, a picture processor 20 is made up of the encoder 101 and the local decider 102, and implements a hybrid encoding method consisting in the combination of motion compensation prediction and DCT well-known in so-called MPEG 2 (ISO/IEC 13813-2).

An input picture S1 is given at a rate of 30 frames/second (60 fields/second) or 25 frames/second (50 fields/second).

In Fig.2, the fields shown by intersected hatching denote top fields or odd fields, while the fields shown by hatching denote bottom fields or even fields. In the present example, each frame is necessarily constituted by a pair of fields. Thus a frame synchronization signal S2 is supplied in synchronism with each frame. In this case, all input pictures are encoded by the picture processor 20 of Fig.1, with the encoder 101 being in operation by being locked by the frame synchronization signal S2.

If the input picture S1 is free of redundant fields, the

moving picture encoding system operates without fail by employing the frame synchronization signal S2.

However, there are occasions wherein redundant pictures are contained in the input picture S1.

Such redundant picture is contained in the moving picture obtained on recording e.g. a motion picture film in a VTR by photo-electric conversion. That is, the number of picture frames of the motion picture film as an original picture source is 24 per second, whereas that of the NTSC television system is 30 frames (60 fields) per second. For compensating the six frames (12 fields) per second which fall in shortage, the same fields are repeated at a rate of one field per two picture frames for converting the two picture frames into five fields for thereby converting the 24 picture frames into 60 fields, that is 30 frames. This method is termed 3:2 pull-down, as will be explained subsequently in detail. The repeated fields are the same as the previous fields and represent redundant pictures.

With the moving picture encoding system, the data volume is diminished by detecting and not encoding the redundant pictures. Thus, although not shown in the example of Fig.1, the encoder 101 detects the redundant pictures in the pre-processing process and simply omits encoding the redundant pictures.

This processing manner is shown specifically in Fig.3.

In the present embodiment, the redundant pictures are shown by plain textured fields and are not encoded.

If the plain-textured field is the odd field, it is the same as the directly previous odd field, whereas, if the plain-textured field is the even field, it is the same as the directly previous even field. Thus, one field is eliminated every five fields and a new input frame is produced by two consecutive fields next to the eliminated field.

The timing of the frame entering the next-stage picture processor is asynchronous with respect to the frame synchronization signal S2, as may be seen by a timing pulse S3, such that there is no possibility of locking with respect to the frame synchronization signal S2. The result is that, with the moving picture processing system of Fig.1 employing the frame synchronization signal S2 in the picture processing system, the frame synchronization signal S2 cannot be used in e.g., the picture processor 20.

On the other hand, in case of processing not only the usual moving pictures shown in Fig.2 but also the moving pictures including redundant pictures shown in Fig.3. the processing by the picture processor 20 is increased in complexity depending on whether or not the pre-processing is to be performed.

In addition, with a series of moving pictures containing redundant pictures in an irregular manner, the frame timing may be changed irregularly in a more complex fashion. There lacks up to now a picture processing device capable of coping with all of these variable timings, while it is difficult to produce such

picture processing device.

OBJECTS AND SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method and apparatus for processing moving pictures capable of processing moving pictures containing redundant pictures at a pre-set period or in an irregular fashion.

It is another object of the present invention to provide a technique in a picture processing system employing a picture synchronization input from the picture input device as master clocks, according to which, even in such case wherein a string of pictures entering the next-stage picture processor is not locked with respect to the synchronization input of the original input moving picture due to pre-processing of eliminating redundant pictures from the original input picture supplied from the picture inputting device, processed pictures can be outputted by picture processing employing the synchronization input of the original input picture as master clocks of the picture processing system.

Thus, it is yet another object of the present invention to provide a technique whereby a synchronization signal for an input frame or field may also be employed in an encoder.

In one aspect, the present invention provides a method for processing a moving picture in which input digital moving picture signals of a pre-set picture rate are processed in accordance with pre-set picture processing and for transmitting the

processed digital picture signals. The input digital moving picture signal has plural field pictures. The method includes a first step of detecting a redundant field from the input digital moving picture signals, a second step of eliminating the detected redundant field from the plural field pictures, a third step of deciding, from a string of field pictures from which the redundant fields have been eliminated, the combination of a top field and a bottom field constituting a frame to be processed in accordance with the pre-set picture processing, and outputting the results of decision, a fourth step of inserting a pre-set signal in the field picture string from which the redundant field has been eliminated for generating picture signals for processing having the same picture rate as the rate of the input digital picture signal, and a fifth step of processing the picture signals for processing in accordance with the pre-set picture processing based upon the results of decision. In this manner, the moving pictures containing the redundant pictures at a constant period or at irregular intervals may be converted to new picture string signals synchronized with the input picture synchronization signals.

Preferably, the method also includes a sixth step of appending to the picture signals for processing the subsidiary information employed for processing the picture signals for processing by the pre-set picture processing.

Preferably, the input digital moving picture signal is a

signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate. By appending the subsidiary information employed for processing the picture signals for processing to the picture signals for processing, correct picture processing may be carried out by the picture encoder based upon the subsidiary information.

If the input digital moving picture signal is a signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate, the subsidiary information includes a first flag specifying which of the top field and the bottom field has been read out first when processing the original image, a second flag specifying whether each picture of the original image has been read out with three fields or with two fields, and a third flag specifying which picture signals of the picture signals for processing are the inserted pre-set signals. In this manner, picture processing may be carried out correctly.

In the sixth step, pre-set picture processing is preferably encoding for compression and the encoding for compression is not executed for picture signals for processing to which the third flag is appended.

In the first step, the redundant field is detected by calculating the inter-field correlation of the input digital moving picture signal.

Preferably, the pre-set signals inserted in the picture signal for processing are invalid signals nonsensical as picture signals. Since these invalid signals need not be encoded for compression by the encoder, picture processing may be carried out efficiently.

If the input digital moving picture signal is a signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate, a redundant field is detected by calculating the inter-field correlation between picture signals of the current field of the input digital moving picture signals and picture signals delayed therefrom by two fields, the number of the input fields of the input digital moving picture signals is counted, it is then judged whether the count value is a pre-set value, and the redundant field is detected from the results of decision and the inter-field correlation, so that the redundant field may be detected reliably.

If the input digital moving picture signal is a signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate, the subsidiary information includes a first flag specifying which of the top field and the bottom field has been read out first when processing the original image, a second flag specifying whether each picture of the original image has been read out with three fields or with two fields, and a third

flag specifying which picture signals of the picture signals for processing are the inserted pre-set signals.

In another aspect, the present invention provides a method for processing moving picture signals in which digital moving picture signals of a pre-set picture rate containing redundant fields are restored from picture signals for processing generated by removing the redundant fields from the digital moving picture signals made up of a plurality of field pictures, inserting pre-set invalid signals corresponding to said redundant fields into the digital moving picture signals from which the redundant fields have been removed and by appending the subsidiary information for controlling the picture processing. The method includes a first step of removing the subsidiary information from the picture signals for processing, a second step of removing the invalid signals from the picture signals for processing using the subsidiary information, and a third step of repeating picture signals of a portion of a picture signal string from which the invalid signals have been removed for generating the redundant fields for restoring the digital picture signals of the pre-set picture rate. In this manner, digital moving picture signals for display may be produced easily.

Thus, in a moving picture processing system employing a picture synchronization input supplied from a picture inputting device as master clocks, if a picture string for processing B to be inputted to a picture processing device A of the next stage

cannot be locked to the picture synchronizing input supplied from the picture inputting device due to pre-processing of removing redundant pictures from the original input moving pictures supplied from the picture inputting device, the picture string B for processing can be re-formed into a new picture string for processing C that can be locked to the picture synchronization input. In this manner, the picture synchronizing input supplied from the picture inputting device can be used at all times as master clocks for the pictured processing device. On the other hand, since the picture processing device, which represents a core portion of the picture processing system, need not be specifically modified from that used in the usual case, that is the case in which the usual input picture string is locked to the picture synchronization input, the picture processing device is not complicated in structure excessively.

With the moving picture signal processing method according to the present invention, the redundant fields are detected and eliminated from the input digital picture signals to form a picture string, the combination of the top field and the bottom field making up the frame for processing by encoding for compression is discriminated from the picture string to form a frame picture string and pre-set signals are inserted into the frame picture string for producing picture signals for processing. In this manner, new picture string signals synchronized with the picture synchronization signals may be

formed from moving pictures containing redundant pictures at a constant period or at irregular intervals.

The subsidiary information for picture processing may be appended to the picture string for processing for enabling correct processing to be performed by the picture encoder based upon the subsidiary information.

If the input digital moving picture signals are the signals read out by the 3:2 pull-down method in which a picture of an original image, such as a picture frame of a motion picture film, is read in two or three fields, the subsidiary information contains a first flag specifying whether it is the top field or the bottom field that has been read out first when reading out the original image, that is a top_field_first flag, a second flag specifying whether a picture of the original image has been read out in three fields or in two fields, that is a repeat_first flag, and a third flag specifying which picture signals are the invalid signals as the preset signals.

In such case, since the encoding for compression can be omitted for these invalid signals, more efficient picture encoding can be achieved.

If the input digital moving picture signals are signals read out by the 3:2 pull-down method according to which a picture of the original image, for example, a picture frame of a motion picture film, is read out in two or three fields, the redundant field detection means preferably includes a field counter which

is adapted for calculating the inter-field correlation between the current field of the input digital moving picture signals and the field delayed therefrom by two pictures, and which is reset to zero on detection of redundant fields, and comparator means for judging whether the count value from the field counter is an odd number of not less than 5. Redundant fields may be reliably detected by detecting the redundant field based upon the output of the comparator means and the inter-field correlation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a block diagram showing an illustrative conventional moving picture processing system.

Fig.2 illustrates frame synchronization.

Fig.3 illustrates the operation of eliminating redundant fields from the 3:2 pull-down signals.

Fig.4 is a block diagram showing a moving picture processing system according to an embodiment of the moving picture processing method according to the present invention.

Fig.5 illustrates the 3:2 pull-down system of reading out one picture frame of a motion picture source with 2 or 3 fields.

Fig.6 is a block circuit diagram showing an illustrative construction of a pre-processor.

Fig.7 is a flowchart for showing an illustrative operation of the pre-processor.

Fig.8 is a timing chart for showing an illustrative operation of the pre-processor.

Fig.9 is a block circuit diagram showing an illustrative construction of a post-processor.

Fig.10 is a flowchart for showing an illustrative operation of the post-processor.

Figs.11A, 11B are timing charts for showing an illustrative operation of the post-processor.

Fig.12 shows an illustrative method for encoding moving pictures.

Fig.13 is a block circuit diagram showing an illustrative encoder for encoding moving pictures.

Fig.14 illustrates an operation of picture encoding type designation, picture encoding sequence and picture re-arraying operation.

Fig.15 illustrates the construction of picture data.

Figs.16A, 16B illustrate a frame/field prediction mode.

Figs.17A, 17B illustrate the frame/field DCT mode.

Fig.18 illustrates a picture display sequence re-arraying operation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig.4, a moving picture processing device for carrying out the moving picture processing method of the present invention will be explained in detail.

Fig.4 shows an example of a moving picture processing system, inclusive of a moving picture processing device, in which an original input moving picture signal is a video signal of a

film source the frame rate of which has been set to 30 Hz by so-called 3:2 pull-down.

The 3-2 pull-down is briefly explained. When the film source, such as a motion picture, is converted into interlaced video signals, the technique known as the 3:2 pull-down is widely employed. That is, if the number of picture frames of a motion picture film is 24 per second, and the interlaced video signal has a picture rate of 30 frames per second or 60 fields per second, the number of fields is converted by the 3:2 pull-down.

That is, such a technique is employed in which, of two consecutive picture frames of a film, that is MF1 and MF2, the first picture frame MF1 is read out with two video fields, while the second picture frame MF2 is read out with three fields.

On the other hand, the inverse 3:2 pull-down is such an operation in which a picture frame read out with three fields is detected from 30 frame/second interlaced video signals, and any redundant repetitive field is removed for producing progressive frames having an ideal frame rate of 24 frames per second. Ideally, the redundant fields appear at a period of five fields.

In a moving picture processing system, shown in Fig.4, an interlaced signal having a rate of 30 frames per second or 60 fields per second, as an input moving picture signal S100, is supplied, with a top field top_field first, from a digital VTR 201, as a picture inputting device.

If the input moving picture signal S100 is a moving picture

converted from the film source by the 3:2 pull-down, a flag S115 is set, while switches 209, 210, 211 and 212 are set to the on-side. If the input moving picture S100 is not the moving picture converted by the 3:2 pull-down, these switches are set to the off-side. With the switches set to the off-side, the system configuration is basically the same as the conventional system. In the following description, it is predicated that the above switches have been set to the on-sides, that is that the input moving pictures contain redundant pictures.

If the switch 209 is connected to the on-side, the input moving picture signal S100 is processed by a pre-processor 202 and thereby converted into a moving picture signal S103.

The processing by the pre-processor 202 is explained further by referring to Fig.6.

The two-field signal correlation between the moving picture signal S100 of the 60 Hz video field, entering a terminal 301, and a field signal S200 outputted with a 2-field delay from a delay unit 302, is calculated. For this calculation, a difference value is calculated by a unit 303 from pixel to pixel. An absolute value unit 304 finds absolute values of the difference values S201, calculated from pixel to pixel, and a sum S203 of the absolute values per field is calculated in an adder 305. The sum S203 is compared by a comparator 306 to a pre-set threshold S204. If the sum is smaller than the threshold value S204, a flag S205 is set. It is noted that any other means for

calculating the correlation between the two fields S100 and S200 may be employed in addition to the above method.

On the other hand, the synchronization input S105 of the field picture signal S100 enters a field counter 309 from a terminal 308. That is, the counter 309 counts up the number of the fields entering the pre-processor 202. If the number of the count value i represented by S206 is an odd number not less than 5, a comparator 310 sets a flag S211. When both the flag S211 and the flag S205 have been set, an output S212 of an AND gate 311 rises, thus indicating that the current input field signal S100 is a redundant field which has been repeated by the 3:2 pull-down. If the flag S212 is set, the counter 309 is cleared to zero. The field found to be a redundant field is removed from the input picture without being encoded.

The reason the criterion of judgement in the comparator 310 as to the count value i being an odd number not less than 5 is that, by the following grounds, the inverse 3:2 pull-down is not guaranteed to operate normally at al times.

First, the pattern of the redundant field appearing at a 5-field period is not guaranteed due to video editing following 3:2 pull-down.

Second, since a smoothing filter is applied during 3:2 pull-down along the time axis, that is between different fields and between different frames, redundant fields become difficult to detect depending upon picture patterns. For example, there are

occasions wherein the flag S205 is not set at the comparator 306 even although the current input field is a redundant field.

Even if the 3:2 pull-down pattern is not guaranteed, it becomes possible for the comparator 310 to continue to give decision as to the redundant field.

Since in effect the 3:2 pull-down is not necessarily carried out regularly, the frame rate for moving pictures after removing the resultant fields from the input moving picture S100 is fluctuated in a range between 24 Hz and 30 Hz. This period is not locked with respect to the synchronization input S105. Thus, in the present embodiment, the input fields are re-arrayed in their sequence, and invalid frames are inserted, by way of pre-processing, for creating a new input picture string that can be locked by the synchronization input. It is this new input picture string that is caused to enter the next stage unit, that is an encoder 203.

The method of re-arraying the fields and inserting the invalid frames in explained by referring to Fig.6. An output field controller 312 causes a switch 316 to switch between three signals, namely the field signal S200, outputted with a delay of two fields (one frame) from the delay unit 302, a field signal delayed by four fields S208 and an invalid field signal S209, based upon the redundant field detection flag S212.

Based upon the position information having detected the redundant field, the display pattern of the input picture is

classified into four shown in Fig.5 by two flags, that is a top field_first flag and a repeat_first_field flag. The top_field first flag specifies whether or not the top field top_field has been read out first on executing 3:2 pull-down on a given picture frame of a motion picture film. The repeat_first_field flag specifies whether or not a given picture frame of the motion picture film has been read out in three fields. The top_field first flag and the repeat_first_field flag are generated in an output field controller 312 and the information of at least two past display patterns are stored internally.

The algorithm of finding the top_field_first flag and the repeat_first_field flag by the output controller 312 is shown in Fig.7. In Fig.7, fp denotes the serial number of the input fields S100 since the time they are supplied. Any addition to fp specifies that the time of the input field S100 progresses towards future. For example, fp=fp+2 denotes that the S100 time has progressed two fields towards future, that is the input of S100 has advanced by two fields.

The respective steps of the flowchart of Fig.7 are explained. After the start of the operation at step 1000, a first field is entered at step 1001. It is then checked at step 1002 whether the parity of the field is for the top field top field or the bottom field bottom_field. The processing is then branched to step 1004 or 1010.

If the result of judgment at step 1002 is YES, that is if

the first field is the top field top_field, control transfers to a field advanced by two fields towards future, in order to check at step 1005 whether or not the field is a redundant field. This is a decision as to whether or not the redundant field detection flag S212 of Fig.6 is set. If the field is the redundant field, the display patterns of three previous fields, inclusive of the current field, are top_field_first = 1 and repeat_first_field = 1 for the respective flags.

The position of the redundant field is set to detected_fp = fp (step 1006). The time for S100 is advanced by one field (step 1007). As the next processing operation, control transfers to the step for the field parity being for the bottom field bottom_field (step 1010). If the field is judged at step 1005 not to be a redundant field, the display patterns of two previous fields not including the current field are top_field_first = 1 and repeat_first_field = 0 for the respective flags (step 1008). The next processing operation transfers to a step 1004 for the field parity being for the top field top_field.

If the result of the previous branching at step 1002 is NO, that is if the first field is the bottom field bottom_field, control transfers to a field advanced by two fields towards future, in order to check at step 1011 whether or not the field is a redundant field. This is a decision as to whether or not the redundant field detection flag S212 of Fig.6 is set.

If the first field is the redundant field, the display

patterns of three previous fields, inclusive of the current field, are top_field_first = 0 and repeat_first_field = 1 for the respective flags. The position of the redundant field is detected_fp = fp (step 1012). The time for S100 is advanced by one field (step 1013). As the next processing operation, control transfers to the step for the field parity being for the top field top_field (step 1004). If the field is judged at step 1005 not to be a redundant field, the display patterns of two previous fields not including the current field are top_field_first = 0 and repeat_first_field = 0 for the respective flags (step 1014). The next processing operation transfers to a step 1010 for the field parity being for the bottom field bottom_field.

By the above process, the output field controller 312 sets the respective flags top_field_first and repeat_first_field.

An illustrative operation of the output field controller 312 is explained by referring to Fig.8.

In this figure, capital letters, such as "A" or "B", denote the top fields, whereas small letters, such as "a" or "b" denote the bottom fields. The interval shown by "|" denotes an input frame period. It is assumed that the redundant fields are detected at positions indicated by "*".

In the illustrative example of Fig.8, the first field "A" of the input S100 is entered (fp = 1) and is found to be top field (steps 1000 to 1003). The field "B" two fields towards future (fp = 3) is not found to be redundant (steps 1003 to

1008). The field "B" further two fields towards future (fp = 5) is found to be redundant (steps 1003 to 1006) and the time is advanced by one field (fp = 6) at step 1007. The field "B" two fields further towards future (fp = 8) is not found to be redundant (steps 1009 to 1014). The field "B" two fields further towards future (fp = 10) is found to be redundant (steps 1009 to 1013). The above processing sets the display pattern as follows:

fp= 1~2: top_field_first = 1, repeat_first_field = 0

fp= 3~5: top_field_first = 1, repeat_first_field = 1

fp= 6~7: top_field_first = 0, repeat_first_field = 0

fp= 8~10: top_field_first = 0, repeat_first_field = 1

An output S210 is hereinafter explained.

The output S210 starts with a delay of 4 fields (2 frames) with respect to the input signal S100. The output S210 is controlled as shown in items (i) to (iv) below by the output field controller 312 sending a changeover control signal S207 to a changeover switch 316 based upon the top_field_first and repeat first_field flags set on the output field controller 312:

(i) With top_field_first = 1 and repeat_first_field = 0;

the field signal S208, delayed by 4 fields, is sequentially outputted by two fields. These fields are of the first frame |A a| of the field signal S208.

(ii) With top_field_first = 1 and repeat_first_field = 1;

the field signal S208, delayed by 4 fields, is sequentially

outputted by two fields. These fields are of the second frame |B b| of the field signal S208 in the example of Fig.8. The top field top_field of the third input frame is a redundant field and hence is removed without being outputted.

(iii) With top_field_first = 0 and repeat_first_field = 0;

the field signal S200, delayed by 2 fields, is outputted, and subsequently the field signal S208, delayed by 4 fields, is outputted. In the example of Fig.8, the field signal S200 is outputted at a position of the top field top_field "B" of the third frame of the field S208 which is redundant and hence removed. That is, the top field top_field "C" of the fourth frame of the field signal S208 is previously stuffed and outputted. The bottom field bottom_field of the third input frame of the field signal S208 is then outputted. As for the input S100, the bottom field bottom_field "c" is temporally ahead of the top field top_field "C", these two fields not making up a frame. However, at an output S103, the top field top_field is temporally at a previous position so that an output frame |C c| is produced.

(iv) With top_field_first = 0 and repeat_first_field = 1;

two invalid fields or one invalid frame is outputted, followed by two fields of the field signal S208 delayed by 4 fields. In the example of Fig.8, if a redundant field is detected at a bottom field bottom_field, such as bottom_field "d" of the fifth frame of the signal S100, two invalid fields are

outputted at the output S103. This is shown in Fig.8 by |x|. Next, |D d|is outputted at the signal S208.

As shown by the above items (i) to (iv), the output controller 312 changes over the switch 316 in order to control the output S210. In the column "quantity of field delay" in Fig.8, there is shown the delay quantity of the respective fields of the output S210 with respect to the signal S100. The values 4, 2 and x denote outputs of the field signal S208 and S200 and invalid fields.

Two consecutive fields of the output S210 represent an output frame. To each output frame, there is appended the frame header information by a frame header multiplexer 313, and the resulting signal S103 is outputted at a terminal 314. The contents of the header include a top_field_first flag, a repeat first_field flag and an invalid frame flag, shown as disabled frame_flag. Illustrative examples of the header information appended to the respective flags are shown in the column "top field_first flag and repeat_first_field flag" in fig.8.

In output frames of S210 and S103, the top field top_field is outputted first, with its frame period being locked with the frame period of the synchronization input signal S105.

In the foregoing explanation, the invalid frames are inserted so as to be synchronized with the frame synchronization signal. However, the invalid fields may also be inserted so as to be synchronized with the field synchronization signal, in

which case the two invalid frames may be inserted at any arbitrary position if the field rate of 60 Hz is observed, there being no necessity of the two fields being inserted consecutively.

Meanwhile, if the switches 209, 210 in Fig.4 are turned off, the signal S100 is an interlacing signal in which usual top_field not processed with 3:2 pull-down is entered first.

In such case, the frame header represents the default contents, in which top_field_first = 1, repeat_first_field = 0 and disabled_frame_flag = 0 at all times.

Without regard to the on/off states of the switches 209, 210 of Fig.4, the signals S100 and S103 may be used as an input S104 to an encoder 203, operating with the synchronization input S105 as a master clock.

The input S104 is processed in many ways by the encoder 203 and the local decoder 205 which represent core portion of the motion picture encoding system. It is noted that the frames designated as invalid frames in the respective frame headers of the input S104 are not processed as valid frames. An illustrative processing operation in such case will be explained subsequently.

The method for outputting the output S109 from the local decoder 205 to the picture outputting device 207 is explained. Referring to Fig.9, a post-processor 206, fed with the output S109, is explained.

Referring to Fig.9, the locally decoded output S109, entering a terminal 400, is sent to a frame header separator 401 where the header contents S303 of the respective frames are read out and sent to an output field controller 403. In the output field controller 403, the information of at least one past display pattern of the header contents is stored. The header contents include the flags top_field_first, repeat_first_field and disabled_frame_flag.

Meanwhile, if the switches 211, 212 shown in Fig.4 are off, S111 is an interlacing signal in which the usual top_field not processed with 3:2 pull-down is first entered.

In such case, the frame header becomes the default contents, such that top_field_first = 1, repeat_first_field = 0 and disabled_frame_flag = 0 at all times.

Based upon the frame header contents, the output field controller 403 of Fig.4 causes a switch 404 to switch between three signals, namely a current input field S300, a field signal S301 with a delay of 2 fields or 1 frame and a field signal S302 with a delay of 4 fields or 2 frames, outputted by a delay unit 402.

An illustrative operation of the post-processor, in particular the output field controller 403 of Fig.9, is explained by referring to Fig.10.

In this figure, capital letters, such as "A" or "B", denote the top fields, whereas small letters, such as "a" or "b" denote

the bottom fields. The interval shown by "|" denotes an input frame period.

The picture output S110 starts with a delay of 2 fields or 1 frame with resect to the input signal S300. The outputting is controlled as shown in items (i) to (v) below in accordance with top_field_first, repeat_first_field and disabled_frame_flag set in the output field controller 403.

(i) top_field_first = 1, repeat_first_field = 0 and disabled frame_flag = 0;

the field signal S301, delayed by 1 frame, is sequentially outputted by two fields. In the present example, shown in Fig.10, these fields are of the first frame |A a| of the field signal S301.

(ii) top_field_first = 1, repeat_first_field = 1 and disabled frame_flag = 0;

the field signal S301, delayed by 1 frame, is sequentially outputted by two fields. Then, the field signal S302, delayed by 2 frames, is outputted by one field. In the example of Fig.10, the second frame |B b| of the field signal S301 is outputted, followed by top field top_field "B" of the second frame of the field signal S302.

(iii) top_field_first = 0, repeat_first_field = 0 and disabled frame_flag = 0;

the field signal S301, delayed by 1 frame, is outputted by one field. Then, the field signal S302, delayed by 2 frames, is

outputted. In the example of Fig.10, the bottom field bottom field "c" of the third frame of the field signal S301 is outputted, followed by top field top_field "C" of the third frame of the field signal S302.

(iv) disabled_frame_flag = 1;

no signal is outputted.

(v) top_field_first = 0, repeat_first_field = 1 and disabled frame_flag = 0;

the current input field S300 is outputted by one field, followed by two fields of the field signal S301 delayed by one frame.

As shown by the above items (i) to (v), the output controller 403 changes over the switch 404 in order to control the output S110. In the column "quantity of field delay" in Fig.10, there is shown the delay quantity of the respective fields of the output S110 with respect to the output S100. The values 4, 2 and 0 denote outputs of S302, S301 and S300, respectively.

Returning to Fig.4, an output S112, obtained via the local decoder 205, switch 211, post-processor 206 if necessary, and the switch 206, may be displayed on a monitor 207 as a picture outputting device.

The above is the manner of operation of the input/output of the moving pictures of the moving picture processing system shown in Fig.4.

In the foregoing description, the invalid signal inserted into picture signals entering the encoder is an invalid frame, and an invalid frame flag is appended to the frame header information. However, the invalid signal units may also be fields, micro-blocks or pixels, in which case a flag specifying that such unit is an invalid signal is appended to each unit as the subsidiary information.

Also, in the foregoing description, the synchronization input period of the input picture is one frame time period. However, the synchronization input period may also be one field time period or one pixel time period.

In the above description of the picture inputting device 201 and the encoder 203, the top field represents the firstly entered interlaced signal. Conversely, with the picture inputting device 201 and the encoder 203, the bottom field may also represent the firstly entered interlaced signal, in which case it suffices to interchange the sequence of the top field top_field which is an odd-field and the bottom field bottom_field which is an even-field.

For example, the signals S210 and S300 are interlaced signals in which it is the bottom_field_first flag that is first entered.

Next, the processing at the encoder 203 and the local decoder 205, constituting a moving picture encoder as a core portion of the moving picture encoding system of Fig.4, is

hereinafter explained.

The moving picture encoder implements a hybrid encoding method consisting in a combination of motion compensated prediction coding and DCT well-known with the so-called MPEG 2 (ISO/IEC 13818-2). With the MPEG 2, pictures of respective frames are I-pictures, P-pictures or B-pictures, and picture signals are encoded by compression encoding.

That is, picture signals of 17 frames, that is frames F1 to F17, are grouped together as a group-of-picture, which is a processing unit. For example, picture signals of the leading frame F1, second frame F2 and the third frame F3 are encoded as I-picture, as B-picture and as P-picture, respectively, as shown in Fig.11A. The fourth and following frame F4 to F17 are alternately processed as B-pictures or P-pictures.

As for the picture signals for the I-picture, the one-frame picture signals are directly transmitted. As for the picture signals of the P-picture, basically the difference from the picture signals of the temporally past I-picture or P-picture is transmitted, as shown in Fig.11A. As for the picture signals of the B-picture, basically the difference from the mean value of the picture signals of the temporally past frame and the picture signals of the temporally future frame is found and encoded.

Fig.12 shows the principle of the method for encoding the moving picture signals. As shown therein, since the first frame F1 is processed as the I-picture, it is directly transmitted as

transmitted data F1X on the transmission route (intra-picture coding). Conversely, since the second frame F2 is processed as the B-picture, the difference between the mean value of the past frame F1 and the mean value of the future frame F3 is calculated, and the resulting difference is transmitted as transmission data F2X.

More specifically, there exist four sorts of processing as the B-picture. The first processing is to transmit data of the original frame F2 directly as transmitted data F2X (SP1) by way of performing intra-coding. This processing is similar to that for the I-picture. The second processing is to calculate the difference from the future frame F3 and to transmit the difference SP2, by way of performing backward predictive coding. The third processing is to transmit the difference from the past frame F1 (SP3) by way of performing forward predictive coding. Finally, the fourth processing is to generate a difference from a mean value of the past frame F1 and the future frame (SP4) and to transmit the difference as transmission data F2X by way of performing bi-directional predictive coding.

Of these four methods, such a method which minimizes the quantity of transmission data is selected.

For transmitting the difference data, a motion vector x1 between the frames F1 and F2, that is between the picture of the current frame and the prediction picture (the picture of the frame the difference of which from the current picture is to be

calculated) is transmitted along with the difference data for forward predictive coding. Similarly, a motion vector x2 between the frames F3 and F2 is transmitted along with the difference data for backward predictive coding, while both the motion vector x1 and the motion vector x2 are transmitted along with the difference data for bi-directional predictive coding.

As for the frame F3 of the P-picture, the difference signal SP3 between the frame F3 and the temporally past frame F1 as the prediction picture, and the motion vector x3, are calculated, and transmitted as transmission data F3X, by way of performing forward predictive coding. Alternatively, data of the original frame D3 are directly transmitted as transmission data F3X (SP1) by way of performing intra-coding. One of these methods is selected which will minimize the quantity of transmitted data, as in the case of the B-picture.

Referring to Fig.13, an illustrative construction of the moving picture encoding device (encoder) is explained. Although not shown precisely, the present encoder is operated by being locked to the picture synchronization input S105, shown in Fig.4

From a terminal 74, an input frame S104 having a frame header is entered, whereas, from a terminal 75, a flag S115, indicating whether or not the input moving picture fed from the picture input device is derived from a film source by 3:2 pull-down.

The input picture S104 is entered to a picture encoding type

designating and picture encoding sequence re-arraying unit 70, which then designates one of the I-, P- and B-pictures in terms of which the pictures of the sequentially entered frames are to be processed. For example, the group-of-picture constituted by the frames F1 to F17 are processed as I, B, P, B, P, ...B, P, as shown in Fig.11. The designated picture encoding types are written in the respective frame headers.

The input pictures are then re-arrayed in the encoding sequence in accordance with the designated picture encoding types. The reason of re-arraying the input pictures is that, since the B-picture is encoded by backward prediction, coding becomes infeasible unless the I-picture or the P-picture as the backward prediction picture is readied in advance. Thus the temporally future I-picture or P-picture has to be encoded before encoding the B-picture. Therefore, the picture sequence is re-arrayed to F1, F3, F2, F5, F4, ... if the picture encoding types are designated as shown for example in Fig.11.

The manner of handling the input frame (input picture or input picture string) S104 in the picture encoding type designating and picture encoding sequence re-arraying unit 70 in case the input picture S104 contains an invalid frame, designated by the frame header disabled_frame_flag, is explained.

It is assumed that the input picture S104 made up of F1 to F13 is entered, as shown in Fig.14, in which "X" denotes an invalid frame. The picture encoding types are sequentially

designated as in a picture string S501 as the invalid frames are disregarded. The numbers in the picture string S501 denote the sequence of designation of the picture encoding types. The pictures are then re-arrayed in the encoding sequence in accordance with the picture encoding types. Thus the picture string S502 is re-arrayed as shown in a picture string S502. In the present case, the signal string S502 is started with a delay of two frames relative to the picture sting S104.

The re-arrayed picture string S502 enters the scan converter 71 where the pictures entered by raster scan are converted into block-format signals. That is, the picture entered by raster scanning is comprised of V lines each consisting of H dots as shown in Fig.15. The scan converter 71 splits the 1-frame signals into M slices, each slice consisting of 16 lines as a unit. Each slice is split into macro-blocks. Each macro-block is made up of luminance signals corresponding to 16x16 pixels (dots), which are further split into blocks Y[1] to Y[4] each consisting of 8x8 dots. These 16x16 dot luminance signals are associated with 8x8 dot Cb signals and 8x8 dot Cr signals.

On the other hand, for executing motion prediction for the frame S502 being encoded, a reference picture S504 is supplied to the motion vector detection circuit 50. The motion vector detection circuit 50 processes the picture data of the respective frames as the I-pictures, P-pictures or as B-pictures, in accordance with the instructions from the picture encoding

type designating and picture encoding sequence re-arraying unit 70. The picture data of a frame processed as an I-picture, such as frame F1, is transferred from the motion vector detection circuit 50 to a forward original picture unit 51a of the frame memory 51 for storage therein. The picture data of the frame processed as the B-picture is transferred to and stored in an original picture unit 51b, while the picture data of the frame processed as the P-picture is transferred to and stored in a backward original picture unit 51c.

If, at the next timing, the picture of a frame to be processed as the B-picture (frame F4) or as the P-picture (frame F5) is supplied, the picture data of the first P-picture (frame F3) so far stored in the backward original picture unit 51c is transferred to the forward original picture unit 51a. The next B-picture (frame F4) is stored (overwritten) in the original picture unit 51b, while the P-picture next to the B-picture is stored (overwritten) in the backward original picture unit 51c. The above operations occur sequentially.

Meanwhile, if the frame S502 is an invalid frame, the motion vector detection circuit 50 waits during a one-frame period without performing any processing.

The macro-block read out from the scan converter 71 is processed with frame prediction mode processing or field prediction mode processing by a prediction mode switching circuit 52. The macro-blocks thus processed are processed by a

calculating unit 53 with intra-coding, forward predictive coding, backward predictive coding or bi-directional predictive coding, under control by a prediction decision circuit 54. Which of these processing operations is to be executed is determined in dependence upon a prediction error signal, that is a difference between a picture to be processed, or a reference picture, and a prediction picture therefor. Thus the motion vector detection circuit 50 generates a sum of absolute values of prediction error signals used for this decision.

The frame prediction mode and the field prediction mode in the prediction mode switching circuit 52 is hereinafter explained.

If the frame prediction mode has been set, the prediction mode switching circuit 52 directly outputs the four luminance blocks Y[1] to Y[4] supplied from the scan converter 71 to the downstream side calculating unit 53. In this case, top-field line data and bottom-field line data exist together in each luminance block, as shown in Fig.16A. With this frame prediction mode, prediction is executed on four luminance blocks (macro-block) as a unit and each one motion vector is associated with these four luminance blocks.

Conversely, the prediction mode switching circuit 52 operated so that the luminance blocks Y[1] and Y[2], among the four luminance blocks, supplied thereto from the scan inverter 71 in a configuration shown in Fig.16A, will be constituted

solely by dots of the top field line, while the remaining two luminance blocks Y[3] and Y[4] will be constituted solely by data of the bottom field line, these being then outputted to the calculating unit 53, as shown in Fig.16B. In such case, a sole motion vector is associated with the two luminance blocks Y[1] and Y[2], while another sole motion vector is associated with the remaining two luminance blocks Y[3] and Y[4].

For the frame prediction mode, the chroma signals are supplied to the calculating unit 53 in a state in which top field line data and bottom field line data exist together, as shown in Fig.16A. For the field prediction mode, upper four lines of chroma blocks Cb and Cr become top field chroma signals associated with the luminance blocks Y[1], Y[2], while lower four lines of the chroma blocks Cb and Cr become bottom field chroma signals associated with the luminance blocks Y[3], Y[4], as shown in Fig.16B.

The motion vector detection circuit 50 outputs the sum of absolute values of prediction errors for the frame prediction mode and the sum of absolute values of prediction errors for the field prediction mode to the prediction mode switching circuit 52. The prediction mode switching circuit 52 compares the sums of the absolute values of the prediction errors for the frame prediction mode and for the field prediction mode and executes the processing for the prediction mode having the smaller value. The resulting data is supplied to the calculating unit 53.

If a 3:2 pull-down source input flag S115 has been set, the input frame S104 is of the progressive structure, so that the prediction mode is fixed at the frame prediction mode.

The motion vector detection circuit 50 generates in the prediction decision circuit 54 the sum of absolute values of the prediction errors for determining which of the intra-coding, forward predictive coding, backward predictive coding or the bidirectional coding is to be executed.

That is, the motion vector detection circuit 50 finds, as the sum of the absolute values of the prediction errors of intra-picture coding, the sum of absolute values of differences between signals Aij of the macro-block of the reference picture and a mean value Aav of the macro-block signals Aij, or $\Sigma|Aij-Aav|$. The motion vector detection circuit 50 also finds, as the sum of the absolute values of the prediction errors of forward predictive coding, the sum of absolute values of differences between signals Aij of the input macro-block and the signal Bij of the macro-block of the prediction picture, or $\Sigma|Aij-Bij|$. The sum of the absolute values of the prediction errors of the backward prediction and bidirectional prediction is found in a similar manner except that the prediction picture used is different from that for forward prediction.

These sums of the absolute values are supplied to the prediction decision circuit 54 which then selects the smallest one of the sums of the absolute values of the prediction errors

of the forward prediction, backward prediction and bidirectional prediction as the sum of the absolute values of the prediction errors for the inter-picture prediction. The prediction decision circuit 54 then compares the sum of the absolute values of the prediction errors for the inter-picture prediction to the sum of the absolute values of the prediction errors of the intra-picture coding and selects the smaller one of the sums of the absolute values in order to select the mode corresponding to the selected sum value as the prediction mode. That is, if the sum of the absolute values of the prediction errors of the intra-picture coding is smaller, the intra-picture prediction mode is set. If the sum of the absolute values of the prediction errors for the inter-picture prediction is smaller, the mode having the smallest sum of the absolute values, among the forward prediction mode, backward prediction mode and the bidirectional prediction mode, is set.

Thus the motion vector detection circuit 50 detects the motion vector between the reference picture and the prediction picture associated with one of the four prediction modes selected by the prediction decision circuit 54, and outputs the detected motion vector to a variable length encoding circuit 58 and to a motion compensation circuit 64. Such a motion vector having the smallest value of the sum of the absolute values of the prediction errors is selected.

When a picture of a frame to be processed as an I-picture

is entered, the intra-frame prediction mode, that is a mode not executing motion prediction, is set, and a switch 53d of the calculating unit 53 is set to a fixed contact a. This permits the picture data of the I-picture to enter a DCT mode switching circuit 55.

The DCT mode switching circuit 55 sets data of the four luminance blocks to a state in which top field lines and bottom field lines exist together (frame DCT mode) or a state in which top field lines and bottom field lines are separated from each other (field DCT mode), and outputs the data to a DCT circuit 56, as shown in Figs.17A or 17B.

That is, the DCT mode switching circuit 55 compares the encoding efficiency for the case in which the top field data and the bottom field data are DCTed in an intermingled state and that for the case in which the top field data and the bottom field data are DCTed in a separated state, and selects a mode exhibiting a better encoding efficiency.

For example, the input signal configuration is such a configuration in which the top field lines and the bottom field lines are in a commingled state, as shown in Fig.17A. The difference between signals of the vertically neighboring top field and bottom field lines is calculated and the sum of absolute values of the differences or the sum of square values of the differences are found. Also, the input signal configuration is such a configuration in which the top field

lines and the bottom field lines are in a separated state, as shown in Fig.17B. The difference between signals of the vertically neighboring top field and bottom field lines is calculated and the sum of absolute values of the differences or the sum of square values of the differences are found. The two sums of the absolute values are compared to each other and the DCT mode for the smaller value of the sums is set. That is, if the former sum is smaller, the frame DCT mode is set, whereas, if the latter sum is smaller, the field DCT mode is set.

Then, data of the configuration associated with the selected DCT mode are outputted to the DCT circuit 56, and a DCT flag specifying the selected DCT mode is outputted to a variable length coding circuit 58 and to a motion compensation circuit 64.

If the 3:2 pull-down source input flag S115 is set, the input frame S104 is of a progressive structure, so that the DCT mode is fixed at the frame DCT mode.

It is seen on comparison of the prediction mode in the prediction mode switching circuit 52 shown in Figs.16A and 16B and the DCT mode in the DCT mode switching circuit 55 shown in Figs.17A and 17B that the data constructions in these two modes are substantially identified with each other.

The picture data of the I-picture outputted by the DCT mode switching circuit 55 is supplied to the DCT circuit 56 where it is DCTed and converted into DCT coefficients. These DCT coefficients are fed to a quantization circuit 57 and quantized

with a quantization step associated with the quantity of data stored in a transmission buffer 59 so as to be fed to the variable length coding circuit 58.

From the frame header information, the variable length coding circuit 58 transmits the picture encoding type, top_field first and repeat_first_field.

The variable length coding circuit 58 is responsive to the quantization step or scale supplied from the quantization circuit 57 to convert picture data supplied from the quantization circuit 57, herein data of the I-picture, into variable length codes, such as Huffman codes, and to output the converted data to the transmission buffer 59.

The variable length encoding circuit 58 also variable length encodes input data thereto, that is the quantization step or scale supplied from the quantization circuit 57, the prediction modes supplied from the prediction decision circuit 54, that is the modes specifying which one of the intra-picture coding, forward predictive coding, backward predictive coding and bidirectional predictive coding has been set, the prediction flag supplied from the prediction mode switching circuit 52, that is a flag specifying which one of the frame prediction mode and the field prediction mode has been set, and the DCT flag outputted by the DCT mode switching circuit 55, that is the flag specifying which one of the frame DCT mode and the field DCT mode has been set.

However, if the 3:2 pull-down source input flag S115 has been set, both the prediction flag and the DCT flag are of fixed values of the frame mode, so that these flags are not outputted by the variable length coding circuit 58. Instead, the variable length coding circuit transmits the information that the flag S115 has been set, that is that the input frame is of the progressive structure.

The transmission buffer 59 transiently stores the input data and outputs data corresponding to the stored quantity to the quantization circuit 57.

If the residual data quantity in the transmission buffer 59 is increased to an allowable upper limit, the transmission buffer increases the quantization scale of the quantization circuit 57 by the quantization control signal for decreasing the data quantity of the quantized data. Conversely, if the residual data quantity in the transmission buffer 59 is decreased to an allowable lower limit, the transmission buffer decreases the quantization scale of the quantization circuit 57 by the quantization control signal for increasing the data quantity of the quantized data. This prohibits overflow or underflow from being produced in the transmission buffer 59.

The data stored in the transmission buffer 59 is read out at a pre-set timing so as to be outputted to a transmission path.

On the other hand, data of the I-picture outputted by the quantization circuit 57 are supplied to a dequantization circuit

60 so as to be dequantized in accordance with the quantization step supplied from the quantization circuit 57. An output of the dequantization circuit 60 is fed to an inverse DCT (IDCT) circuit 61 and thereby inverse DCTed so as to be then supplied to and stored in a forward predicted picture portion 63a of a frame memory 63.

When a picture of a frame to be processed as a P-picture is supplied from the scan converter 71, the sums of absolute values of the macro-block-based inter-frame differences (prediction errors) are supplied from the motion vector detection circuit 50 to the prediction mode switching circuit 52 and to the prediction decision circuit 54, in the same manner as described above. The frame/field prediction mode, intra-picture prediction mode or the forward prediction mode is set in association with the sums of the macro-block-based prediction errors.

When the intra-frame prediction mode is set, the calculating unit 53 sets the movable contact of the switch 53d to its fixed contact a, as described above. Thus, similar to the I-picture data, the corresponding data is supplied via the DCT mode switching circuit 55, DCT circuit 56, quantization circuit 57, variable length coding circuit 58 and the transmission buffer 59 to the transmission path. The same data is also supplied via the dequantization circuit 60, IDCT circuit 61 and the calculating unit 62 to a backward predicted picture portion 63b of the frame memory 63 for storage therein.

At the same time as the switch 53d is set to the side of the fixed contact b for the forward prediction mode, data of a picture stored in the forward predicted picture portion 63a of the frame memory 63, herein the picture of the I-picture, are read out and motion-compensated by the motion compensation circuit 64 in association with the motion vector outputted by the motion vector detection circuit 50.

Output predicted picture data from the motion prediction circuit 64 is fed to a calculating unit 53a, which subtracts, from the data of the macro-block of the reference picture supplied from the prediction mode switching circuit 52, the predicted picture data for the macro-block, supplied from the motion compensation circuit 64, and outputs the difference, that is predicted errors. The difference data is transmitted on the transmission path via the DCT mode switching circuit 55, DCT circuit 56, quantization circuit 57, variable length coding circuit 58 and the transmission buffer 59. The difference data is also locally decoded by the dequantization circuit 60 and the IDCT circuit 61 so as to be supplied to the calculating unit 62.

However, if the 3:2 pull-down source input flag S115 has been set, both the prediction flag and the DCT flag are of fixed values of the frame mode, so that these flags are not outputted by the variable length coding circuit 58. Instead, the variable length coding circuit transmits the information that the flag S115 has been set, that is that the input frame is of the

progressive structure.

The calculating unit 62 is also fed with the same data as the predicted picture data supplied to the calculating unit 53a. The calculating unit 62 adds the predicted output picture data of the motion compensation circuit 64 to the output difference data from the IDCT circuit 61. The picture data of the P-picture are fed to and stored in the backward predicted picture portion 63b of the frame memory 63.

When fed from the scan converter 71 with the picture of a frame to be processed as a B-picture, the motion vector detection circuit 50 transmits the sums of the absolute values of the macro-block-based inter-frame differences (prediction errors) to the prediction mode switching circuit 52 and to the prediction decision circuit 54. The prediction mode switching circuit 52 and to the prediction decision circuit 54 then set the frame/field mode in dependence upon the magnitudes of the sums of the absolute values of the macro-block-based inter-frame differences, while setting the prediction mode to one of the intra-picture coding, forward predictive coding, backward predictive coding and bidirectional predictive coding.

The switch 53d is set to the side of the fixed contacts a or b for the intra-frame prediction mode or the forward prediction mode, respectively, as described above. At this time, the processing similar to that for the P-picture is performed for data transmission.

Conversely, when the prediction mode is the backward prediction mode or the bidirectional prediction mode or, the switch 53d is set to the sides of the fixed contacts c or d, respectively.

For the backward prediction mode when the switch 53d is set to the contact c, the data of the picture stored in the backward predicted picture portion 63b, herein the picture of the P-picture, is read out so as to be motion-compensated in association with the motion vector outputted by the motion vector detection circuit 50.

The predicted picture data outputted by the motion compensation circuit 64 is supplied to the calculating unit 53b. The calculating unit 53b subtracts the predicted picture data supplied from the motion compensation circuit 64 from the input macro-block data supplied from the prediction mode switching circuit 52 and output the resulting difference data. The resulting difference data is transmitted on the transmission path via the DCT mode switching circuit 55, DCT circuit 56, quantization circuit 57, variable length encoding circuit 58 and the transmission buffer 59. The difference data is also locally decoded by the dequantization circuit 60 and the IDCT circuit 61 so as to be supplied to the calculating unit 62.

The calculating unit 62 is also fed with the same data as the predicted picture supplied to the calculating unit 53b. The calculating unit 62 adds the predicted output picture data of the

motion compensation circuit 64 to the output difference data of the IDCT circuit 61. This gives picture data of the locally decoded B-picture.

For the bi-directional prediction mode, when the switch 53d is set to the side of the contact d, data of the picture stored in the forward predicted picture portion 63a, herein the picture of the I-picture, and data of the picture stored in the backward predicted picture portion 63b, herein the picture of the P-picture, are read out and motion-compensated by the motion compensation circuit 64 in association with the motion vector outputted by the motion vector detection circuit 50.

The predicted picture data, outputted by the motion compensation circuit 64, is fed to a calculating unit 53c. The calculating unit 53c subtracts, from data of an input macro-block supplied from the prediction mode switching circuit 52, a mean value of the predicted picture data supplied form the motion compensation circuit 64, and outputs difference data. This difference data is transmitted on the transmission path via the DCT mode switching circuit 55, DCT circuit 56, quantization circuit 57, variable length encoding circuit 58 and the transmission buffer 59. The difference data is also locally decoded by the dequantization circuit 60 and the IDCT circuit 61 so as to be supplied to the calculating unit 62.

The calculating unit 62 is also fed with the same data as the predicted picture supplied to the calculating unit 53c. The

calculating unit 62 adds the predicted output picture data of the motion compensation circuit 64 to the output difference data of the IDCT circuit 61. This gives picture data of the locally decoded B-picture.

If the 3:2 pull-down source input flag S115 has been set, both the prediction flag and the DCT flag are of fixed values of the frame mode, so that these flags are not outputted by the variable length coding circuit 58. Instead, the variable length coding circuit transmits the information that the flag S115 has been set, that is that the input frame is of the progressive structure.

Since the B-picture is not used as the prediction picture for other pictures, it is not stored in the frame memory 63.

In the frame memory, bank switching is occasionally performed between the forward prediction picture and the backward prediction picture so that the forward prediction picture or the backward prediction picture will be selected and outputted for a given reference picture.

The foregoing description has been made on luminance blocks. However, the chroma blocks are also similarly processed and transmitted on the macro-block bases as shown in Figs.16A, 16B, 17A and 17B. The motion vector employed for processing the chroma block corresponds to the motion vector of the associated luminance block halved in both the vertical and horizontal directions.

If invalid frames are fed from the scan converter 71, the DCT circuit 56, dequantization circuit 60, inverse DCT circuit 61 or the motion compensation circuit 64 performs no processing such that nonsensical data is outputted by the calculating unit 62. No data is written at this time in the frame memory 63. During this time, no bitstream is outputted by the variable length encoding circuit 58.

If the encoded data of the I-, P- and B-picture or the invalid frame is routed as described above, the picture data locally decoded by the calculating unit 62 is entered to the scan converter 72 which converts the macro-block-based input data into raster scanning data S505. The raster scanning data S505 enters a picture display sequence re-arraying unit 73. Fig.18 shows illustrative examples of the output of the picture display sequence re-arraying unit 73. The picture display sequence re-arraying unit 73 re-arrays the display sequence of the input picture in accordance with the following rules (i) to (iii) based upon the picture encoding types.

(i) The I-picture, initially entered, is stored in the picture display sequence re-arraying unit 73.

(ii) If the picture entered next is the B-picture or the invalid frame, the picture is directly outputted. If the picture entered next is the I- or P-picture, the I- or P-picture stored in the picture display sequence re-arraying unit 73 is outputted. The currently entered I- or P-picture is newly stored in the picture

display sequence re-arraying unit 73.

(iii) The processing reverts to (ii).

The locally decoded picture S109 is outputted from the picture display sequence re-arraying unit 73 as shown in (i) to (iii) above.

The locally decoded picture S109 is outputted via a post-processor 206 to a monitor 207 as a picture outputting unit as explained with reference to Fig.4.

WHAT IS CLAIMED IS:

1. A method for processing a moving picture in which input digital moving picture signals of a pre-set picture rate in accordance with pre-set picture processing and transmitting the processed digital picture signal, said input digital moving picture signal having plural field pictures, comprising:

a first step of detecting a redundant field from said input digital moving picture signals;

a second step of eliminating the detected redundant field from said plural field pictures;

a third step of deciding, from a string of field pictures from which the redundant fields have been eliminated, the combination of a top field and a bottom field constituting a frame to be processed in accordance with said pre-set picture processing, and outputting the results of decision;

a fourth step of inserting a pre-set signal in the field picture string from which said redundant field has been eliminated for generating picture signals for processing having the same picture rate as the rate of the input digital picture signal; and

a fifth step of processing said picture signals for processing in accordance with said pre-set picture processing based upon the results of decision.

2. The moving picture processing method as claimed in claim 1 further comprising a sixth step of appending to said picture

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signals for processing the subsidiary information employed for processing said picture signals for processing by said pre-set picture processing.

3. The moving picture processing method as claimed in claim 1 wherein said input digital moving picture signal is a signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate.

4. The moving picture processing method as claimed in claim 2 wherein, if said input digital moving picture signal is a signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate, said subsidiary information comprises:

a first flag specifying which of the top field and the bottom field has been read out first when processing the original image;

a second flag specifying whether each picture of the original image has been read out with three fields or with two fields; and

a third flag specifying which picture signals of said picture signals for processing are said inserted pre-set signals.

5. The moving picture processing method as claimed in claim 4 wherein said pre-set picture processing is encoding for compression and wherein said encoding for compression is not executed for picture signal for processing to which the third

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flag is appended.

6. The moving picture processing method as claimed in claim 1 wherein, in said first step, said redundant field is detected by calculating the inter-field correlation of said input digital moving picture signal.

7. The moving picture processing method as claimed in claim 4 wherein said input digital moving picture signal is a signal generated by 3:2 pull-down according to which each picture of an original image is read out in two or three fields for changing the picture rate, and wherein, in said first step, said redundant field is detected by calculating the inter-field correlation between picture signals of the current field of the input digital moving picture signals and picture signals delayed therefrom by two fields.

8. The moving picture processing method as claimed in claim 7 wherein, in said first step, the number of the input fields of said input digital moving picture signals is counted, it is then judged whether the count value is a pre-set value and wherein said redundant field is detected from the results of decision and said inter-field correlation.

9. The moving picture processing method as claimed in claim 4 wherein said pre-set signals inserted in said picture signal for processing are invalid signals nonsensical as picture signals.

10. A method for processing moving picture signals in which digital moving picture signals of a pre-set picture rate

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containing redundant fields are restored from picture signals for processing generated by removing the redundant fields from the digital moving picture signals made up of a plurality of field pictures, inserting pre-set invalid signals corresponding to said redundant fields into the digital moving picture signals from which said redundant fields have been removed and by appending the subsidiary information for controlling the picture processing, comprising:

a first step of removing said subsidiary information from said picture signals for processing;

a second step of removing said invalid signals from said picture signals for processing using said subsidiary information; and

a third step of repeating picture signals of a portion of a picture signal string from which said invalid signals have been removed for generating said redundant fields for restoring said digital picture signals of said pre-set picture rate.

11. The moving picture processing method as claimed in claim 10 wherein, in said third step, 3:2 pull-down is carried out in which a picture of the picture signal string from which the invalid signals have been removed is read out in two or three fields for modifying the picture rate.

12. The moving picture processing method as claimed in claim 11 wherein said subsidiary information comprises a first flag specifying which of the top field an the bottom field making up

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a picture is to be read out first, a second flag specifying with which of the three field rate and the two-field rate the picture of the picture signals for processing is to be read out and a third flag specifying which of the picture signals of the picture signals for processing are the inserted invalid signals.

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MOVING PICTURE PROCESSING METHOD

ABSTRACT

A method for processing a moving picture includes five steps. Firstly, a redundant field from the plural field pictures of the input digital moving picture signals is detected. Secondly, the detected redundant field is eliminated from the plural field pictures. Thirdly, from a string of field pictures from which the redundant fields have been eliminated, the combination of a top field and a bottom field constituting a frame is decided to be processed in accordance with the pre-set picture processing, and outputting the results of decision. Fourthly, a pre-set signal is inserted in the field picture string from which the redundant field has been eliminated for generating picture signals for processing having the same picture rate as the rate of the input digital picture signal. Lastly, the picture signals for processing are processed in accordance with the pre-set picture processing based upon the results of decision.

Figure 4

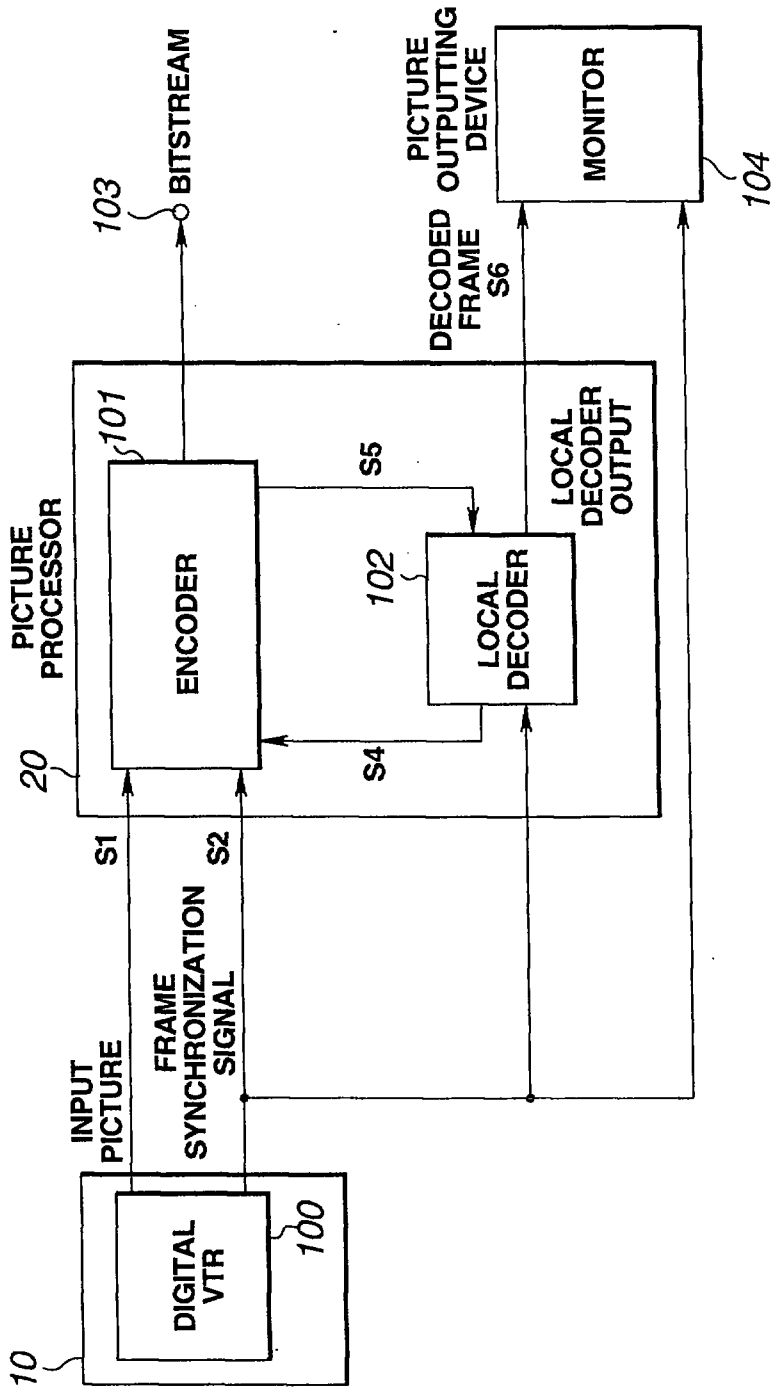

10
DIGITAL VTR
100
INPUT PICTURE
FRAME SYNCHRONIZATION SIGNAL
S1
S2
20
PICTURE PROCESSOR
ENCODER
101
LOCAL DECODER
102
S4
S5
LOCAL DECODER OUTPUT
DECODED FRAME S6
PICTURE OUTPUTTING DEVICE
MONITOR
104
103
BITSTREAM

FIG.1

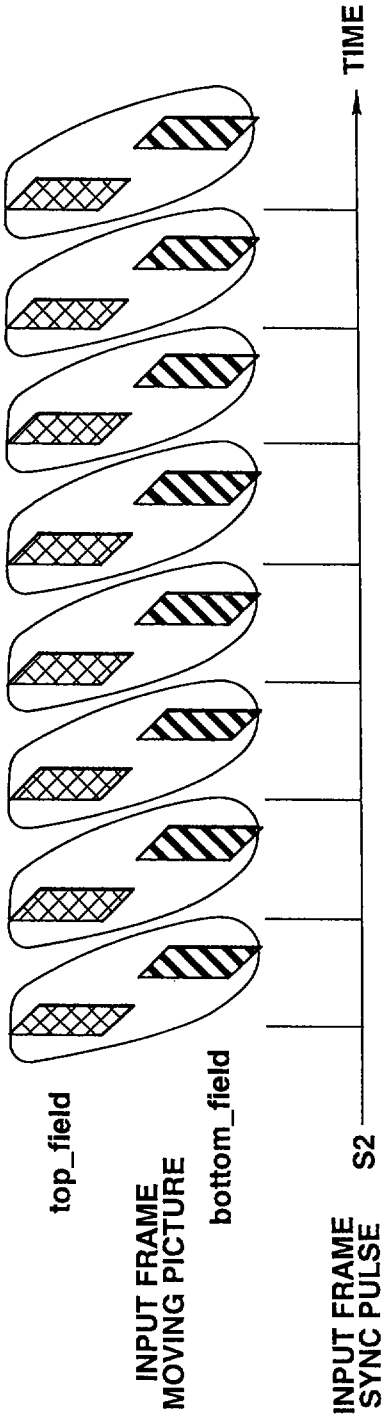

TIME
INPUT FRAME
SYNC PULSE
S2
INPUT FRAME
MOVING PICTURE
top_field
bottom_field

FIG.2

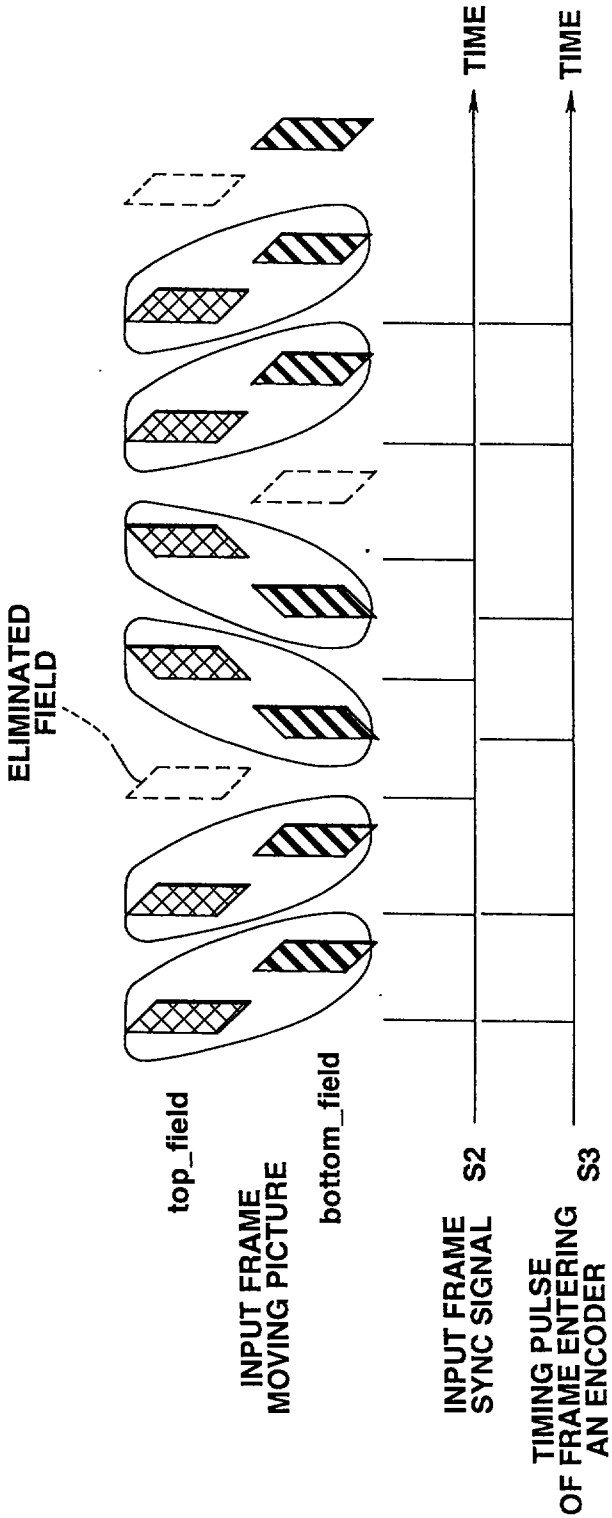

ELIMINATED FIELD
top_field
bottom_field
INPUT FRAME MOVING PICTURE
INPUT FRAME SYNC SIGNAL
S2
TIME
TIMING PULSE OF FRAME ENTERING AN ENCODER
S3
TIME

FIG.3

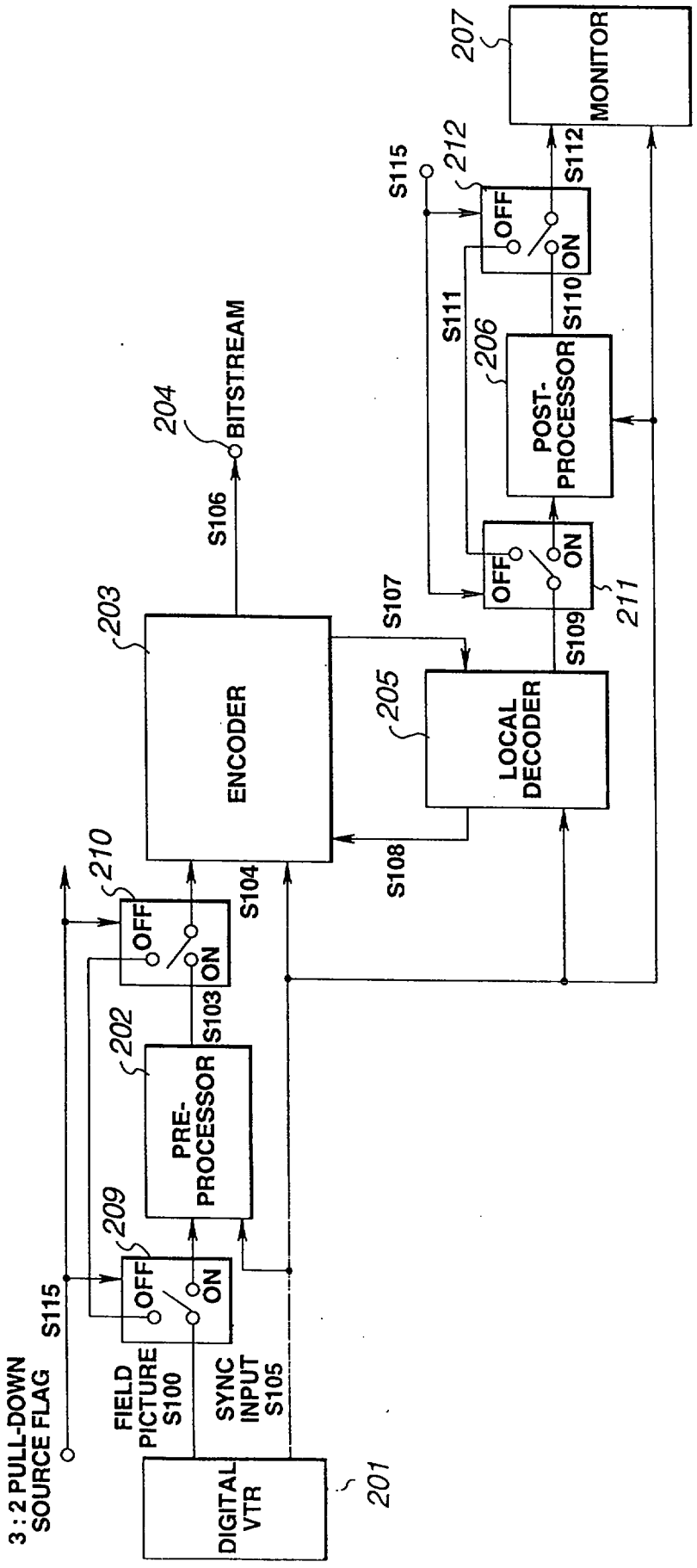

3:2 PULL-DOWN SOURCE FLAG
S115
FIELD PICTURE S100
SYNC INPUT S105
DIGITAL VTR
201
OFF
ON
209
PRE-PROCESSOR
202
S103
OFF
ON
210
S104
ENCODER
203
S106
BITSTREAM
204
S107
S108
LOCAL DECODER
205
OFF
ON
211
S109
S111
POST-PROCESSOR
206
S110
OFF
ON
212
S115
S112
MONITOR
207

FIG.4

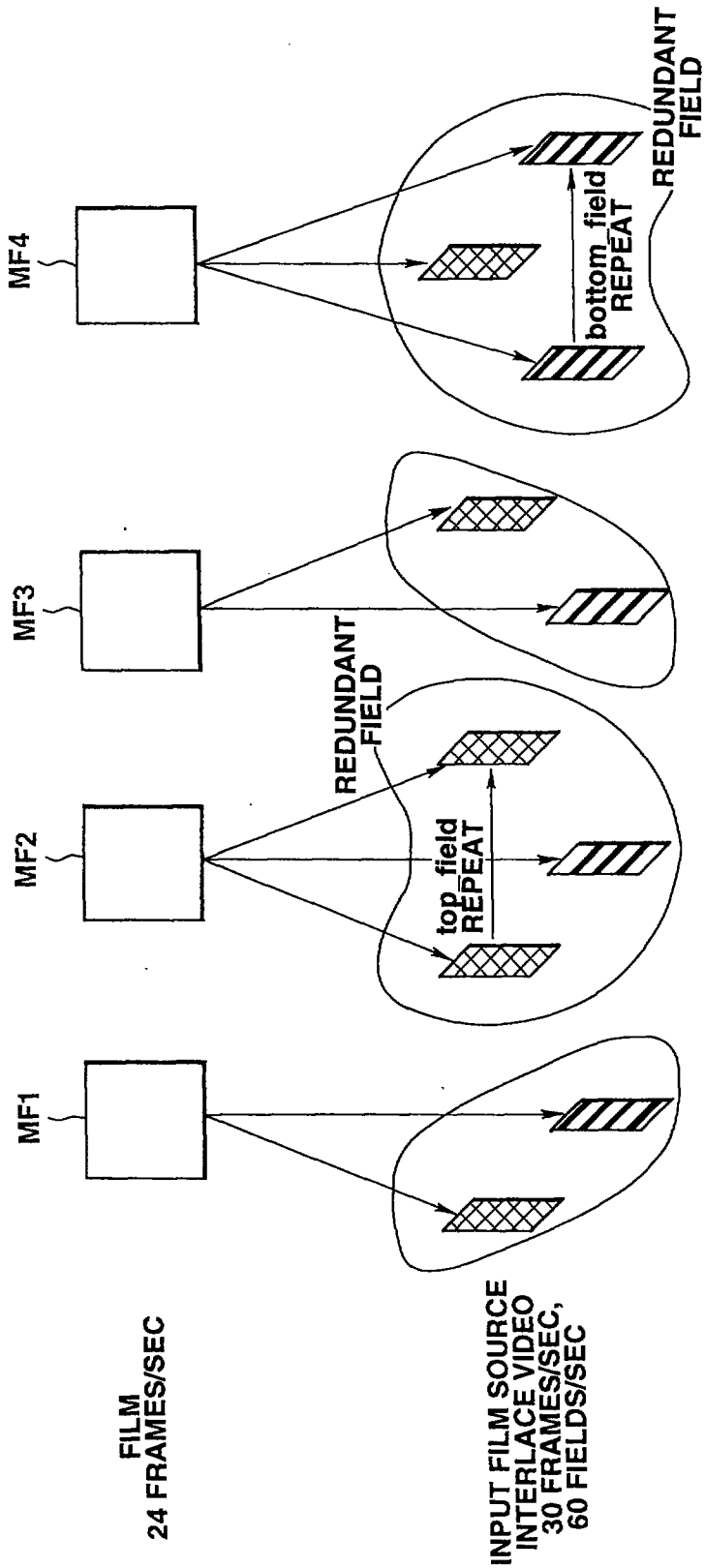

FILM
24 FRAMES/SEC
INPUT FILM SOURCE
INTERLACE VIDEO
30 FRAMES/SEC,
60 FIELDS/SEC
MF1
MF2
MF3
MF4
REDUNDANT FIELD
top_field REPEAT
REDUNDANT FIELD
bottom_field REPEAT
top_field_first FLAG
1
1
0
0
repeat_first_field FLAG
0
1
0
1

FIG.5

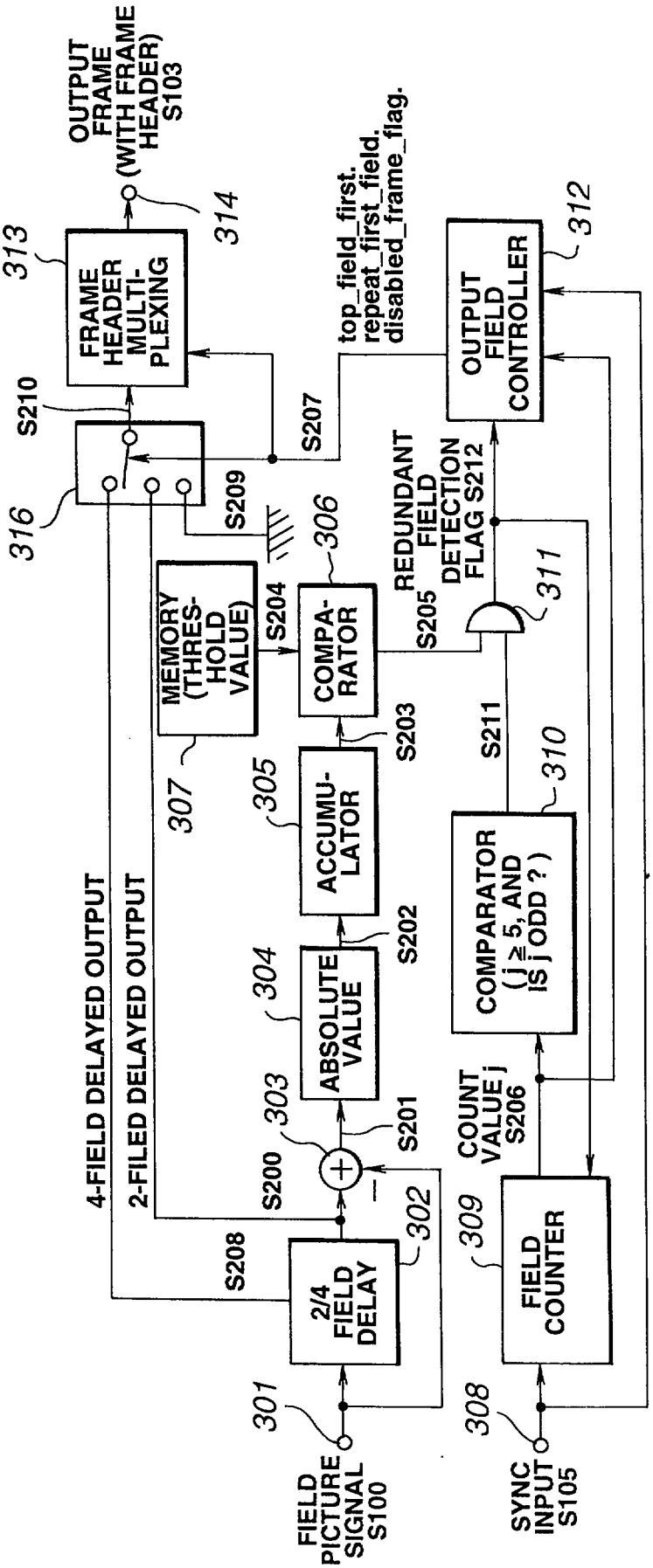

OUTPUT FRAME (WITH FRAME HEADER) S103
314
313
FRAME HEADER MULTI-PLEXING
S210
316
S207
top_field_first,
repeat_first_field,
disabled_frame_flag.
OUTPUT FIELD CONTROLLER
312
S209
306
MEMORY (THRES-HOLD VALUE)
S204
COMPA-RATOR
S205
REDUNDANT FIELD DETECTION FLAG S212
311
307
305
ACCUMU-LATOR
S203
S211
310
4-FIELD DELAYED OUTPUT
2-FILED DELAYED OUTPUT
304
ABSOLUTE VALUE
S202
COMPARATOR (j ≥ 5, AND IS j ODD ?)
303
S201
COUNT VALUE j S206
S200
302
S208
2/4 FIELD DELAY
309
FIELD COUNTER
301
308
FIELD PICTURE SIGNAL S100
SYNC INPUT S105
202

FIG.6

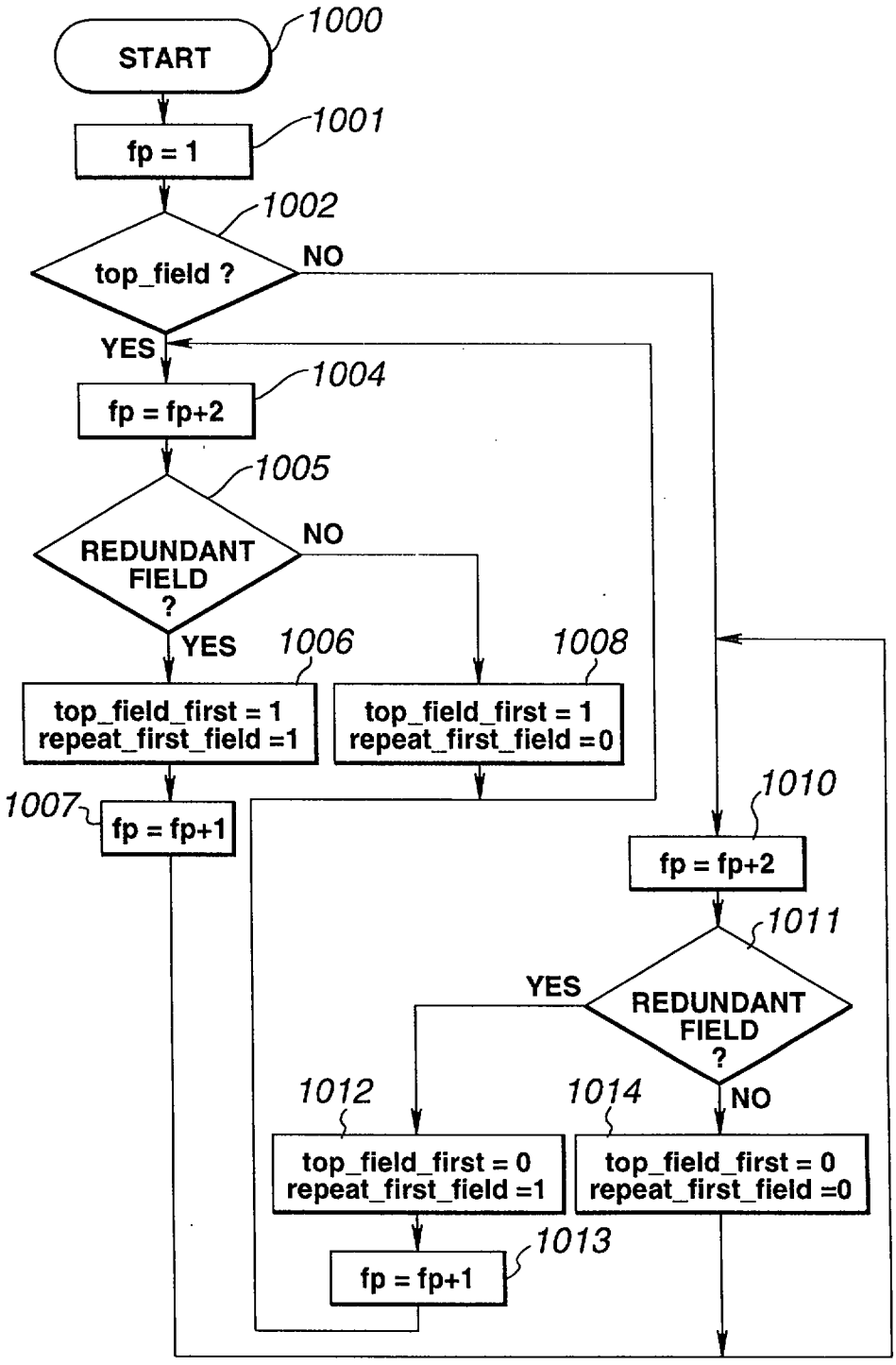

START
1000
fp = 1
1001
top_field ?
1002
NO
YES
fp = fp+2
1004
REDUNDANT FIELD ?
1005
NO
YES
1006
top_field_first = 1
repeat_first_field =1
1008
top_field_first = 1
repeat_first_field =0
1007
fp = fp+1
1010
fp = fp+2
1011
YES
REDUNDANT FIELD ?
NO
1012
top_field_first = 0
repeat_first_field =1
1014
top_field_first = 0
repeat_first_field =0
1013
fp = fp+1

FIG.7

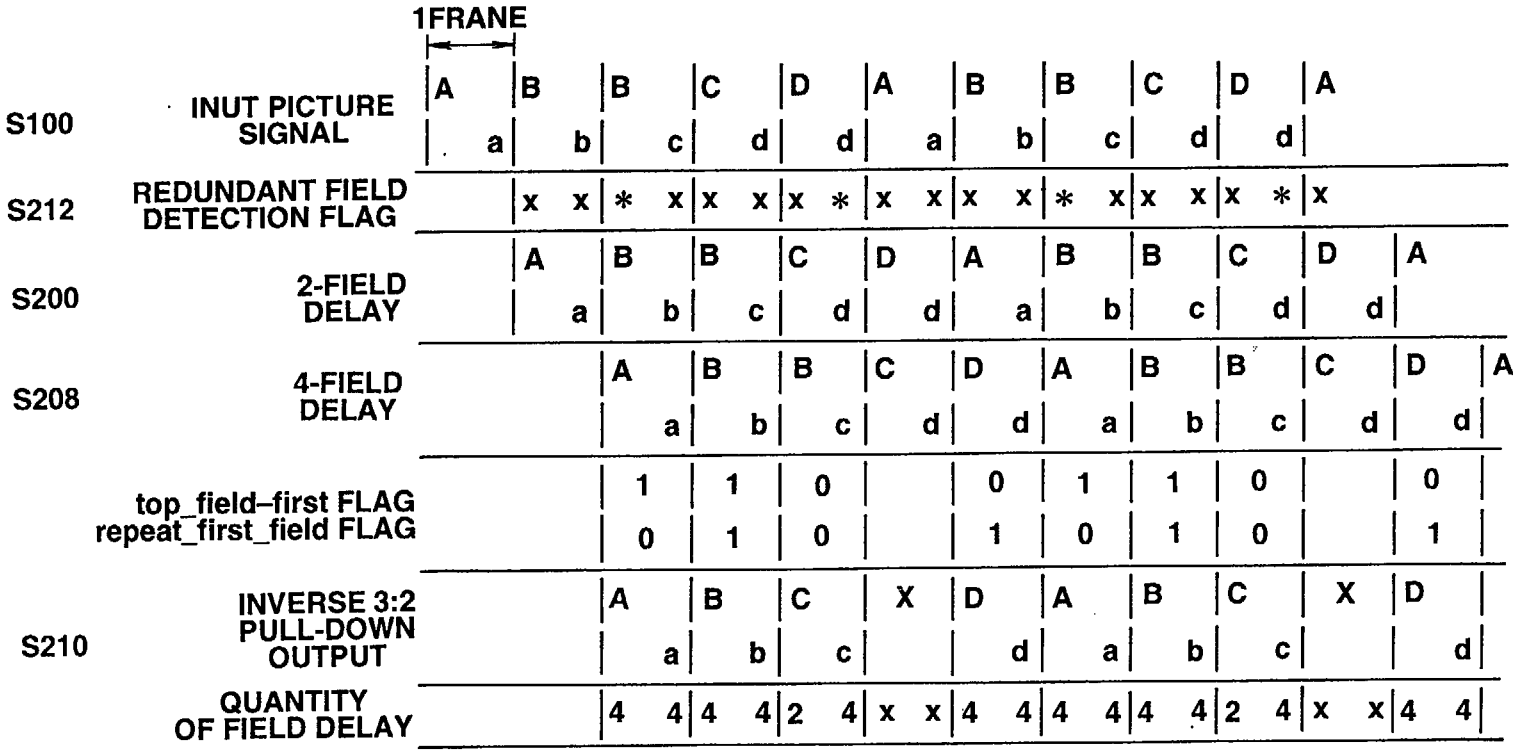

1FRANE
S100
INUT PICTURE SIGNAL
S212
REDUNDANT FIELD DETECTION FLAG
S200
2-FIELD DELAY
S208
4-FIELD DELAY
top_field–first FLAG
repeat_first_field FLAG
S210
INVERSE 3:2 PULL-DOWN OUTPUT
QUANTITY OF FIELD DELAY

FIG.8

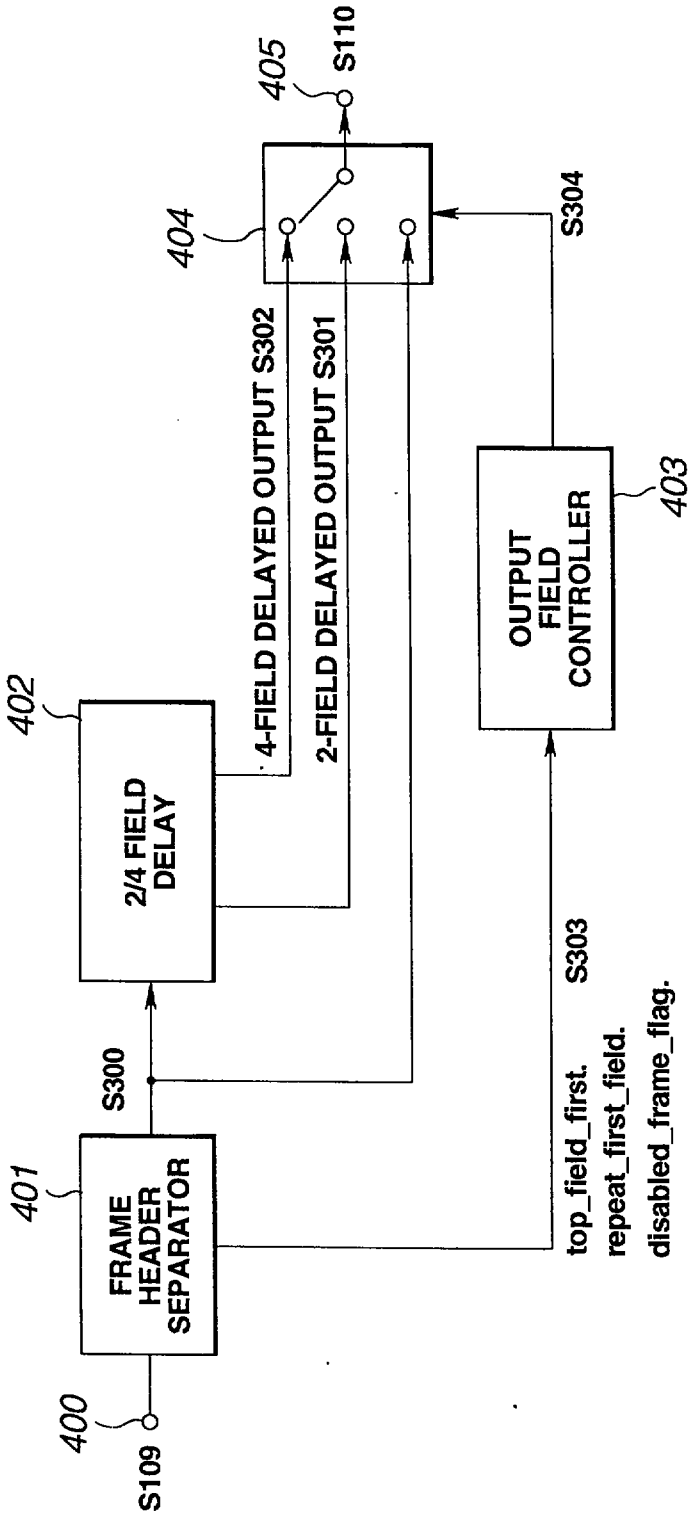

400
S109
401
FRAME HEADER SEPARATOR
S300
402
2/4 FIELD DELAY
4-FIELD DELAYED OUTPUT S302
2-FIELD DELAYED OUTPUT S301
404
405
S110
S304
403
OUTPUT FIELD CONTROLLER
top_field_first.
repeat_first_field.
disabled_frame_flag.
S303

FIG.9

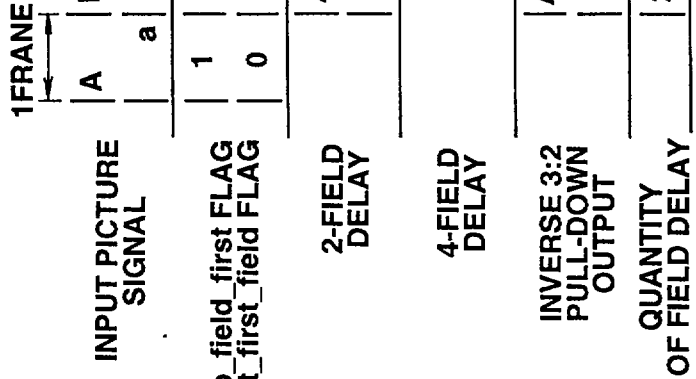

1FRANE
S300
INPUT PICTURE SIGNAL
S303
top_field_first FLAG
repeat_first_field FLAG
S301
2-FIELD DELAY
S302
4-FIELD DELAY
S110
INVERSE 3:2 PULL-DOWN OUTPUT
QUANTITY OF FIELD DELAY

FIG.10

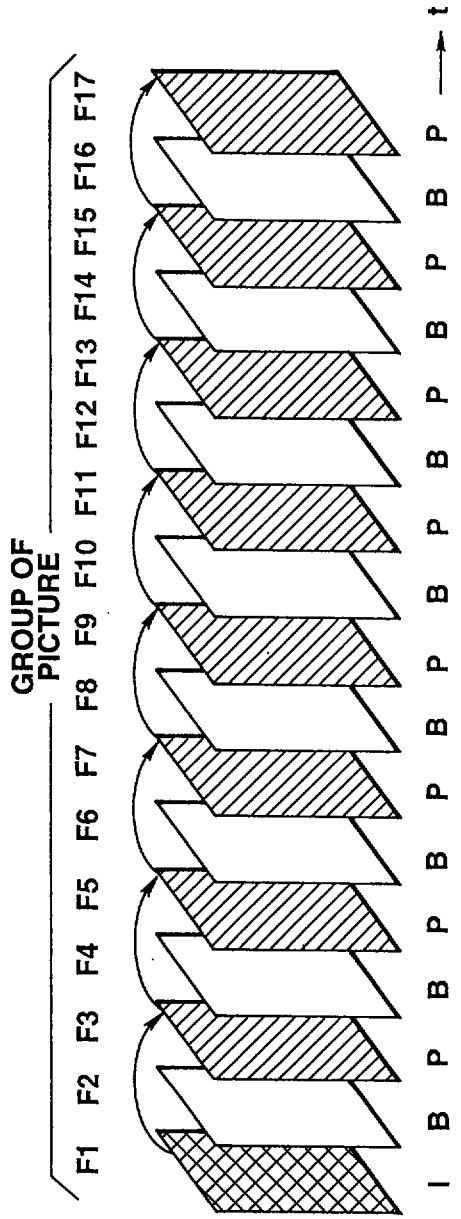


FIG.11A

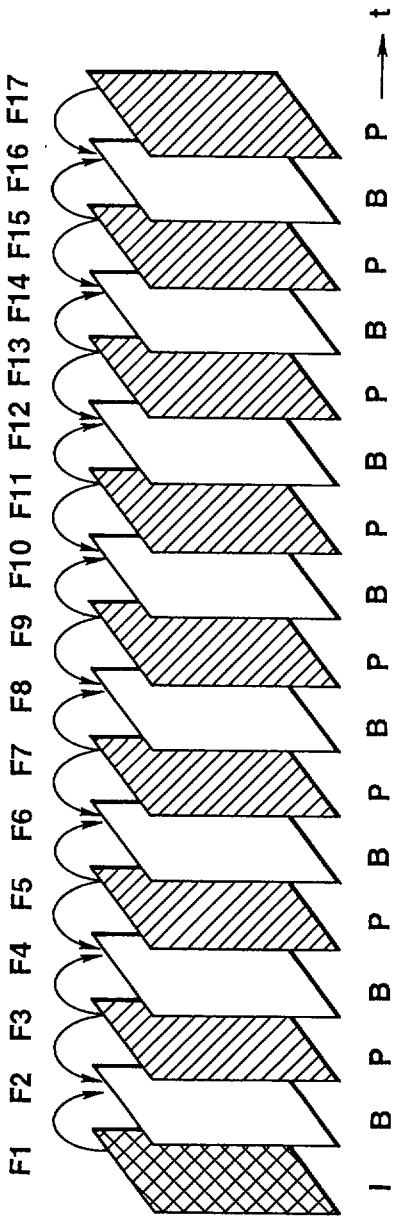


FIG.11B

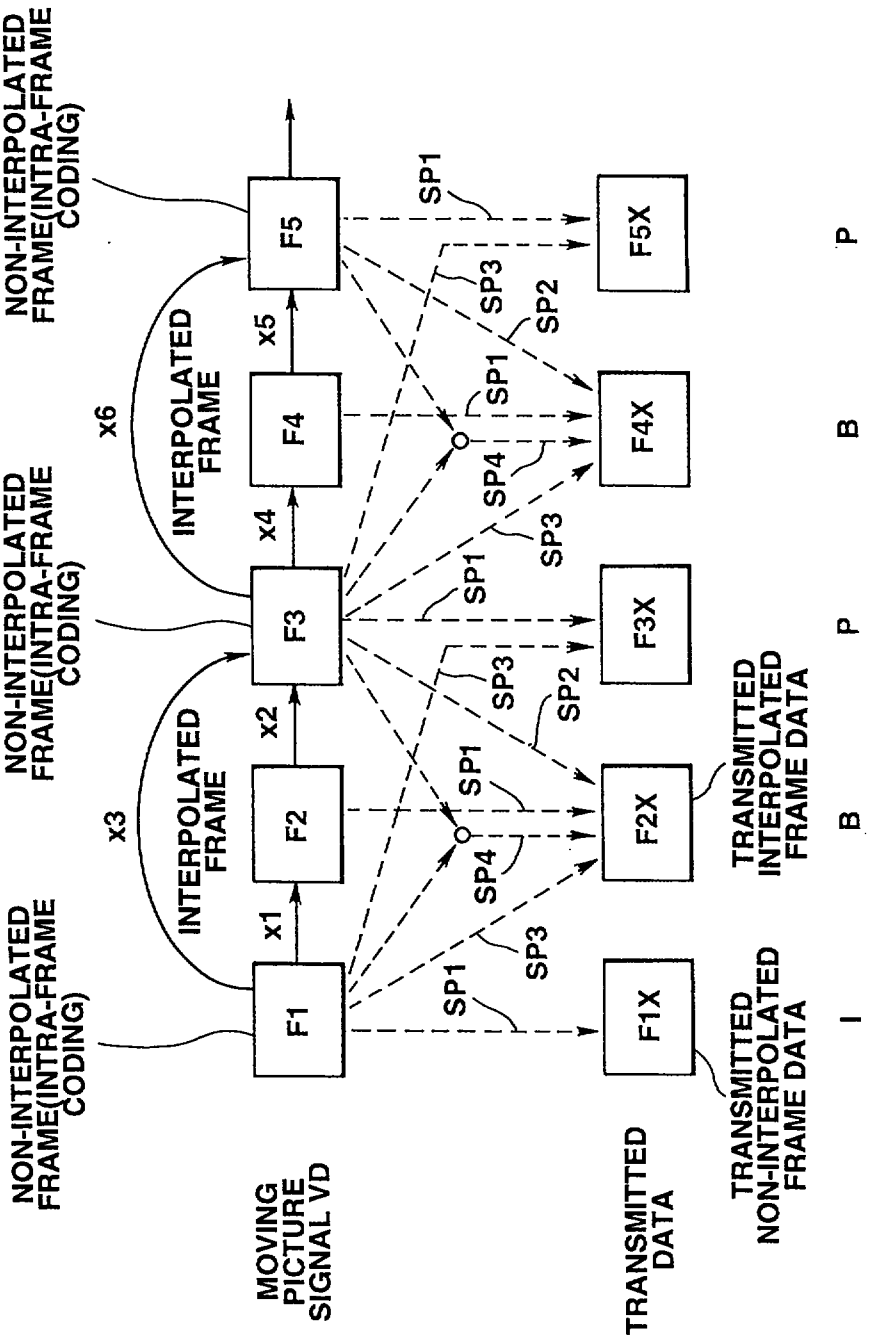

NON-INTERPOLATED FRAME(INTRA-FRAME CODING)
NON-INTERPOLATED FRAME(INTRA-FRAME CODING)
NON-INTERPOLATED FRAME(INTRA-FRAME CODING)
INTERPOLATED FRAME
INTERPOLATED FRAME
x1
x2
x3
x4
x5
x6
F1
F2
F3
F4
F5
F1X
F2X
F3X
F4X
F5X
SP1
SP2
SP3
SP4
MOVING PICTURE SIGNAL VD
TRANSMITTED DATA
TRANSMITTED NON-INTERPOLATED FRAME DATA
TRANSMITTED INTERPOLATED FRAME DATA
I
B
P
B
P

FIG.12

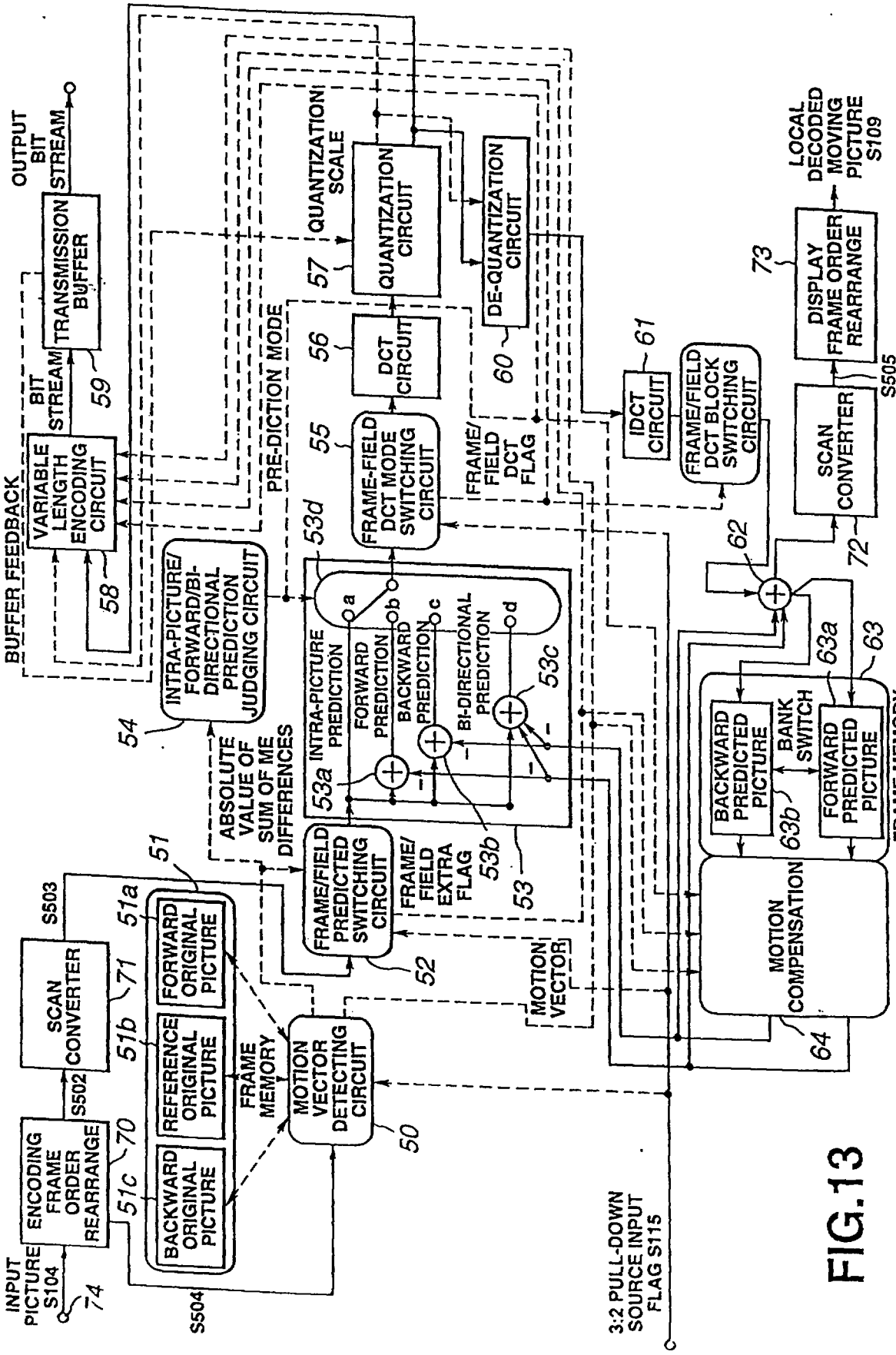

INPUT PICTURE S104
ENCODING FRAME ORDER REARRANGE
SCAN CONVERTER
S502
S503
S504
BACKWARD ORIGINAL PICTURE
REFERENCE ORIGINAL PICTURE
FORWARD ORIGINAL PICTURE
FRAME MEMORY
MOTION VECTOR DETECTING CIRCUIT
INTRA-PICTURE/ FORWARD/BI-DIRECTIONAL PREDICTION JUDGING CIRCUIT
ABSOLUTE VALUE OF SUM OF ME DIFFERENCES
FRAME/FIELD PREDICTED SWITCHING CIRCUIT
INTRA-PICTURE PREDICTION
FORWARD PREDICTION
BACKWARD PREDICTION
BI-DIRECTIONAL PREDICTION
FRAME/FIELD EXTRA FLAG
MOTION VECTOR
PRE-DICTION MODE
FRAME-FIELD DCT MODE SWITCHING CIRCUIT
DCT CIRCUIT
QUANTIZATION CIRCUIT
QUANTIZATION SCALE
DE-QUANTIZATION CIRCUIT
FRAME/FIELD DCT FLAG
IDCT CIRCUIT
FRAME/FIELD DCT BLOCK SWITCHING CIRCUIT
MOTION COMPENSATION
BACKWARD PREDICTED PICTURE
BANK SWITCH
FORWARD PREDICTED PICTURE
FRAME MEMORY
SCAN CONVERTER
DISPLAY FRAME ORDER REARRANGE
LOCAL DECODED MOVING PICTURE S109
S505
VARIABLE LENGTH ENCODING CIRCUIT
TRANSMISSION BUFFER
BUFFER FEEDBACK
BIT STREAM
OUTPUT BIT STREAM
3:2 PULL-DOWN SOURCE INPUT FLAG S115

FIG.13

S104		F02	F02	F03	F04	x01	F05	F06	F07	F08	x02	F09	F10	F11	F12	x03	F13		
S501		I01	B02	P03	B04	x01	P05	B06	P07	B08	x02	P09	B10	P11	B12	x03	P13		
S502				I01	P03	B02	P05	B04	x01	P07	B06	P09	B08	x02	P11	B10	P13	B12	x03

I* *: I - PICTURE
P* *: P- PICTURE
B* *: B - PICTURE
x* *: INVALID FRAME

FIG.14

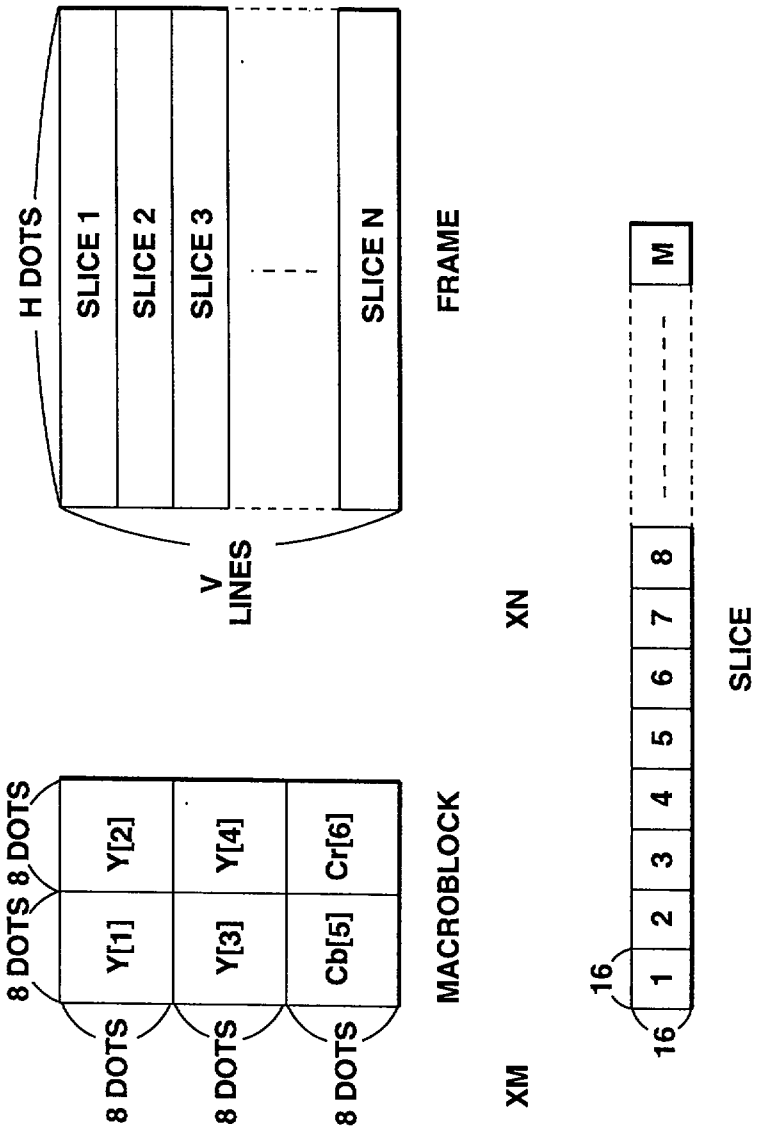

H DOTS
SLICE 1
SLICE 2
SLICE 3
SLICE N
FRAME
V LINES
XN
8 DOTS 8 DOTS
Y[1]
Y[2]
Y[3]
Y[4]
Cb[5]
Cr[6]
MACROBLOCK
8 DOTS
8 DOTS
8 DOTS
XM
16
16
1
2
3
4
5
6
7
8
M
SLICE

FIG.15

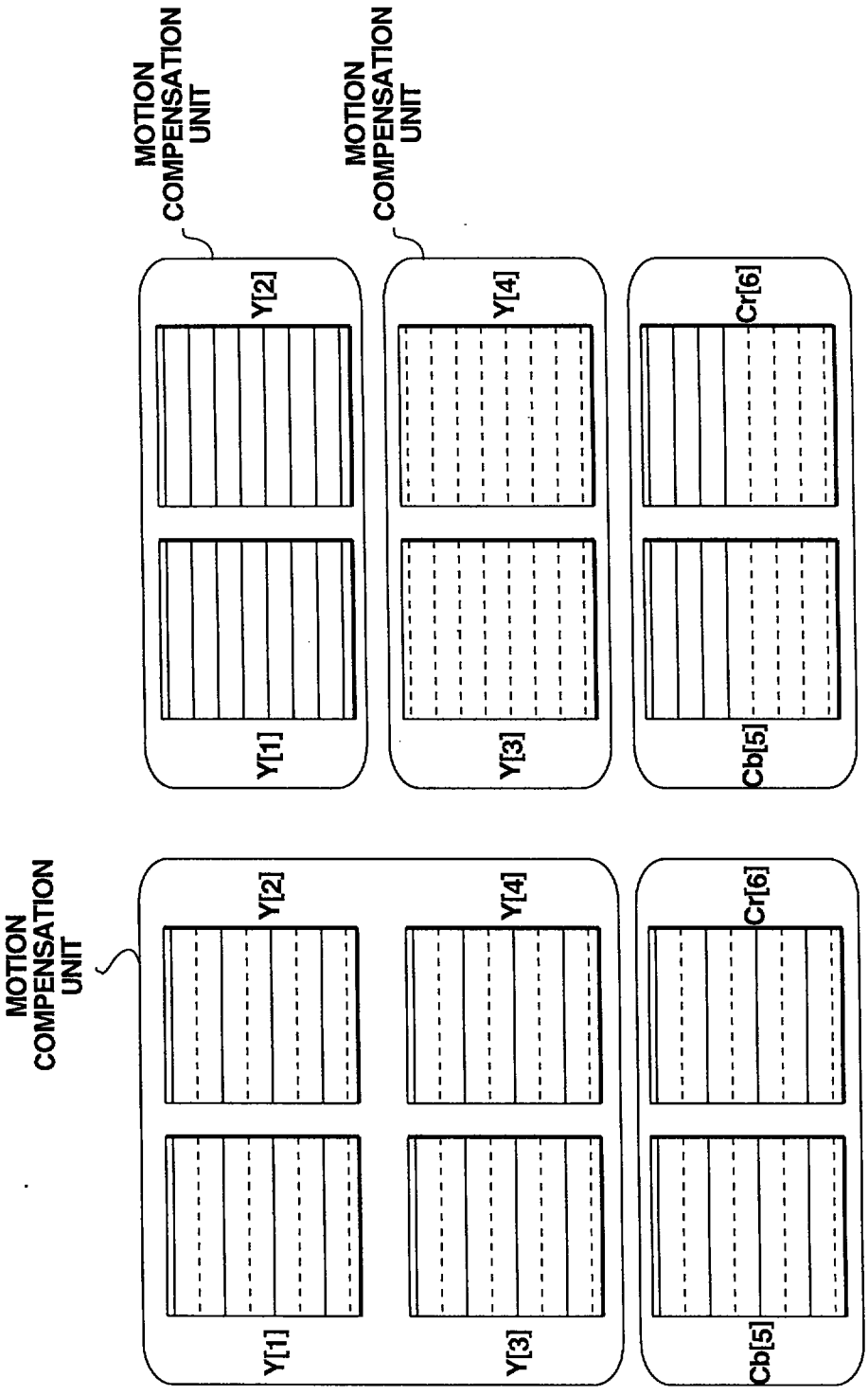


FIG.16A

FIG.16B

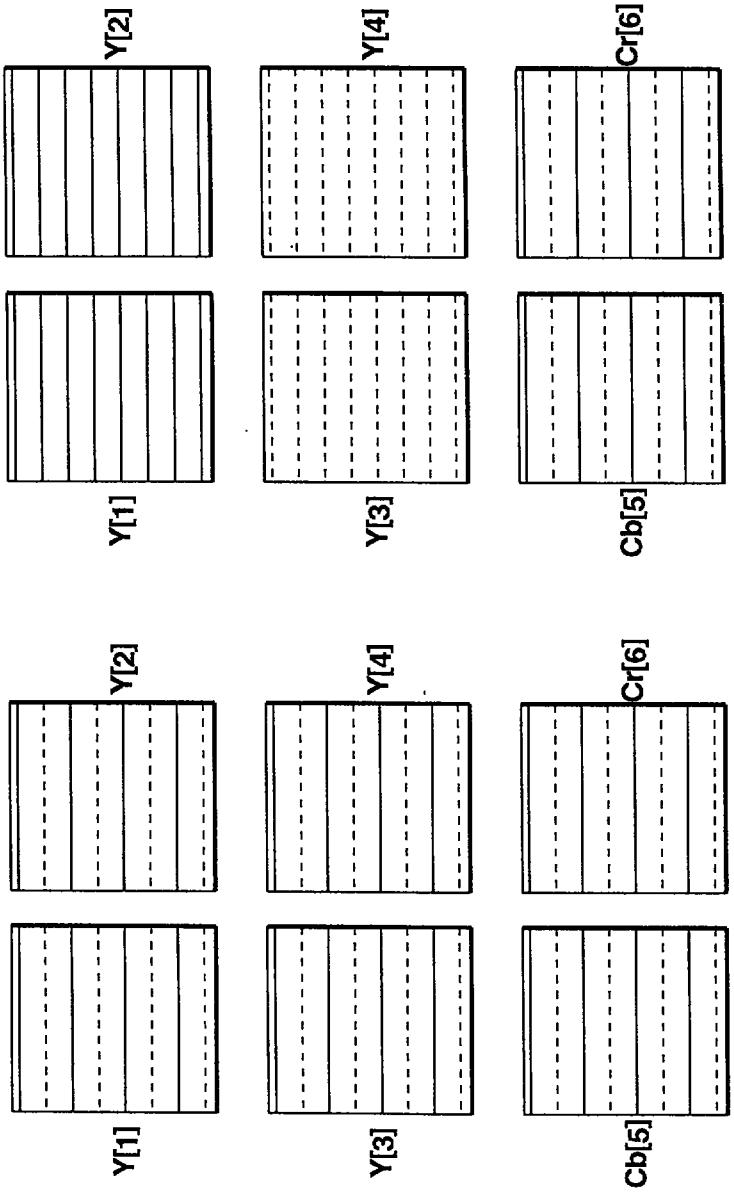


FIG.17A

FIG.17B

S505		I01	P03	B02	P05	B04	x01	P07	B06	P09	B08	x02	P11	B10	P13	B12	x03	
S109			I01	B02	P03	B04	x01	P05	B06	P07	B08	x02	P09	B10	P11	B12	x03	P13

I* *: I - PICTURE
P* *: P- PICTURE
B* *: B - PICTURE
x* *: INVALID FRAME

FIG.18

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What is claimed is:

1. A method of processing a signal representing a moving picture which is divided into a plurality of frames such that each respective frame is formed of one odd field and one even field, the signal generated according to a 3:2 pull-down process where each respective redundant field is repeated after two respective frames for converting a motion picture film to a moving pictures video and supplied at a predetermined clock rate from a moving picture source for input to a signal processing device for predetermined processing operations on the input signal, said method comprising the steps of:

detecting a redundant field from the input signal;

combining the odd and even fields to form the respective frames such that the redundant field is eliminated from the input signal;

inserting a predetermined invalid frame into the input signal to obtain an output signal for processing at a substantially the same clock rate as the predetermined clock rate of the input signal such that the moving picture source and signal processing device are synchronized to operate at substantially the same clock rate; and

adding supplemental data to the output signal for indicating which of the respective odd and even fields are combined to form the respective frames and for indicating where the predetermined invalid frame is inserted, wherein the supplemental data includes a first flag for specifying whether the odd field precedes the even field in the respective frame of the input signal, a second flag for specifying whether the respective frame of the input signal contains two fields or three fields, and a third flag for specifying whether a current frame of the output signal is the predetermined invalid frame.

2. The method according to claim 1, wherein the predetermined processing operations include an encoding operation for signal compression, wherein the encoding operation is not carried out for the predetermined invalid

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frame if the third flag is active.

3. The method according to claim 2, wherein the redundant field is detected by calculating a difference between two fields of the input signal.

4. The method according to claim 3, wherein the two fields between which the difference is calculated are successive odd or even fields.

5. The method according to claim 4, wherein the redundant field is detected by counting the fields of the input signal such that upon reaching a predetermined count the difference between the two fields is calculated.

6. A method of restoring a processed signal representing a moving picture which is divided into a plurality of frames such that each respective frame is formed of one odd field and one even field, the processed signal obtained by detecting a redundant field from an input signal generated according to a 3:2 pull-down process where each respective redundant field is repeated after two respective frames for converting a motion picture film to a moving pictures video, by combining the odd and even fields to form the respective frames such that the redundant field is eliminated from the input signal, by inserting a predetermined invalid frame into the input signal to obtain an output signal for processing at a substantially the same clock rate as a predetermined clock rate of the input signal, and by adding supplemental data to the output signal, wherein the supplemental data includes a first flag for specifying whether the odd field precedes the even field in the respective frame of the input signal, a second flag for specifying whether the respective frame of the input signal contains two fields or three fields, and a third flag for specifying whether a current frame of the output signal is the predetermined invalid frame, said method comprising the steps of:

separating from the processed signal the supplemental data which indicates which of the respective odd and even fields were combined to form the respective frames and further indicates where the predetermined invalid frame was

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inserted;

removing the predetermined invalid frame from the processed signal based on the supplemental data; and

repeating a respective field in the processed signal at a portion from which the predetermined invalid frame was removed for generating the redundant field, whereby the processed signal is substantially the same as the input signal.

7. An apparatus for processing a signal representing a moving picture which is divided into a plurality of frames such that each respective frame is formed of one odd field and one even field, the signal generated according to a 3:2 pull-down process where each respective redundant field is repeated after two respective frames for converting a motion picture film to a moving pictures video and supplied at a predetermined clock rate from a moving picture source for input to a signal processing device for predetermined processing operations on the input signal, said apparatus comprising:

means for detecting redundant field from the input signal;

means for combining the odd and even fields to form the respective frames such that the redundant field iseliminated from the input signal;

means for inserting a predetermined invalid frame into the input signal to obtain an output signal for processing at a substantially the same clock rate as the predetermined clock rate of the input signal such that the moving picture source and signal processing device are synchronized to operate at substantially the same clock rate; and

means for adding supplemental data to the output signal for indicating which of the respective odd and even fields are combined to form the respective frames and for indicating where the predetermined invalid frame is inserted, wherein the supplemental data includes a first flag for specifying whether the odd field precedes the even field in the respective frame of the input signal, a second flag for specifying whether the respective frame of the

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input signal contains two fields or three fields, and a third flag for specifying whether a current frame of the output signal is the predetermined invalid frame.

8. The apparatus according to claim 7, wherein the predetermined processing operations include an encoding operation for signal compression, wherein the encoding operation is not carried out for the predetermined invalid frame if the third flag is active.

9. The apparatus according to claim 8, wherein the means for detecting a redundant field comprises means for calculating a difference between two fields of the input signal.

10. The apparatus according to claim 9, wherein the two fields between which the difference is calculated are successive odd or even fields.

11. The apparatus according to claim 10, wherein the means for calculating includes means for counting the fields of the input signal such that upon reaching a predetermined count the difference between the two fields is calculated.

12. An apparatus for restoring a processed signal representing a moving picture which is divided into a plurality of frames such that each respective frame is formed of one odd field and one even field, the processed signal obtained by detecting a redundant field from an input signal generated according to a 3:2 pull-down process where each respective redundant field is repeated after two respective frames for converting a motion picture film to a moving pictures video, by combining the odd and even fields to form the respective frames such that the redundant field is eliminated from the input signal, by inserting a predetermined invalid frame into the input signal to obtain an output signal for processing at a substantially the same clock rate as a predetermined clock rate of the input signal, and by adding supplemental data to the output signal, wherein the supplemental data includes a first flag for specifying whether the odd field precedes the even field in the respective frame of the input signal, a second flag for specifying whether the respective frame of the input

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signal contains two fields or three fields, and a third flag for specifying whether a current frame of the output signal is the predetermined invalid frame, said apparatus comprising:

means for separating from the processed signal the supplemental data which indicates which of the respective odd and even fields had been combined to form the respective frames and further indicates where the predetermined invalid frame has been inserted;

means for removing the predetermined invalid frame from the processed signal based on the supplemental data; and

means for repeating a respective field in the processed signal at portion from which the predetermined invalid frame had been removed for generating the redundant field, whereby the processed signal is substantially the same as the input signal.

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