

PACKAGE SUBSTRATE, SEMICONDUCTOR DEVICE, AND ELECTRONIC APPARATUS

ABSTRACT

5 This application provides a package substrate, a semiconductor device, and an electronic
device, to reduce crosstalk between pins of a chip, and reduce a packaging area by increasing
utilization of pins, thereby reducing development costs of the semiconductor device. The package
substrate includes a substrate body and a plurality of unit regions disposed on the substrate body.
The unit region includes two first solder ball structures. The first solder ball structure includes six
first solder balls. The six first solder balls are arranged, with two of them in a row, to form three
10 parallel rows of two solder balls: a first row of solder balls, a second row of solder balls, and a
third row of solder balls. Four first solder balls in the first row of solder balls and the second row
of solder balls are respectively located at four vertices of one parallelogram, and four first solder
balls in the second row of solder balls and the third row of solder balls are respectively located at
four vertices of the other parallelogram; and the two parallelograms are arranged axisymmetric
15 about the second row of solder balls.
(Fig.4)