

FREQUENCY MODULATION RECEIVER IN
PARTICULAR FOR AN RDS APPLICATION

The present invention concerns the field of frequency modulation receivers (hereinafter " FM receivers ") able to receive a signal at a high frequency from a transmitter, particularly for a Radio Data System (RDS) application.

With reference to Figure 1 of the present description, French Patent
5 No. 2705,176 discloses a conventional FM receiver 1 which includes an antenna 2, a high frequency stage (RF) 3, a mixer 4, a local oscillator 5, an intermediate frequency (IF) filter 6, an amplifier/limiter 7, an FM demodulation stage 8 and an automatic frequency control (AFC) stage 9.

Antenna 2 receives a signal having a frequency comprised within the FM
10 transmission band (i.e. between 88 and 108 MHz), and supplies the corresponding electric signal to RF stage 3.

RF stage 3 is tuned onto the carrier frequency f_c of a predetermined transmitter so as to provide, in response to the electric signal originating from the antenna, an amplified signal having a frequency comprised within a frequency band centred on
15 frequency f_c .

Mixer 4 receives the signal originating from RF stage 3, as well as a signal originating from local oscillator 5, multiplies these signals, and supplies to IF filter 6 a signal modulated at an intermediate frequency f_{IF} , the latter being generally chosen to be equal to approximately 70 kHz.

20 IF filter 6 is arranged to receive the signal modulated at frequency f_{IF} and, in response to provide a signal located within a frequency band centred around intermediate frequency F_{IF} .

Amplifier/limiter 7 receives the signal originating from IF filter 6, limits its amplitude to eliminate any amplitude modulation (AM) component and, in response,
25 provides this amplified/limited signal.

FM demodulation stage 8 demodulates the signal originating from amplifier/limiter 7, and provides the demodulated signal to an audio amplifier (not shown in Figure 1).

AFC stage 9 allows fine tuning to be performed between frequency f_{LO} of the
30 signal from local oscillator 5 as a function of the continuous output of demodulator 8 in order to keep intermediate frequency f_{IF} constant.

One problem of an FM radio receiver such as that shown in Figure 1 consists in the fact that considerable distortion can appear by aliasing, when the modulation frequency (i.e. that of the message signal) is greater than half of intermediate
35 frequency f_{IF} .

The problem of aliasing distortion arises particularly in transmission systems using frequency division multiplexing, as is the case in Europe with FM broadcasting, in particular for an RDS application. Indeed, the effect of such distortion can be that decoding the RDS data becomes impossible.

5 Figure 2 of the present description shows the frequency spectral distribution of the signals present in FM receiver 1, during an RDS application. Audio data are modulated in stereophony on a sub-carrier of 38 kHz, while other data corresponding to the RDS data are present in the form of low amplitude signals modulated on a sub-carrier of 57 kHz by phase shift (PSK modulation). In order to allow the RDS data to be
10 decoded, and with reference once more to Figure 1, the output bandwidth of FM demodulation stage 8 would have to be at least 60 kHz. Indeed, assuming that the intermediate frequency f_{IF} used is of the order of 70 kHz, the audio data and the RDS data can be mixed by aliasing.

 A first conventional solution to the problem of frequency aliasing consists in
15 using a higher frequency f_{IF} . US Patent No. 4,885,802 discloses an FM receiver implementing such a solution.

 One drawback of such an FM receiver lies in the fact that it requires the use of additional means to filter the response of the image frequency of the RF signal, which also increases the electric power consumption.

20 Another drawback of such an FM receiver lies in the fact that the maximum intermediate frequency which can be used is imposed by the image frequency rejection and by the spacing of the channels or transmitters in the FM broadcasting band. Consequently, the audio bandwidth of the demodulated signals cannot thus simply be improved by increasing intermediate frequency f_{IF} of the FM receiver.

25 A second conventional solution to the problem of frequency aliasing consists in providing a signal having a higher frequency than intermediate frequency f_{IF} to the demodulation stage.

 With reference to Figure 3 of the present description, US Patent No. 5,483,695 discloses an FM receiver implementing such a solution. It will be noted in Figure 3 that
30 similar objects to those in Figure 1 have been designated by the same references. FM receiver 20 further includes a signal generator circuit 24 able to generate n signals at intermediate frequency f_{IF} , and a multiplier circuit 28 able to multiplier between them the n signals to provide a signal modulated at a frequency equal to n times intermediate frequency f_{IF} .

35 One drawback of FM receiver 20 lies in the fact that it is necessary to generate signals in phase quadrature and having a frequency equal to intermediate frequency f_{IF} , which considerably increases the electric power consumption.

One object of the present invention is to provide an FM radio receiver for an RDS application which overcomes the aliasing problem, in particular an FM radio receiver able to extract the RDS data present in a radio-frequency signal received by said receiver.

5 Another object of the present invention is to provide an FM radio receiver answering the usual criteria in the semiconductor industry as to low electric power consumption.

Another object of the present invention is to provide an FM radio receiver in the form of an integrated circuit answering the usual criteria in the semiconductor industry
10 as to rationality and surface occupation.

These objects, in addition to others, are achieved by the FM receiver according to claim 1.

One advantage of the arrangement of the locked loop of such a receiver is that intermediate frequency f_{IF} is enslaved to a predetermined value so that the aliasing
15 phenomenon does not prevent decoding of the RDS data present in a radio-frequency signal received by the receiver.

Another advantage of such an arrangement is that the receiver may operate with low intermediate frequencies f_{IF} , without it being necessary to use high frequency values, or frequency multiplication. This results in low electric power consumption,
20 which allows an FM receiver of this type to be used for an RDS application, for example.

These objects, features and advantages of the present invention in addition to others, will appear more clearly upon reading the detailed description of a preferred embodiment of the invention, given solely by way of example, with reference to the
25 annexed drawings, in which:

- Figure 1, which has already been cited, shows a first conventional FM receiver;

- Figure 2, which has already been cited, shows the spectral frequency distribution of the signals present in the FM receiver of Figure 1, during an RDS
30 application;

- Figure 3, which has already been cited, shows a second conventional FM receiver;

- Figure 4 shows a preferred embodiment of an FM receiver according to the present invention;

- Figure 5 shows in detail a circuit of the FM receiver of Figure 4;

- Figure 6 shows in detail another circuit of the FM receiver of Figure 4;

- Figures 7A to 7C show the spectral frequency distributions of signals present in the FM receiver of Figure 4, during an RDS application, for three different predetermined values respectively; and

- Figure 8 shows an improvement of the circuit of Figure 6.

5 With reference to Figure 4, a preferred embodiment of an FM receiver according to the present invention will be described. It will be noted in Figure 4 that the reference 29 designates such a receiver, and that similar objects to those of Figure 1 have been designated by the same references.

10 FM receiver 29 includes an antenna 2, a local oscillator 5, a mixer unit 30, a demodulation stage 8 and an automatic frequency control (AFC) stage 36. It will be noted that a receiver of this type is able to be made in a device requiring the supply of RDS data, for example in a timepiece such as a wristwatch.

15 Antenna 2 includes an output terminal 2a connected to RF stage 3. Antenna 2 is arranged to be able to receive a signal having a frequency comprised within the FM transmission band (i.e. between 88 and 108 MHz) and, in response, to supply an electrical signal S1 representative of the received signal via terminal 2a.

Local oscillator 5 includes two input terminals 5a and 5b and an output terminal 5c connected to mixer unit 30. Local oscillator 5 is arranged to provide an electric signal S3, as is described in more detail hereinafter.

20 Mixer unit 30 includes an input terminal 30a connected to output terminal 3b of RF stage 3, an input terminal 30b connected to output terminal 5c of local oscillator 5, and an output terminal 30c connected to demodulation stage 8. Mixer unit 30 is arranged to supply, in response to signals S2 and S3, an electric signal S6 at an intermediate frequency f_{IF} .

25 Preferably, mixer unit 30 is made by connecting in series a mixer 4, an IF filter 6 and an amplifier/limiter 7, as shown in Figure 5.

30 Mixer 4 includes two input terminals 4a and 4b connected to the respective terminals 30a and 30b of mixer unit 30, and an output terminal 4c connected to IF filter 6. Mixer 4 is arranged to be able to: receive, via terminal 4a, signal S2, and via terminal 4b; electric signal S3; multiply signals S2 and S3 by each other; and supply, via terminal 4c, an electric signal S4 so that the latter is modulated at intermediate frequency f_{IF} . By way of example, intermediate frequency f_{IF} is selected to be equal to approximately 70 kHz.

35 IF filter 6 includes an input terminal 6a connected to output terminal 4c of mixer 4, and an output terminal 6b connected to a amplifier/limiter 7. IF filter 6 is arranged to be able to receive, via terminal 6a, signal S4 and, in response, to supply an electric signal S5 located within a frequency band centred around intermediate frequency f_{IF} .

Amplifier/limiter 7 includes an input terminal 7a connected to output terminal 6b of IF filter 6, and an output terminal 7b connected to output terminal 30c of mixer unit 30. Amplifier/limiter 7 is arranged to be able to receive, via terminal 7a, signal S5, limit the amplitude of this signal to eliminate any AM component therefrom and, in response, to supply signal S6 via terminal 7b.

With reference once more to Figure 4, FM demodulation stage 8 includes an input terminal 8a connected to output terminal 7b of amplifier/limiter 7, and an output terminal 8b connected to an audio amplifier (not shown in Figure 4). FM demodulation stage 8 is arranged to be able to receive, via terminal 8a, signal S6, demodulate this signal and, in response, supply an electric signal S7 representing demodulated signal S6.

It is to be noted that an embodiment of demodulation stage 8 is disclosed in US Patent No. 5,808,510.

AFC stage 36 includes an input terminal 36a connected to output terminal 7b of amplifier/limiter 7, and an output terminal 36c connected to input terminal 5b of local oscillator 5. AFC stage 36 is arranged to allow fine tuning to be performed between frequency f_{LO} of signal S3 of local oscillator 5, in order to keep intermediate frequency f_{IF} constant, as is described in more detail hereinafter.

FM receiver 29 further includes a locked loop 32 arranged to enslave intermediate frequency f_{IF} from a pilot frequency f_p . It will be recalled that such a frequency is always available in an FM multiplex signal, and allows reconstitution of the carrier which is removed in a stereophonic FM receiver. Within the scope of the present description, pilot frequency f_p is present in signal S7, and is typically equal to 19 kHz.

For this purpose, locked loop 32 includes a phase locked loop (PLL) filter 34 and AFC stage 36.

Filter 34 includes an input terminal 34a connected to output terminal 8b of demodulation stage 8, and an output terminal 34b connected to AFC stage 36. Filter 34 is arranged to receive, via terminal 34a, signal S7 and, in response, supply, via terminal 34b, an electric signal S8 having a substantially equal frequency to pilot frequency f_p .

Filter 34 may be made from a phase locked loop (PLL) having a bandwidth determined so as to be able to supply the signal at pilot frequency f_p and with a high signal to noise ratio (SNR). This allows a stable reference frequency to be provided, capable of performing the AFC function, without it being necessary to use additional means able to provide a reference frequency.

AFC stage 36 further includes an input terminal 36b connected to output terminal 34b of filter 34. AFC stage 36 is arranged to be able to receive signal S6 at intermediate frequency f_{IF} and signal S8 at pilot frequency f_p and, in response, provide an electric signal S9 able to control local oscillator 5 (i.e. the supply of signal S3 at frequency f_{LO}) so that intermediate frequency f_{IF} has a mean value enslaved to a predetermined value, as is described hereinafter.

Figure 6 shows in detail an embodiment of AFC stage 36 which includes a first frequency divider 38, a phase and frequency comparator 40 and a loop filter 42.

Divider 38 includes an input terminal 38a connected to input terminal 36a of AFC stage 36, and an output terminal 38b connected to comparator 40. Divider 38 is arranged to be able to receive, via terminal 38a, signal S6 at frequency f_{IF} and, in response, supply, via terminal 38b, an electric signal S11 at a frequency equal to : f_{IF}/N , N being an integer number.

Comparator 40 includes an input terminal 40a connected to output terminal 38b of divider 38, an input terminal 40b connected to input terminal 36b of AFC stage 36, and an output terminal 40c connected to filter 42. Comparator 40 is arranged to be able to receive, via terminals 40a and 40b, signal S11 at frequency f_{IF}/N and signal S8 at pilot frequency f_p , to compare signals S11 and S8 with each other and, in response, to supply, via terminal 40c, an error signal S12 which is proportional to the frequency difference between frequencies f_{IF}/N and f_p .

Filter 42 includes an input terminal 42a connected to output terminal 40c of comparator 40, and an output terminal 42b connected to output terminal 36c of AFC stage 36. Filter 42 is arranged to be able to receive, via terminal 42a, signal S12 and, in response, to supply via terminal 42b, signal S9 representative of the difference between frequencies f_{IF}/N and f_p .

Essentially, with reference to Figures 4 to 6, when loop 32 is locked, intermediate frequency f_{IF} then has a mean value which is substantially equal to : $N \cdot f_p$, this value corresponding to said predetermined value which allows the signals containing the RDS data to be decoded.

Three cases representative of three frequency ranges in which said predetermined value can be chosen so as to allow decoding of the signals containing the RDS data, will now be described, purely by way of example. These three cases will be described with reference once more to Figure 2, and in relation to the respective Figures 7A to 7C which show the spectral distributions of the signals containing the RDS data and frequency f_{IF} for three different predetermined values respectively.

With reference to Figure 7A, let us consider the first case wherein said predetermined value is chosen so that frequency f_{IF} is enslaved to 76 kHz, taking the values cited in relation to Figure 2.

With reference to Figure 7B, let us consider the second case wherein said
5 predetermined value is chosen so that frequency f_{IF} is comprised between 72 and 73.5 kHz, taking the value cited in relation to Figure 2.

With reference to Figure 7C, let us consider the third case wherein said predetermined value is chosen so that frequency f_{IF} is comprised between 78.5 and 80 kHz, taking the values cited in relation to Figure 2.

10 Thus, in the aforementioned three cases, there is no overlap between the spectral distribution of the signals containing the RDS data and those of the audio data, so that the aliasing phenomenon does not prevent demodulation of the signals containing the RDS data.

It goes without saying for those skilled in the art that the above description may
15 undergo various modifications without departing from the scope of the present invention.

By way of improvement, and with reference once again to Figure 4, receiver 29 may include a high frequency (RF) stage 3, including an input terminal 3a connected to output terminal 2a of antenna 2, and an output terminal 3b connected to mixer unit
20 30. RF stage 3 is arranged to be able to receive, via terminal 3a, signal S1 and, in response, to supply, via terminal 3b, an amplified electric signal S2 having a frequency comprised within a frequency band centred on a carrier frequency f_c of a predetermined transmitter.

One advantage of such an arrangement of RF stage 3 is that it substantially
25 increases the sensitivity of receiver 29, so that the latter can then operate with RF signals of low amplitude.

Also by way of improvement, and with reference once more to Figure 4, receiver 29 can include a frequency locked loop (FLL) 31 including an input terminal 31a connected to output terminal 8b of demodulation stage 8, to receive signal S7,
30 and an output terminal 31b connected to input terminal 5a of local oscillator 5, to supply a signal S10.

One advantage of such an arrangement of FLL filter 31 is that the deviation of signal S6 can be reduced.

Also by way of improvement, and with reference to Figure 8, AFC stage 36 can
35 further include a second frequency divider 44. It is to be noted in Figure 8 that similar objects to those of Figure 6 have been designated by the same references.

As Figure 8 shows, divider 44 includes an input terminal 44a connected to input terminal 36b of AFC stage 36, and an output terminal 44b connected to input terminal 40b of comparator 40. Divider 44 is arranged to be able to receive, via terminal 44a, signal S8 at pilot frequency f_p and, in response, to supply via terminal 44b, an electric
5 signal S13 at a frequency equal to: f_p/M , M being an integer number.

Essentially, and with reference to Figures 4 and 8, when loop 32 is locked, intermediate frequency f_{IF} then has a mean value which is substantially equal to $N/M \cdot f_p$.

One advantage of such an arrangement of divider 44 is that the resolution of
10 locked loop 32 is increased. By way of example, in the event that $M = 19$, intermediate frequency f_{IF} may then be adjusted by steps of 1 kHz.



CLAIMS

1. FM receiver (29) able to receive a high frequency signal from a transmitter, said receiver including:

- an antenna (2) for receiving said high frequency signal and providing a first electric signal (S1) representative of said received signal;

5 - a high frequency stage (3) for providing a second electric signal (S2) amplified with respect to said first signal and at a frequency comprised within a frequency band centred on a carrier frequency (f_c) of said transmitter;

- an oscillator (5) for providing, in response to a control signal (S9), a third electric signal (S3);

10 - a mixer unit (30) for providing the product of said second and third signals in the form of a fourth electric signal (S6) at an intermediate frequency (f_{IF}); and

- an FM demodulation stage (8) for demodulating said fourth signal and providing the result in the form of a fifth electric signal (S7);

15 said receiver being characterized in that it further includes a locked loop arranged to enslave said intermediate frequency (f_{IF}) from a pilot frequency (f_p) present in said fifth signal (S7),

said locked loop including an automatic frequency control stage (36) for providing said control signal to said oscillator in response to said fifth signal (S7), so as to keep the intermediate frequency (f_{IF}) of said fourth signal (S6) constant.

20 2. Receiver (29) according to claim 1, characterised in that said locked loop (32) further includes:

- a phase locked loop filter (34) for providing a sixth electric signal (S8) at said pilot frequency (f_p) in response to said fifth signal (S7);

25 said automatic frequency control stage (36) providing said control signal in response to said fourth signal (S6) at said intermediate frequency (f_{IF}) and to said sixth signal (S8) at said pilot frequency (f_p), so that said intermediate frequency (f_{IF}) has a mean value enslaved to a predetermined value depending on said pilot frequency (f_p).

30 3. Receiver (29) according to claim 2, characterised in that said phase locked loop filter (34) is formed so as to have a determined bandwidth, so as to be able to provide said sixth signal (S8) at said pilot frequency (f_p) and with a high signal to noise signal.

4. Receiver (29) according to claim 2, characterised in that said automatic frequency control stage (36) includes :

35 - a first frequency divider (38) for providing, in response to said fourth signal (S6) at said intermediate frequency (f_{IF}), a seventh electric signal (S11) at a first



frequency (f_{IF}/N) equal to said intermediate frequency divided by a first integer number (N);

- a phase and frequency comparator (40) for providing, in response to said seventh signal (S11) at said first frequency (f_{IF}/N) and to said sixth signal (S8) at said pilot frequency (f_p), an eighth electric signal (S12) representative of the difference between said first frequency (f_{IF}/N) and said pilot frequency (f_p); and

- a loop filter (42) for providing, in response to said eighth signal (S12), said control signal (S9) representative of the difference between said first frequency (f_{IF}/N) and said pilot frequency (f_p), so that said intermediate frequency (f_{IF}) has a mean value enslaved to a predetermined value ($N \cdot f_p$) equal to the product of said pilot frequency (f_p) by said first integer number (N).

5. Receiver (29) according to claim 2, characterised in that said automatic frequency control stage (36) includes:

- a first frequency divider (38) for providing, in response to said fourth signal (S6) at said intermediate frequency (f_{IF}), a seventh electric signal (S11) at a first frequency (f_{IF}/N) equal to said intermediate frequency divided by a first integer number (N);

- a second frequency divider (44) for providing, in response to said sixth signal (S8) at said pilot frequency (f_p), a ninth electric signal (S13) at a second frequency (f_p/M) equal to said pilot frequency (f_p) divided by a second integer number (M);

- a phase and frequency comparator (40) for providing, in response to said seventh signal (S11) at said first frequency (f_{IF}/N) and to said ninth signal (S13) at said second frequency (f_p/M), an eighth electric signal (S12) representative of the difference between said first and second frequencies; and

- a loop filter (42) for providing, in response to said eighth signal (S12), said control signal (S9) representative of the difference between said first frequency (f_{IF}/N) and said second frequency (f_p/M), so that said intermediate frequency (f_{IF}) has a mean value enslaved to a second predetermined value ($N/M \cdot f_p$) equal to the product of said pilot frequency (f_p) and said first integer number (N) divided by said second integer number (M).

6. Receiver (29) according to claim 1, characterised in that said locked loop (32) further includes a frequency locked loop filter (31) arranged to receive said fifth signal (S7) and to provide in response a tenth electric signal (S10) to said oscillator (5), so as to reduce the deviation of said fourth signal (S6).

7. Receiver (29) according to claim 1, characterised in that said mixer unit (30) includes, connected in series, a mixer (4), an intermediate frequency filter (6) and an amplifier/limiter (7).



- 11 -

8. Receiver (29) according to claim 1, characterised in that said pilot frequency (fp) is equal to 19 kHz.