SEMICONDUCTOR DEVICE AND METHOD OF FORMING WIRE STUDS AS VERTICAL INTERCONNECT IN FO-WLP

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming wire studs as vertical interconnect in a fan-out wafer level package (Fo-WLP).

Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of

functions such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or base current or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed operations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end manufacturing, and back-end manufacturing, each involving

potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each semiconductor die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual semiconductor die from the finished wafer and packaging the die to provide structural support and environmental isolation. The term "semiconductor die" as used herein refers to both the singular and plural form of the words, and accordingly, can refer to both a single semiconductor device and multiple semiconductor devices.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller semiconductor die size can be achieved by improvements in the front-end process resulting in semiconductor die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

Semiconductor packages often use conductive pillars or vias as a vertical interconnect through encapsulant around a semiconductor die, e.g., between a topside interconnect structure and bottom side interconnect structure. A via is typically formed through the encapsulant and filled with conductive material. The formation of conductive vias is time consuming and involves expensive equipment. The conductive vias may become delaminated from the topside interconnect structure

and bottom side interconnect structure resulting in a manufacturing defect or latent defect.

Summary of the Invention

A need exists for a simple and cost effective vertical interconnect structure in a Fo-WLP. Accordingly, in one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a substrate, disposing a semiconductor die over a first surface of the substrate, attaching a wire stud to the first surface of the substrate, depositing an encapsulant over the substrate, semiconductor die, and wire stud, and forming an interconnect structure over the encapsulant and electrically connected to the wire stud.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a substrate, disposing a semiconductor die over the substrate, attaching a wire stud to the substrate, and depositing an encapsulant over the substrate, semiconductor die, and wire stud.

In another embodiment, the present invention is a semiconductor device comprising a substrate and semiconductor die disposed over the substrate. A wire stud is attached to the substrate. An encapsulant is deposited over the substrate, semiconductor die, and wire stud. An interconnect structure is formed over the encapsulant.

In another embodiment, the present invention is a semiconductor device comprising a substrate and semiconductor die disposed over the substrate. A wire stud is attached to the substrate. An encapsulant is deposited over the substrate,

semiconductor die, and wire stud.

Brief Description of the Drawings

FIG. 1 illustrates a printed circuit board (PCB) with different types of packages mounted to its surface;

FIGs. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGs. 3a-3c illustrate a semiconductor wafer with a plurality of semiconductor die separated by a saw street;

FIGs. 4a-4k illustrate a process of forming wire studs as vertical interconnect in a Fo-WLP;

FIG. 5 illustrates an opposing orientation of the semiconductor die in the Fo-WLP;

FIGs. 6a-6i illustrate another process of forming wire studs as vertical interconnect in a Fo-WLP;

FIGs. 7a-7b illustrate an PoP arrangement with the Fo-WLP having wire studs as vertical interconnect; and

FIGs. 8a-8b illustrate a SiP arrangement with the Fo-WLP having wire studs as vertical interconnect.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined

by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, and resistors, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices by dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin

film deposition can involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual semiconductor die and then packaging the semiconductor die for structural support and environmental isolation. To singulate the semiconductor die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual semiconductor die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. 1 illustrates electronic device 50 having a chip carrier substrate or printed circuit board (PCB) 52 with a plurality of semiconductor packages mounted on its surface. Electronic device 50 can have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. 1 for purposes of illustration.

Electronic device 50 can be a stand-alone system that

uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device 50 can be a subcomponent of a larger system. For example, electronic device 50 can be part of a cellular phone, personal digital assistant (PDA), digital video camera (DVC), or other electronic communication device. Alternatively, electronic device 50 can be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASIC), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components. Miniaturization and weight reduction are essential for the products to be accepted by the market. The distance between semiconductor devices must be decreased to achieve higher density.

In FIG. 1, PCB 52 provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces 54 are formed over a surface or within layers of PCB 52 using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces 54 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 54 also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may

only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including bond wire package 56 and flipchip 58, are shown on PCB 52. Additionally, several types of second level packaging, including ball grid array (BGA) 60, bump chip carrier (BCC) 62, dual in-line package (DIP) 64, land grid array (LGA) 66, multi-chip module (MCM) 68, quad flat non-leaded package (QFN) 70, and quad flat package 72, are shown mounted on PCB 52. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB 52. In some embodiments, electronic device 50 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using less expensive components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGs. 2a-2c show exemplary semiconductor packages. FIG. 2a illustrates further detail of DIP 64 mounted on PCB 52. Semiconductor die 74 includes an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit can

include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active region of semiconductor die 74. Contact pads 76 are one or more layers of conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within semiconductor die 74. During assembly of DIP 64, semiconductor die 74 is mounted to an intermediate carrier 78 using a gold-silicon eutectic layer or adhesive material such as thermal epoxy or epoxy resin. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads 80 and bond wires 82 provide electrical interconnect between semiconductor die 74 and PCB 52. Encapsulant 84 is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating semiconductor die 74 or bond wires 82.

FIG. 2b illustrates further detail of BCC 62 mounted on PCB 52. Semiconductor die 88 is mounted over carrier 90 using an underfill or epoxy-resin adhesive material 92. Bond wires 94 provide first level packaging interconnect between contact pads 96 and 98. Molding compound or encapsulant 100 is deposited over semiconductor die 88 and bond wires 94 to provide physical support and electrical isolation for the device. Contact pads 102 are formed over a surface of PCB 52 using a suitable metal deposition process such as electrolytic plating or electroless plating to prevent oxidation. Contact pads 102 are electrically connected to one or more conductive signal traces 54 in PCB 52. Bumps 104 are formed between contact pads 98 of BCC 62 and contact pads 102 of PCB 52.

In FIG. 2c, semiconductor die 58 is mounted face down to intermediate carrier 106 with a flipchip style first level

packaging. Active region 108 of semiconductor die 58 contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active region 108. Semiconductor die 58 is electrically and mechanically connected to carrier 106 through bumps 110.

BGA 60 is electrically and mechanically connected to PCB 52 with a BGA style second level packaging using bumps 112. Semiconductor die 58 is electrically connected to conductive signal traces 54 in PCB 52 through bumps 110, signal lines 114, and bumps 112. A molding compound or encapsulant 116 is deposited over semiconductor die 58 and carrier 106 to provide physical support and electrical isolation for the device. The flipchip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die 58 can be mechanically and electrically connected directly to PCB 52 using flipchip style first level packaging without intermediate carrier 106.

FIG. 3a shows a semiconductor wafer 120 with a base substrate material 122, such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support. A plurality of semiconductor die or components 124 is formed on wafer 120 separated by a non-active, inter-die wafer area or saw street 126 as described above. Saw street 126 provides cutting areas to singulate semiconductor wafer 120 into individual semiconductor die 124.

FIG. 3b shows a cross-sectional view of a portion of semiconductor wafer 120. Each semiconductor die 124 has a back surface 128 and active surface 130 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 130 to implement analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die 124 may also contain integrated passive devices (IPDs), such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 124 is a ball grid array (BGA) type device.

An electrically conductive layer 132 is formed over active surface 130 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 132 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 132 operates as contact pads electrically connected to the circuits on active surface 130. Conductive layer 132 can be formed as contact pads disposed side-by-side a first distance from the edge of semiconductor die 124, as shown in FIG. 3b. Alternatively, conductive layer 132 can be formed as contact pads that are offset in multiple rows such that a first row of contact pads is disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row is disposed a second distance from the edge of the die.

In FIG. 3c, semiconductor wafer 120 is singulated

through saw street 126 using a saw blade or laser cutting tool 134 into individual semiconductor die 124.

FIGs. 4a-4k illustrate, in relation to FIGs. 1 and 2a-2c, a process of forming wire studs as a vertical interconnect between a substrate and build-up interconnect structure in a Fo-WLP. FIG. 4a shows an interposer substrate 140 including one or more laminated layers of polytetrafluoroethylene pre-impregnated (prepreg), FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, substrate 140 contains one or more insulating or dielectric layers 142.

A plurality of vias is formed through substrate 140 using laser drilling, mechanical drilling, or deep reactive ion etching (DRIE). The vias are filled with Al, Cu, Sn, Ni, Au, Ag, titanium (Ti), tungsten (W), or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 144.

An electrically conductive layer or redistribution layer (RDL) 146 is formed over a first surface of substrate 140 and conductive vias 144 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 146 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 146 is electrically connected to conductive vias 144.

An electrically conductive layer or RDL 148 is formed over a second surface of substrate 140 opposite the first surface and conductive vias 144 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering,

electrolytic plating and electroless plating. Conductive layer 148 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 148 is electrically connected to conductive vias 144 and conductive layer 146. In another embodiment, conductive vias 144 are formed through substrate 140 after forming conductive layer 146 and/or conductive layer 148.

The resulting interposer substrate 140 provides electrical interconnect vertically and laterally across the substrate through conductive layers 146 and 148 and conductive vias 144 according to the electrical function of semiconductor die 124. Portions of conductive layers 146 and 148 and conductive vias 144 are electrically common or electrically isolated according to the design and function of semiconductor die 124.

Substrate 140 can also be a multi-layer flexible laminate, ceramic, copper foil, glass, or semiconductor wafer including an active surface containing one or more transistors, diodes, and other circuit elements to implement analog circuits or digital circuits.

In FIG. 4b, semiconductor die 124 from FIG. 3c is mounted to interposer substrate 140 using, for example, a pick and place operation with active surface 130 oriented toward the substrate. Semiconductor die 124 are secured to substrate 140 with a die attach adhesive, such as epoxy resin. Conductive layer 132 of semiconductor die 124 is electrically connected to conductive layer 146 of substrate 140. FIG. 4c shows semiconductor die 124 mounted to substrate 140.

In FIG. 4d, a plurality of wire studs 150 is attached to substrate 140 by compression bonding, stitch bonding, or ball bonding in a form free air ball (FAB) or loop profile. Wire

studs 150 compress upon contact with conductive layer 146 shown as base portion 150a. Stem 150b can be cut to the proper length, e.g., 250-500 micrometers (μm). Wire studs 150 provide a z-direction vertical interconnect structure.

FIG. 4e shows a carrier or temporary substrate 160 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 162 is formed over carrier 160 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. The substrate, semiconductor die, and wire studs assembly from FIG. 4d is inverted and mounted to carrier 160 and interface layer 162. Wire studs 150 can be the same height as semiconductor die 124 or a lesser height than the semiconductor die to avoid bending the wire studs during mounting to carrier 160. Wire studs 150 can also be a greater height than semiconductor die 124. Wire studs 150 have sufficient diameter to remain rigid and stable during subsequent manufacturing processes.

In FIG. 4f, an encapsulant or molding compound 164 is deposited over carrier 160 and around substrate 140, semiconductor die 124, and wire studs 150 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 164 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 164 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 4g, carrier 160 and interface layer 162 are removed by chemical etching, mechanical peeling, chemical

mechanical planarization (CMP), mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping. The substrate, semiconductor die, and wire studs assembly is inverted.

A portion of encapsulant 164 is removed by shallow depth laser direct ablation (LDA) using laser 166 to expose stem 150b of wire studs 150. Alternatively, a portion of encapsulant 164 is removed by an etching process through a patterned photoresist layer to expose wire studs 150. The exposure of wire studs 150 may not be necessary if the wire studs are already exposed by nature of being the same height or greater height as semiconductor die 124.

In FIG. 4h, a build-up interconnect structure 170 is formed over encapsulant 164 and semiconductor die 124. The build-up interconnect structure 170 includes an electrically conductive layer or RDL 172 formed using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 172 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer 172 extends into the removed portion of encapsulant 164 that exposes wire studs 150 to electrically connect to the wire studs. Other portions of conductive layer 172 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

The build-up interconnect structure 170 further includes an insulating or passivation layer 174 formed over encapsulant 164 and semiconductor die 124 and around conductive layer 172 for electrical isolation using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer 174 contains one or more layers of silicon

dioxide (SiO_2), silicon nitride (Si_3N_4), silicon oxynitride (SiON), tantalum pentoxide (Ta_2O_5), aluminum oxide (Al_2O_3), or other material having similar insulating and structural properties.

In FIG. 4i, a portion of encapsulant 164 opposite interconnect structure 170 undergoes a grinding operation with grinder 178 to planarize the surface and reduce a thickness of the encapsulant. A chemical etch or CMP process can also be used to remove mechanical damage resulting from the grinding operation and planarize encapsulant 164. The reduced thickness of encapsulant 164 remains covering substrate 140 to protect conductive layer 148.

In FIG. 4j, a portion of encapsulant 164 is removed by shallow depth LDA using laser 180 to expose conductive layer 148 of substrate 140 for electrical interconnect to other semiconductor devices, as discussed in FIGs. 7a-7b and 8a-8b.

In FIG. 4k, an electrically conductive bump material is deposited over conductive layer 172 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, lead (Pb), Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 172 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 182. In some applications, bumps 182 are reflowed a second time to improve electrical contact to conductive layer 172. In one embodiment, bumps 182 are formed over a UBM having a wetting layer, barrier layer, and adhesive layer. The bumps can also be compression bonded or

thermocompression bonded to conductive layer 172. Bumps 182 represent one type of interconnect structure that can be formed over conductive layer 172. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Fo-WLP 184 uses wire studs 150 for vertical electrical interconnect between substrate 140 and build-up interconnect structure 170. Wire studs 150 simplify the manufacturing process to reduce cost and reduce delamination issues with the vertical interconnect structure in the Fo-WLP.

FIG. 5 shows an embodiment with semiconductor die 124 mounted back surface 128 to interposer substrate 140. If necessary, a portion of encapsulant 164 is removed by LDA to expose conductive layer 132, similar to FIG. 4g. A portion of conductive layer 172 extends into the removed portion of encapsulant 164 that exposes conductive layer 132 of semiconductor die 124 to electrically connect to the semiconductor die, similar to FIG. 4h.

FIGs. 6a-6i illustrate, in relation to FIGs. 1 and 2a-2c, another process of forming wire studs as a vertical interconnect between a substrate and build-up interconnect structure in a Fo-WLP. FIG. 6a shows an interposer substrate 190 including one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, substrate 190 contains one or more insulating or dielectric layers 192.

A plurality of vias is formed through substrate 190 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable

electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 194.

An electrically conductive layer or RDL 196 is formed over a first surface of substrate 190 and conductive vias 194 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 196 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 196 is electrically connected to conductive vias 194.

An electrically conductive layer or RDL 198 is formed over a second surface of substrate 190 opposite the first surface and conductive vias 194 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating and electroless plating. Conductive layer 198 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 198 is electrically connected to conductive vias 194 and conductive layer 196. In another embodiment, conductive vias 194 are formed through substrate 190 after forming conductive layer 196 and/or conductive layer 198.

An electrically conductive layer 200 is formed over conductive layer 198 outside the mounting site of semiconductor die 124 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating and electroless plating. Conductive layer 200 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 200 operates as a bonding pad electrically connected to conductive layer 198 and

conductive vias 194.

The resulting interposer substrate 190 provides electrical interconnect vertically and laterally across the substrate through conductive layers 196 and 198 and conductive vias 194 according to the electrical function of semiconductor die 124. Portions of conductive layers 196 and 198 and conductive vias 194 are electrically common or electrically isolated according to the design and function of semiconductor die 124.

Substrate 190 can also be a multi-layer flexible laminate, ceramic, copper foil, glass, or semiconductor wafer including an active surface containing one or more transistors, diodes, and other circuit elements to implement analog circuits or digital circuits.

Semiconductor die 124 from FIG. 3c is mounted to interposer substrate 190 using, for example, a pick and place operation with back surface 128 oriented toward the substrate. Semiconductor die 124 are secured to substrate 190 with a die attach adhesive, such as epoxy resin. FIG. 6b shows semiconductor die 124 mounted to substrate 190.

In FIG. 6c, a plurality of wire studs 202 are attached to substrate 190 by compression bonding, stitch bonding, or ball bonding in a form FAB or loop profile. Wire studs 202 compress upon contact with conductive layer 196 shown as base portion 202a. Stem 202b can be cut to the proper length, e.g., 250-500 μm. Wire studs 202 provide a z-direction vertical interconnect structure.

FIG. 6d shows a carrier or temporary substrate 210 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-

sided tape 212 is formed over carrier 210 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. The substrate, semiconductor die, and wire studs assembly from FIG. 6c is inverted and mounted to carrier 210 and interface layer 212. Wire studs 202 can be the same height as semiconductor die 124 or a lesser height than the semiconductor die to avoid bending the wire studs during mounting to carrier 190. Wire studs 202 can also be a greater height than semiconductor die 124. Wire studs 202 have sufficient diameter to remain rigid and stable during subsequent manufacturing processes.

In FIG. 6e, an encapsulant or molding compound 214 is deposited over carrier 210 and around substrate 190, semiconductor die 124, and wire studs 202 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 214 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 214 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 6f, carrier 210 and interface layer 212 are removed by chemical etching, mechanical peeling, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping. The substrate, semiconductor die, and wire studs assembly is inverted.

A portion of encapsulant 214 is removed by shallow depth LDA using laser 216 to expose stem 202b of wire studs 202. Alternatively, a portion of encapsulant 214 is removed by an etching process through a patterned photoresist layer to expose wire studs 202. The exposure of wire studs 202 may not be

necessary if the wire studs are already exposed by nature of being the same height or greater height as semiconductor die 124. If necessary, a portion of encapsulant 164 is also removed by shallow depth LDA using laser 216 to expose conductive layer 132 of semiconductor die 124.

In FIG. 6g, a build-up interconnect structure 220 is formed over encapsulant 214 and semiconductor die 124. The build-up interconnect structure 220 includes an electrically conductive layer or RDL 222 formed using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 222 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer 222 extends into the removed portion of encapsulant 214 that exposes wire studs 202 to electrically connect to the wire studs. Another portion of conductive layer 222 is electrically connected to conductive layer 132 of semiconductor die 124. Other portions of conductive layer 222 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

The build-up interconnect structure 220 further includes an insulating or passivation layer 224 formed over encapsulant 214 and semiconductor die 124 and around conductive layer 222 for electrical isolation using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer 224 contains one or more layers of SiO_2, Si_3N_4, SiON, Ta_2O_5, Al_2O_3, or other material having similar insulating and structural properties.

In FIG. 6h, a portion of encapsulant 214 opposite interconnect structure 220 undergoes a grinding operation with grinder 228 to planarize the surface and reduce a thickness of

the encapsulant and expose conductive layer 200. A chemical etch or CMP process can also be used to remove mechanical damage resulting from the grinding operation and planarize encapsulant 214. The reduced thickness of encapsulant 214 remains covering substrate 190 to protect conductive layer 198.

In FIG. 6i, an electrically conductive bump material is deposited over conductive layer 222 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 222 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 230. In some applications, bumps 230 are reflowed a second time to improve electrical contact to conductive layer 222. In one embodiment, bumps 230 are formed over a UBM having a wetting layer, barrier layer, and adhesive layer. The bumps can also be compression bonded or thermocompression bonded to conductive layer 222. Bumps 230 represent one type of interconnect structure that can be formed over conductive layer 222. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Fo-WLP 232 uses wire studs 202 for vertical electrical interconnect between substrate 190 and build-up interconnect structure 220. Wire studs 202 simplify the manufacturing process to reduce cost and reduce delamination issues with the vertical interconnect structure in the Fo-WLP

FIGs. 7a-7b show an embodiment for stacking

semiconductor packages in a package-on-package (PoP) arrangement. In FIG. 7a, semiconductor package 240 includes semiconductor die or component 242 with back surface 244 and active surface 246 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 246 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die 242 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 242 is a BGA or land grid array (LGA) type device.

Semiconductor die 242 is mounted to substrate 250, which includes conductive traces 252. A plurality of bond wires 254 is connected between contact pads 256 formed on active surface 246 of semiconductor die 242 and conductive traces 252 of substrate 250. An encapsulant 258 is deposited over semiconductor die 242, substrate 250, and bond wires 254. Bumps 260 are formed over conductive traces 252 of substrate 250 opposite semiconductor die 242.

FIG. 7b shows semiconductor package 240 mounted to Fo-WLP 184 from FIG. 4k with bumps 260 bonded to conductive layer 148 of substrate 140 as PoP 262.

FIGs. 8a-8b show another embodiment for stacking semiconductor packages in a PoP or system-in-package (SiP) arrangement. In FIG. 8a, semiconductor package 270 includes semiconductor die or component 272 with back surface 274 and active surface 276 containing analog or digital circuits

implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 276 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die 272 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 272 is a BGA or LGA type device.

Semiconductor die 272 is mounted to substrate 280, which includes conductive traces 282. A plurality of bond wires 284 is connected between contact pads 286 formed on active surface 276 of semiconductor die 272 and conductive traces 282 of substrate 280. An encapsulant 288 is deposited over semiconductor die 272, substrate 280, and bond wires 284. Bumps 290 are formed over conductive traces 282 of substrate 280 opposite semiconductor die 272.

FIG. 8b shows semiconductor package 270 mounted to Fo-WLP 184 from FIG. 4k with bumps 290 bonded to conductive layer 148 as SiP 292. In addition, discrete semiconductor devices 294 are disposed over encapsulant 164 and electrically connected to conductive layer 148 of substrate 140 with conductive paste 298. Discrete semiconductor devices 294 can be passive components, such as inductors, capacitors, or resistors. Discrete semiconductor devices 294 can also be active components, such as transistors or diodes.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a substrate;

disposing a semiconductor die over a first surface of the substrate;

attaching a wire stud to the first surface of the substrate;

depositing an encapsulant over the substrate, semiconductor die, and wire stud; and

forming an interconnect structure over the encapsulant and electrically connected to the wire stud.

2. The method of claim 1, further including removing a portion of the encapsulant to expose the wire stud.

3. The method of claim 1, further including removing a portion of the encapsulant by laser direct ablation.

4. The method of claim 1, further including forming a bonding pad over a second surface of the substrate opposite the first surface of the substrate.

5. A method of making a semiconductor device, comprising:

providing a substrate;

disposing a semiconductor die over the substrate;

attaching a wire stud to the substrate; and

depositing an encapsulant over the substrate, semiconductor die, and wire stud.

6. The method of claim 5, further including forming an interconnect structure over the encapsulant and electrically connected to the wire stud.

7. The method of claim 5, further including removing a portion of the encapsulant to expose the wire stud.

8. The method of claim 5, further including removing a portion of the encapsulant to expose the substrate.

9. The method of claim 5, further including forming a bonding pad over a surface of the substrate opposite the wire stud.

10. A semiconductor device, comprising:

a substrate;

a semiconductor die disposed over the substrate;

a wire stud attached to the substrate; and

an encapsulant deposited over the substrate, semiconductor die, and wire stud.

11. The semiconductor device of claim 10, further including an interconnect structure formed over the encapsulant.

12. The semiconductor device of claim 11, wherein the interconnect structure is electrically coupled to the wire stud.

13. The semiconductor device of claim 11, wherein the interconnect structure is electrically coupled to the semiconductor die.

14. The semiconductor device of claim 10, further including a bonding pad formed over a surface of the substrate opposite the wire stud.

15. The semiconductor device of claim 10, further including a semiconductor package disposed over the semiconductor die and electrically connected to the substrate.