

Abstract of Disclosure

CIRCUIT LAYOUT STRUCTURE

A circuit layout structure includes a wafer having at least a cell region and a scribe line region defined thereon, a metal pattern formed in a first insulating layer in the scribe line region, a second insulating layer and a hard mask layer formed on the metal pattern and the first insulating layer, and at least a dummy pattern formed in the second insulating layer and the hard mask layer in the scribe line region. The dummy pattern has a transmission rate between 0% and 1%.

Figure 4