CLAIMS

1. A method comprising:

obtaining a first carrier bonded to an upper surface of a silicon wafer, wherein one or more through silicon vias are extended through the silicon wafer and a passivation stack, wherein the passivation stack is disposed below a bottom surface of the silicon wafer, wherein a portion of each of the one or more through silicon vias is exposed through an opening of one or more openings in the passivation stack, wherein each exposed portion is coupled to one or more electrical contacts or one or more electrical contacts are disposed on the one or more openings in the passivation stack;

de-bonding the first carrier from the upper surface of the silicon wafer; and

dicing the silicon wafer into subsections comprising dies, such that each die comprises a portion of the upper surface of the silicon wafer, the portion of the upper surface of the silicon wafer comprising an active surface, at least one through silicon via of the one or more through silicon vias, and at least one electrical contact of the one or more electrical contacts on a second surface of the die, the second surface of the die parallel to the active surface; and

wherein the one or more electrical contacts comprise one or more pillar bumps.

2. The method of claim 1, further comprising:

forming fan-out regions, the forming comprising:

coupling the active surfaces of the dies to a fan-out carrier, the coupling creating a first space adjacent to a first edge of each active surface of each die and a second space adjacent to a second edge of each active surface of each die;

forming a molding layer by depositing mold on the second surfaces of the dies and in each first space and each second space to form the molding layer over the fan-out carrier; and

polishing a top surface of the molding layer such that the at least one electrical contact of the one or more electrical contacts on the second surface of each die and the polished top surface of the molding layer form a contiguous surface.

3. The method of claim 2, wherein the contiguous surface comprises flat electrical contacts of equal height and thickness.

4. The method of claim 2, further comprising:

forming a metallization layer by coating metal on the contiguous surface in a pattern.

5. The method of claim 4, wherein the metallization layer comprises a fan-out redistribution layer based on the pattern distributing additional electrical contacts at locations different from locations of the at least one electrical contact of the one or more electrical contacts on the second surface of each die.

6. The method of claim 4, wherein the metallization layer comprises an under bump layer, based on the pattern distributing additional electrical contacts at locations of the at least one electrical contact of the one or more electrical contacts on the second surface of each die.

7. The method of claim 4, wherein coating the metal on the contiguous surface comprises:

utilizing a photolithography technique to create the pattern;

electroplating the pattern, wherein the electroplating comprises depositing on the one or more openings, wherein the one or more openings comprise photoresist; and

stripping away the photoresist to reveal the metallization layer.

8. The method of claim 2, further comprising:

forming a new passivation layer on the contiguous surface to planarize the contiguous surface;

forming openings in the new passivation layer to expose the at least one electrical contact of the one or more electrical contacts on the second surface of each die; and

forming a metallization layer by coating metal on the new passivation layer in a pattern.

9. The method of claim 4, further comprising:

depositing an electrical short prevention passivation layer on the metallization layer; and

utilizing photolithography to open the electrical short prevention passivation layer at one or more locations to from electrical connection pads to the metallization layer.

10. The method of claim 9, further comprising, releasing the fan-out carrier to expose an active device surface comprising the active surfaces of the dies and surfaces of the first spaces and the second spaces contiguous with the active surfaces, the releasing comprising:

attaching a second carrier to the electrical short prevention passivation layer with an adhesive material; and

de-coupling the fan-out carrier from the active surfaces of the dies utilizing a technique selected from the group consisting of: applying mechanical pressure, heating the fan-out carrier, and applying a solvent.

11. The method of claim 10, wherein the second carrier is comprised of a material selected from the group consisting of: glass, silicon, metal, polyethylene terephthalate, and tape.

12. The method of claim 10, further comprising:

preparing the active device surface to act as a sensor.

13. The method of claim 12, wherein the preparing comprises:

washing the active device surface; and

processing the active device surface utilizing a technique selected from the group consisting of: spin coating the active device surface with a chemical solution, applying

the chemical solution by sol-gel, spraying the active device surface with the chemical solution mechanically polishing the active device surface, and baking the active device surface.

14. The method of claim 12, further comprising:

forming a fluidic flow channel over the active device surface, comprising:

attaching one or more lids to a portion of the mold to form the fluidic flow channel between the active device surface and the one or more lids; and

removing the second carrier from the electrical short prevention passivation layer to create a resultant structure.

15. The method of claim 14, further comprising:

dicing the resultant structure into sub-structures, wherein each substructure comprises at least one die and at least one lid.

16. The method of claim 1, wherein the passivation stack comprises a metallization layer.

17. The method of claim 16, wherein the metallization layer comprises a redistribution layer.

18. The method of claim 1, wherein the fabricating is accomplished utilizing a technique selected from the group consisting of: an electroplating technique and a sputtering technique.

19. The method of any of claims 1 – 18, wherein the first carrier comprises a glass carrier, and wherein the carrier is bonded to the active surface with a bonding agent selected from the group consisting of: epoxy, resin, and adhesive.

20. The method of any of claims 1 – 18, wherein the silicon wafer comprises a complementary metal–oxide–semiconductor.

21. The method of any of claims 1 – 18, further comprising:

prior to dicing the silicon wafer into subsections, placing the silicon wafer on a second carrier, such that the second carrier is coupled to the passivation stack;

prior to forming fan-out regions, releasing the second carrier from the silicon wafer.

22. The method of claim 21, wherein the second carrier comprises a tape, and wherein the releasing comprises applying an element selected from the group consisting of: thermal energy and ultra violet radiation.

23. The method of any of claims 2 – 18, wherein coupling the active surfaces of the dies to the fan-out carrier comprises forming a temporary bonding layer between the active surfaces and the fan-out carrier, wherein the temporary bonding layer protects the active surfaces during the forming of the fan-out regions.

24. The method of any of claims 2 – 15, wherein the molding layer is deposited to reach a height greater than a height of the at least one electrical contact on the second surface of each die.

25. The method of any of claims 1 – 18, wherein each die comprises a light detection device.

26. The method of claim 2 – 15, wherein forming the molding layer further comprises curing the mold to attain mechanical stability.

27. The method of claim 26, wherein the curing is at a temperature of one hundred degrees Celsius to one hundred and eighty degrees Celsius.

28. The method of claim 26, wherein the curing is for thirty minutes to three hundred minutes.

29. The method of claim 8, wherein the electrical short prevention passivation layer comprises a material selected from the group consisting of: a polyamide, an epoxy and a solder mask.