

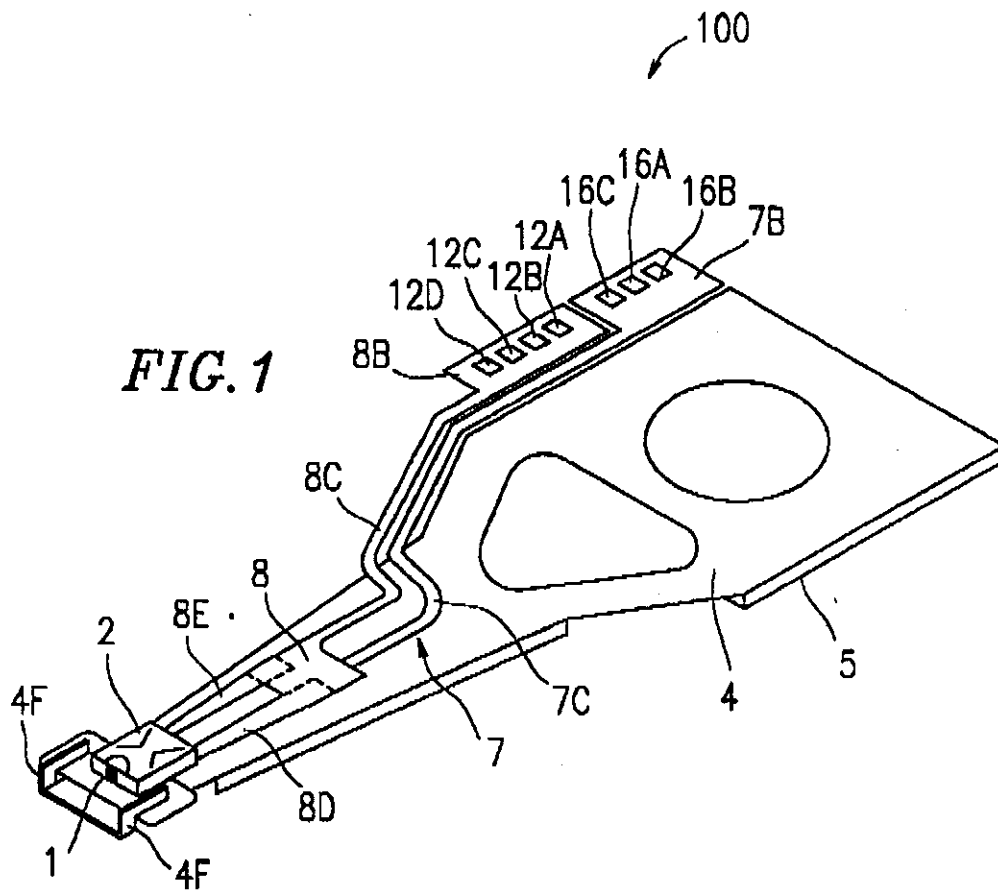


FIG. 2

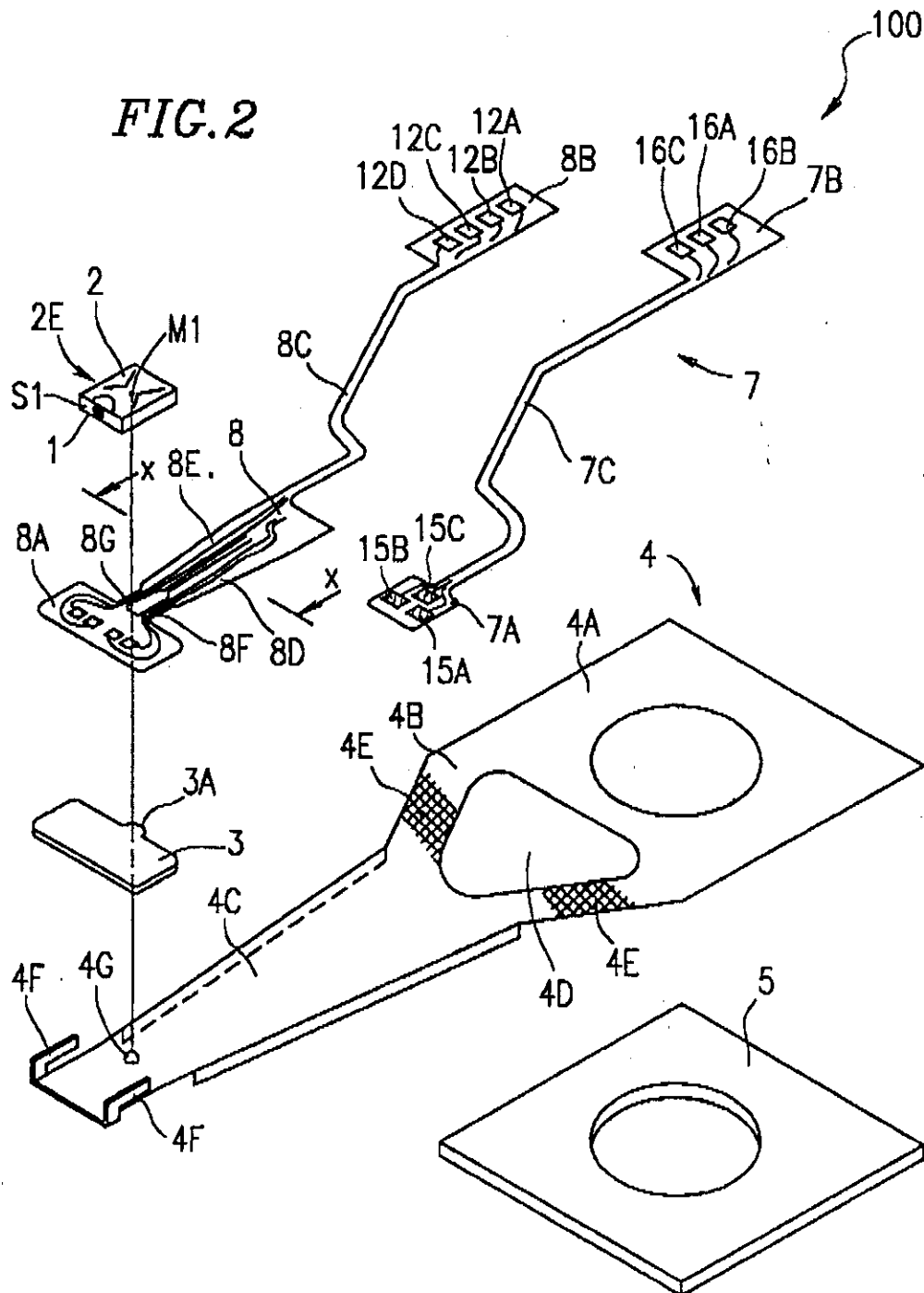


FIG. 3

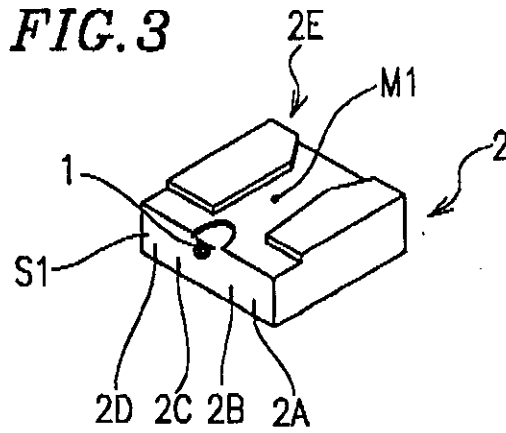


FIG. 4

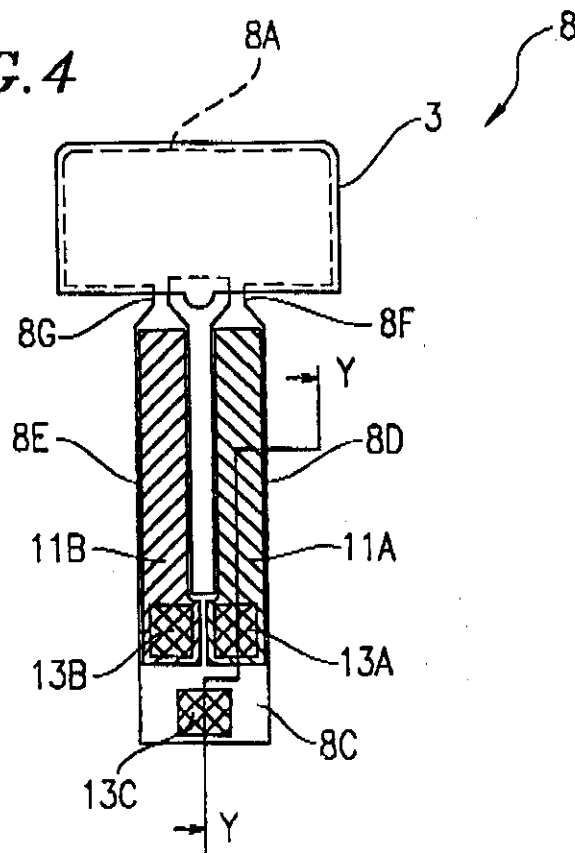


FIG. 5

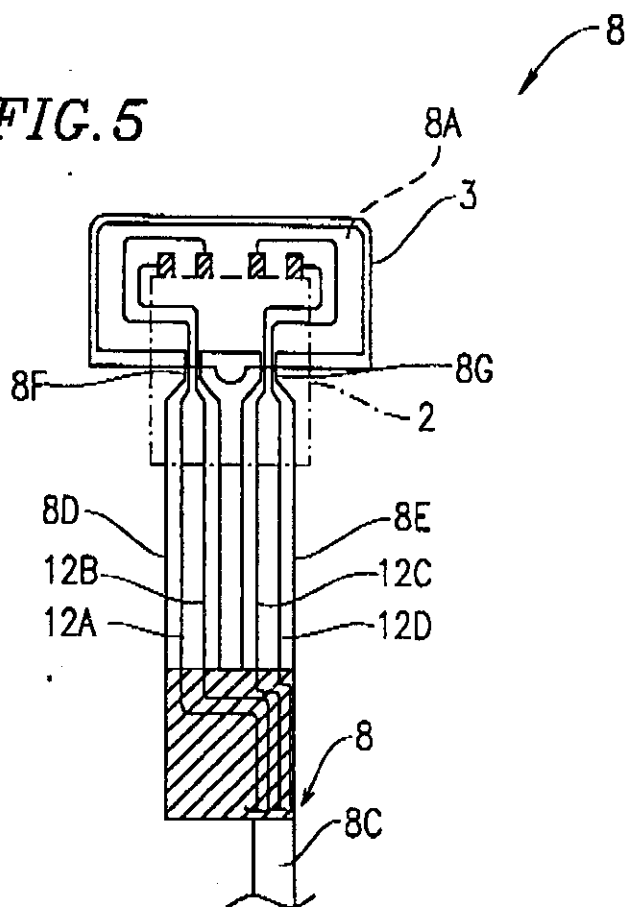
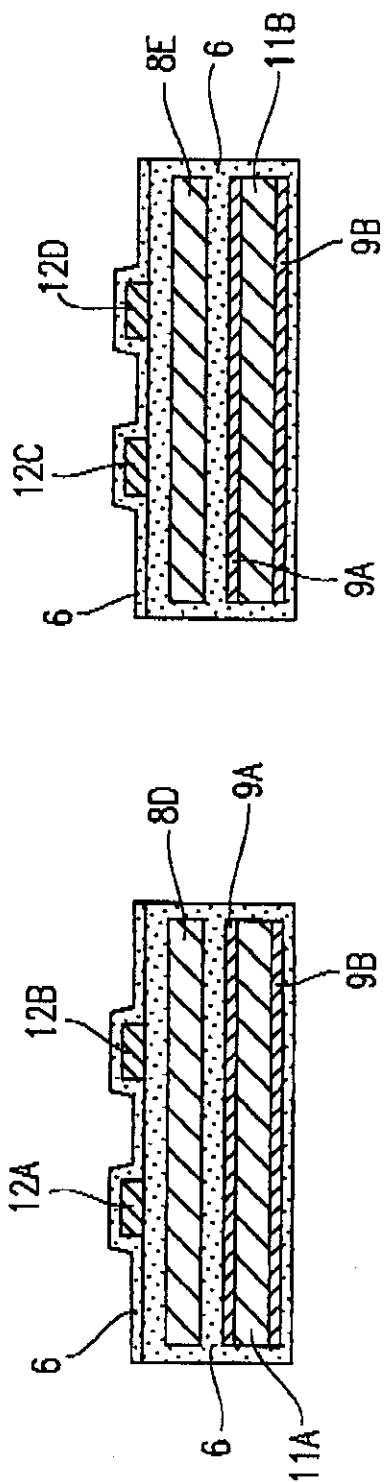
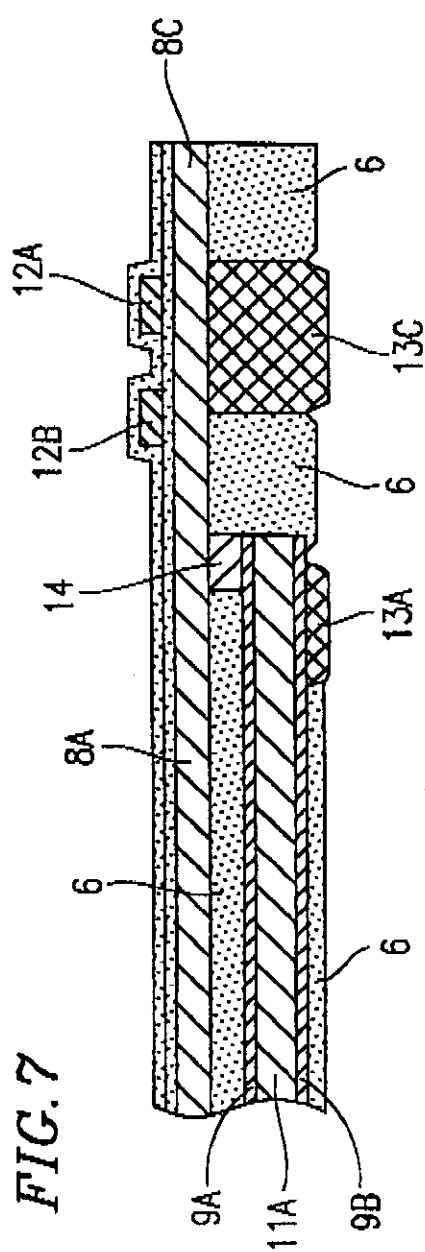
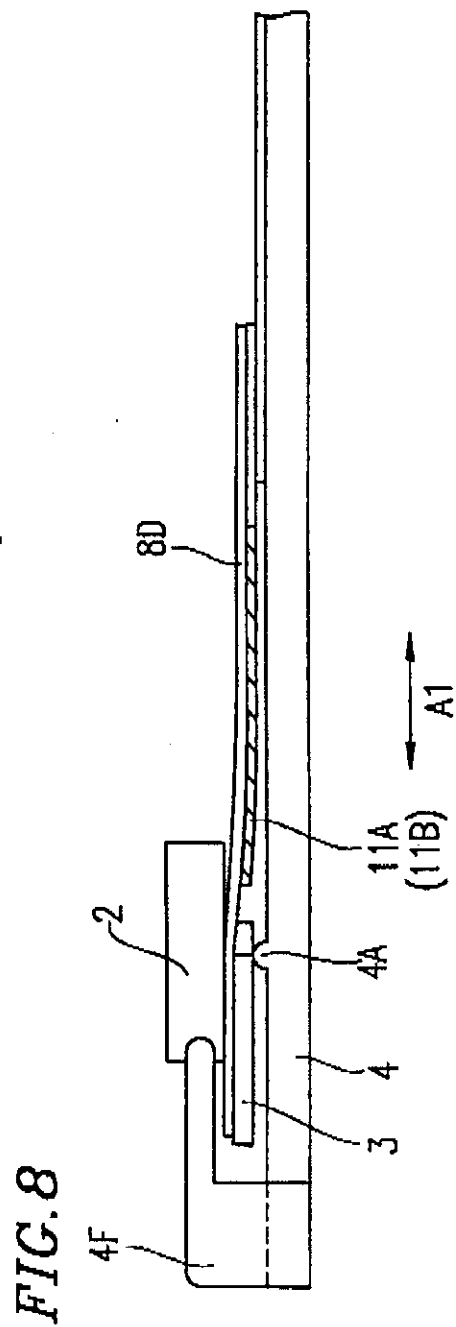
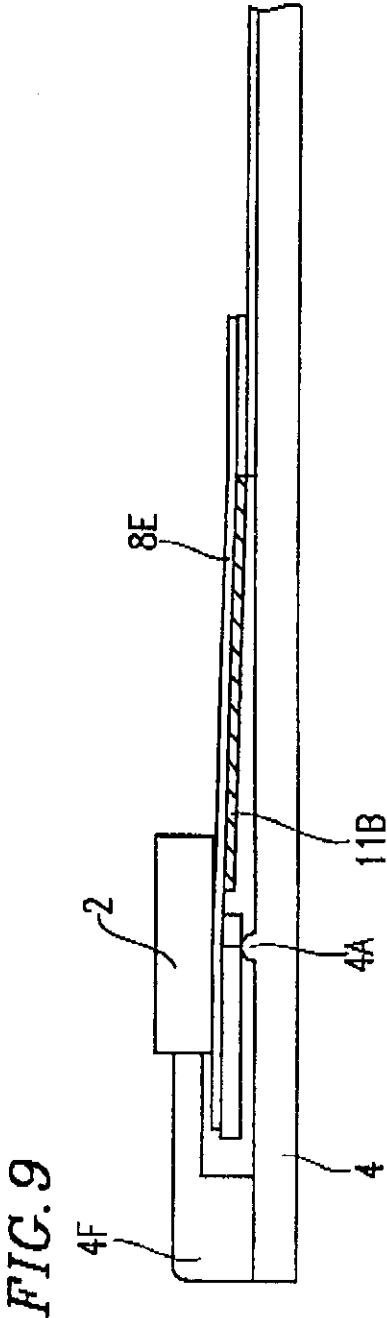


FIG. 6









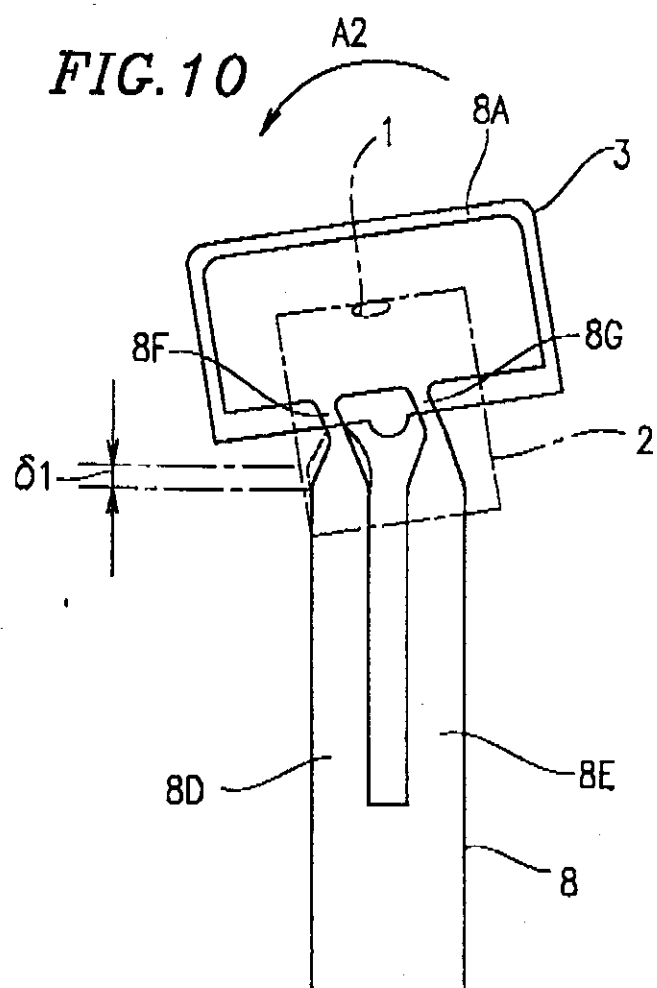


FIG. 11

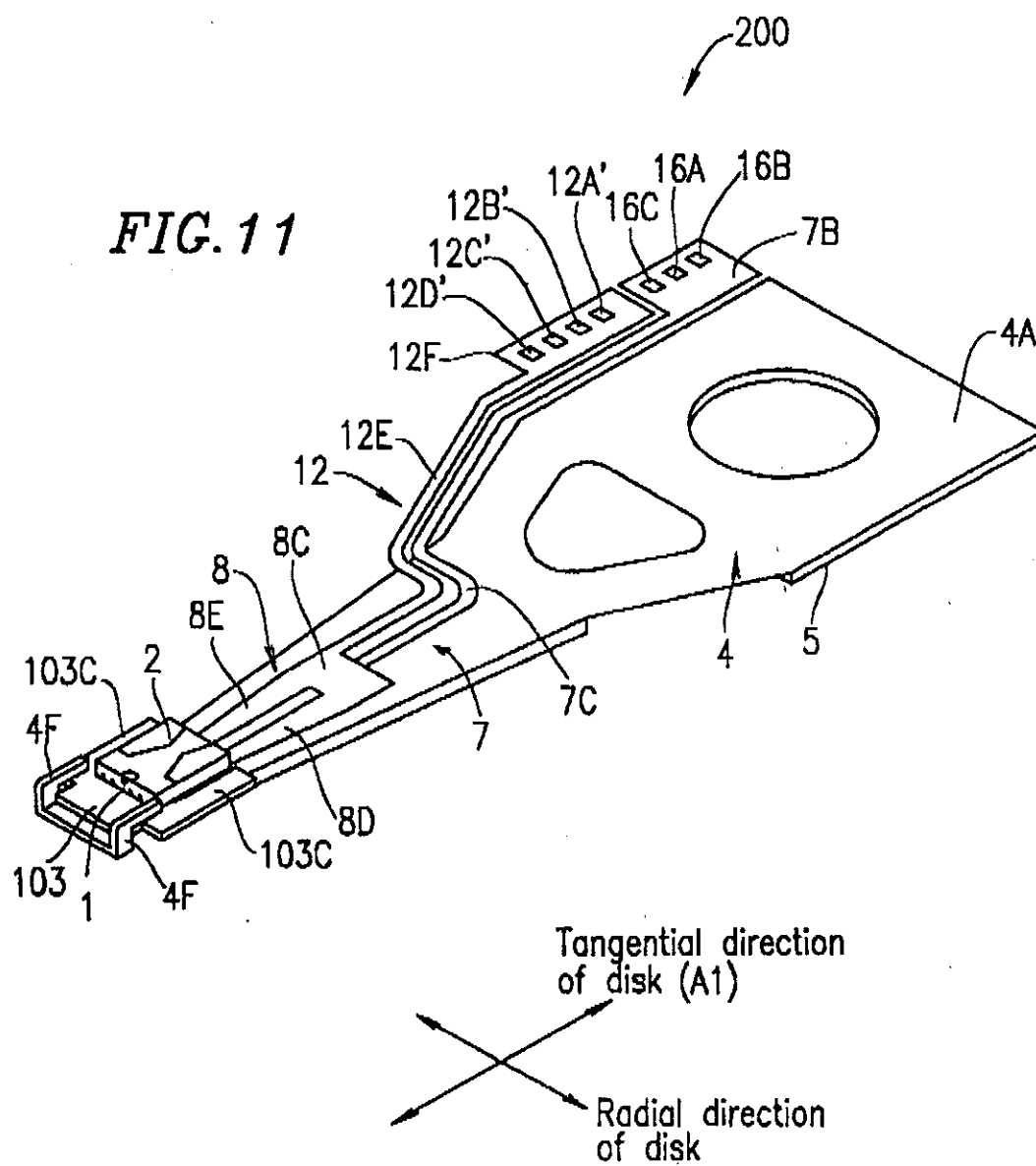
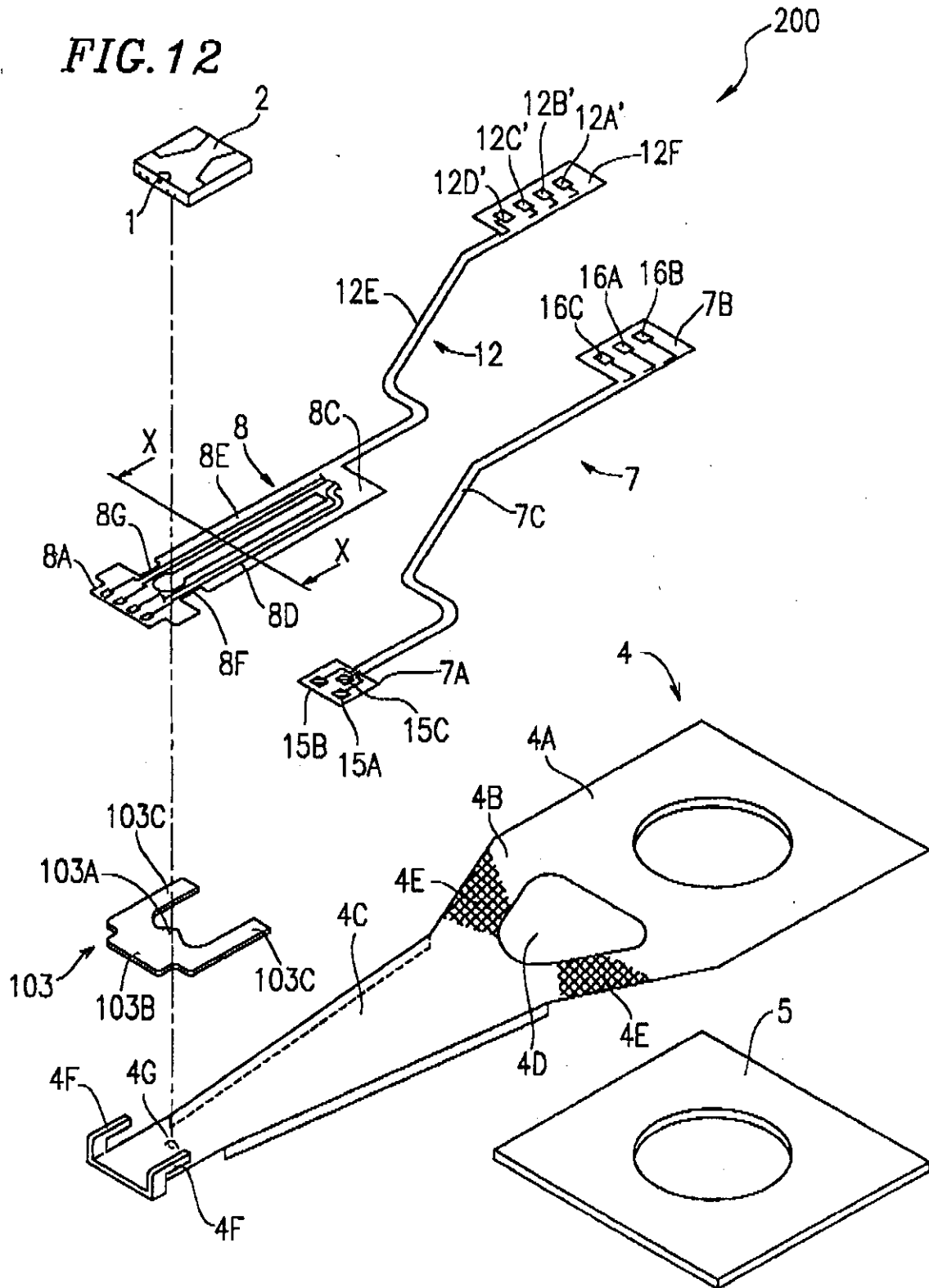


FIG. 12



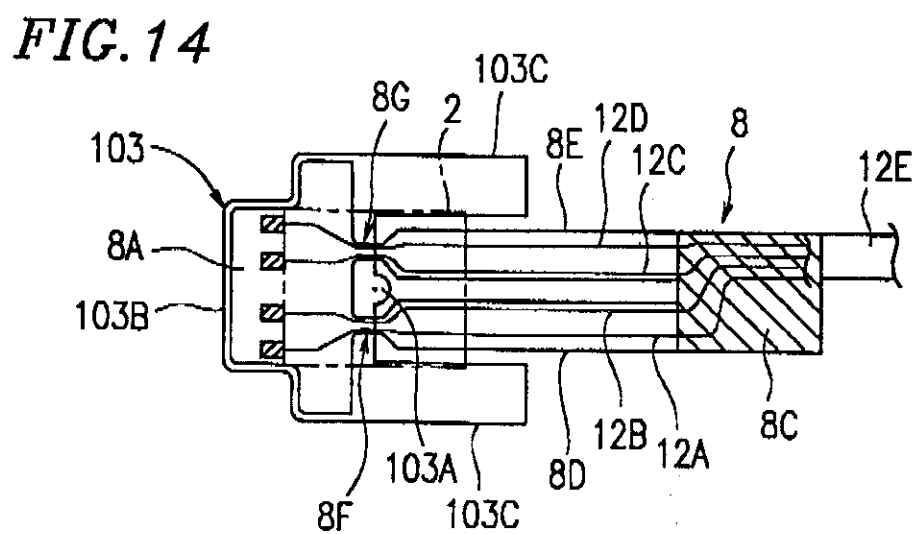
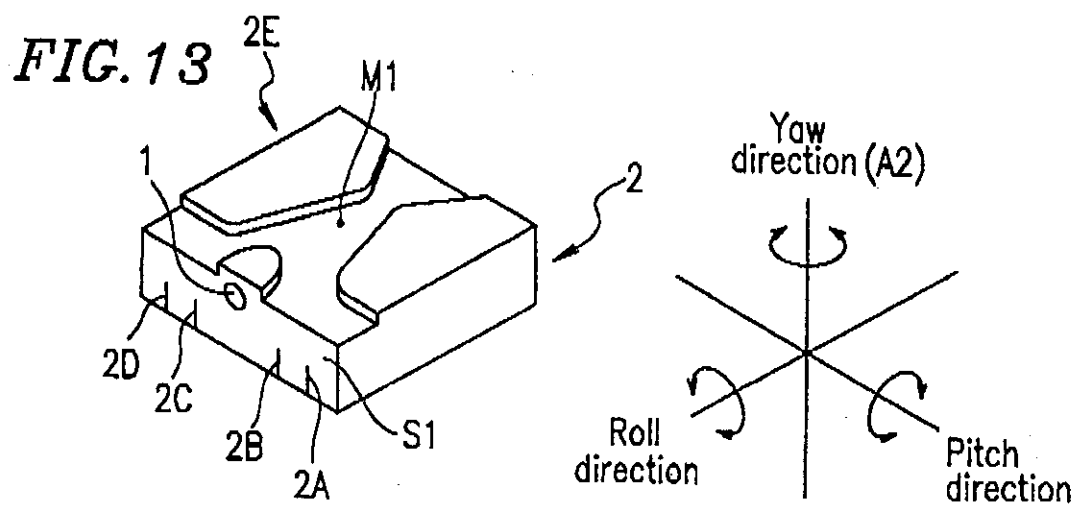


FIG. 15

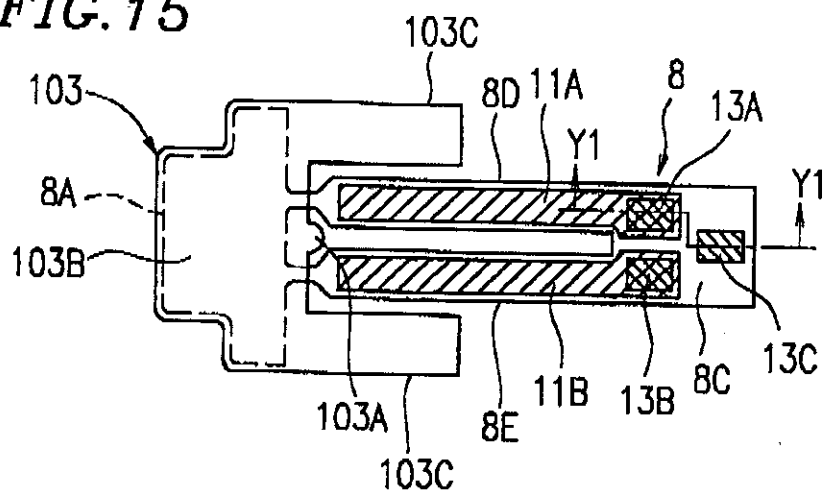


FIG. 16

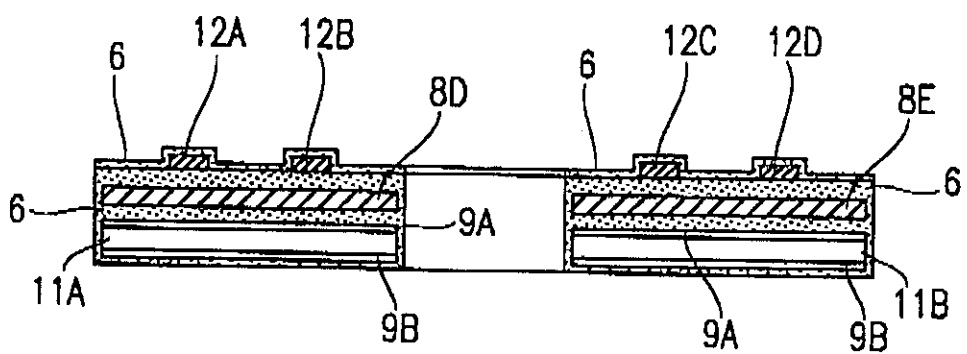


FIG. 17

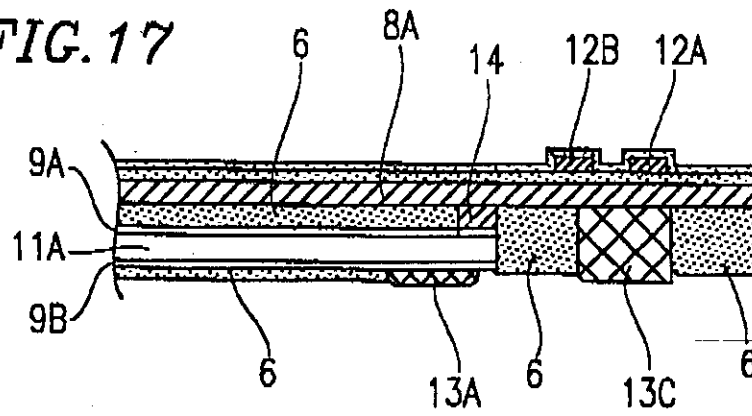


FIG. 18

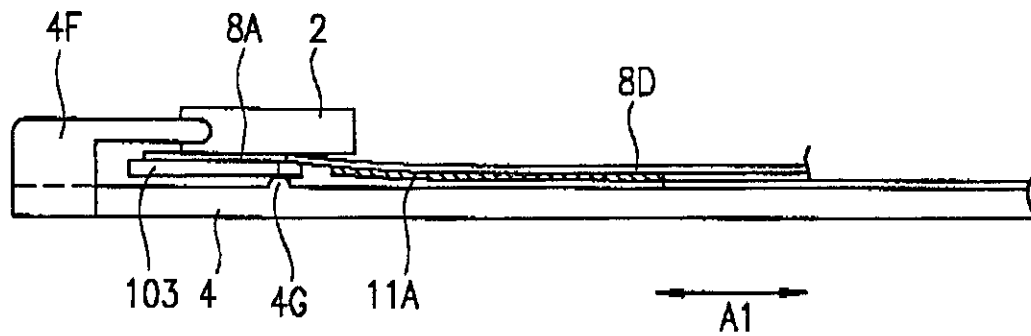
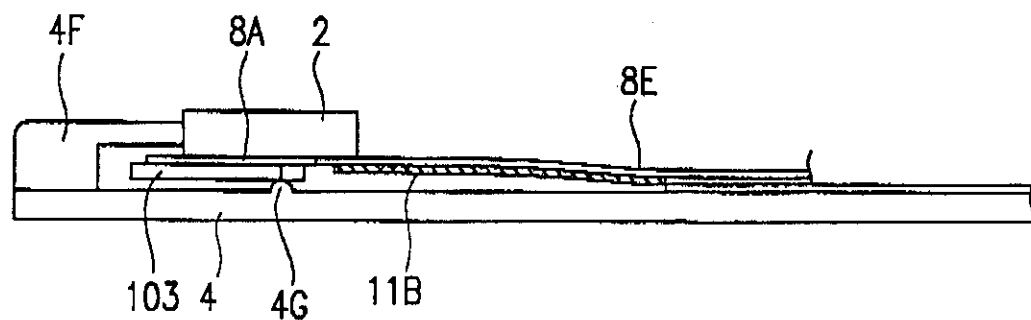


FIG. 19



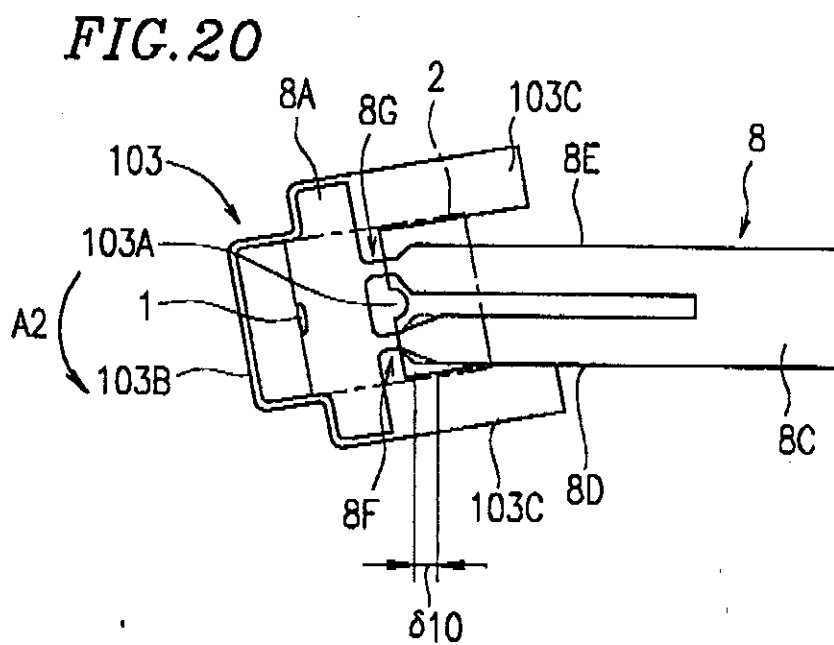


FIG. 22A

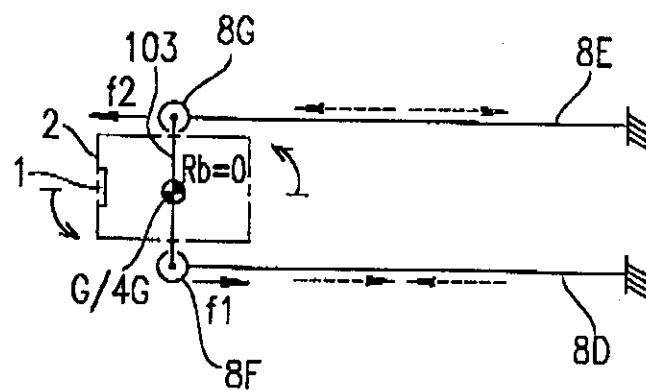


FIG. 22B

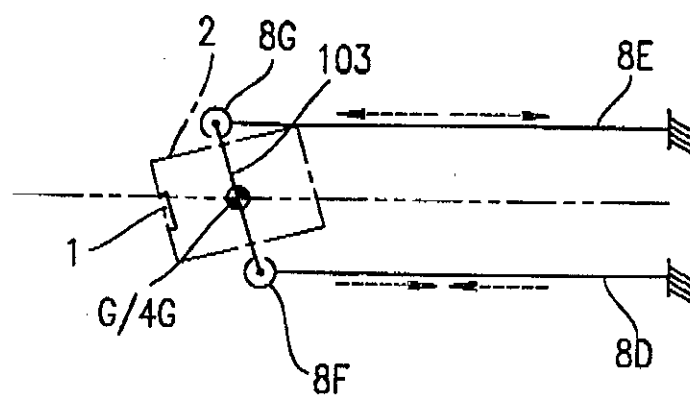


FIG.23A

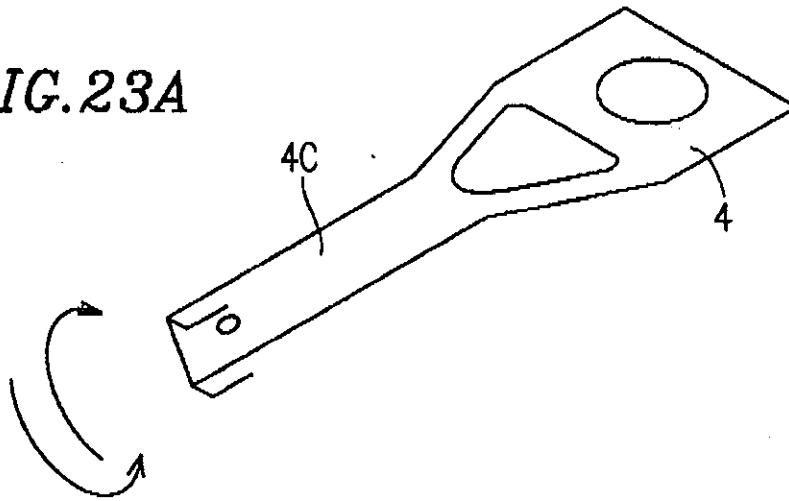


FIG.23B

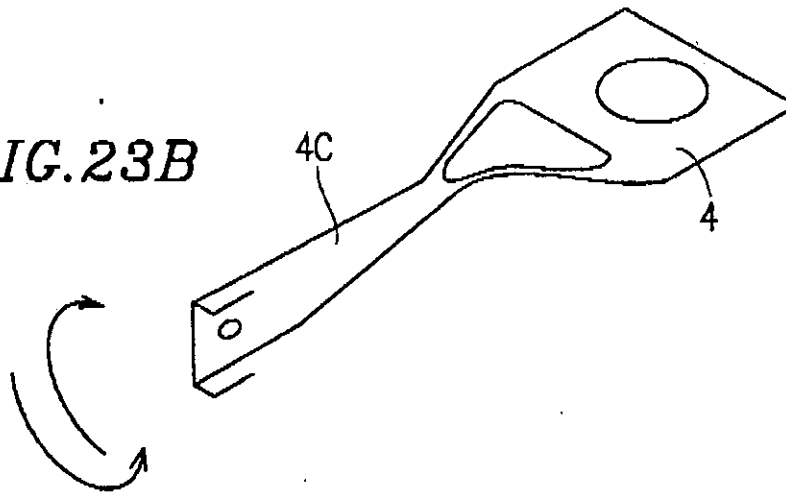
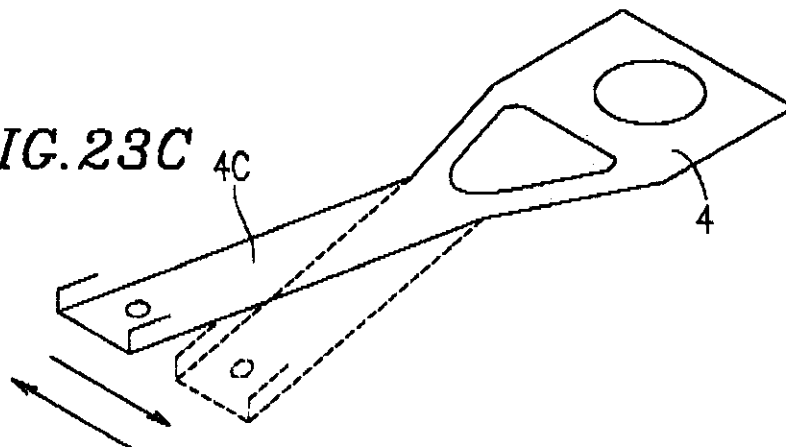


FIG.23C



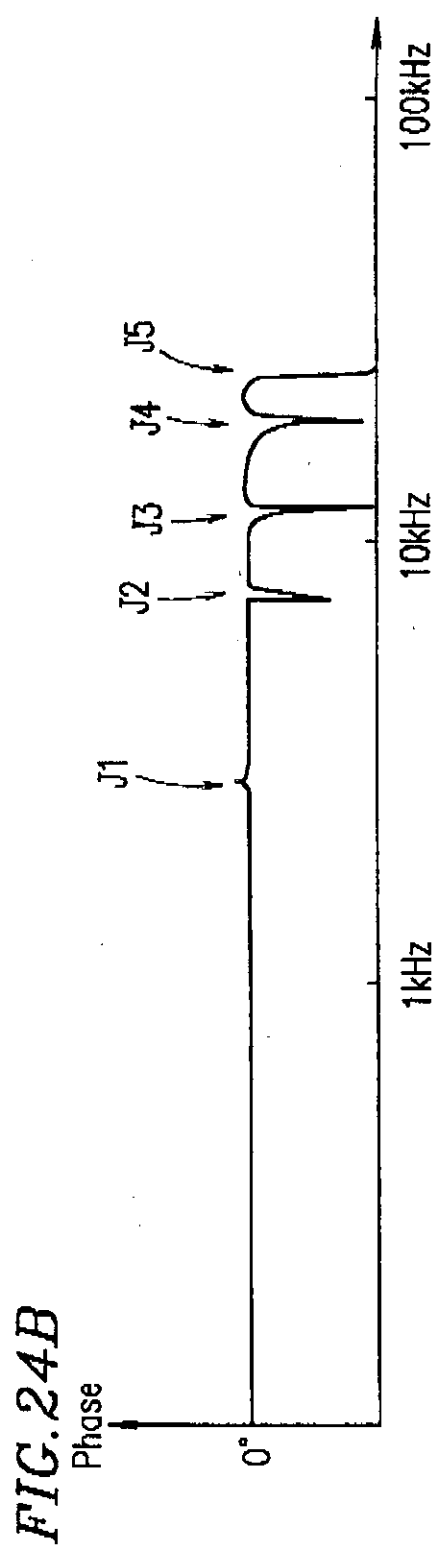
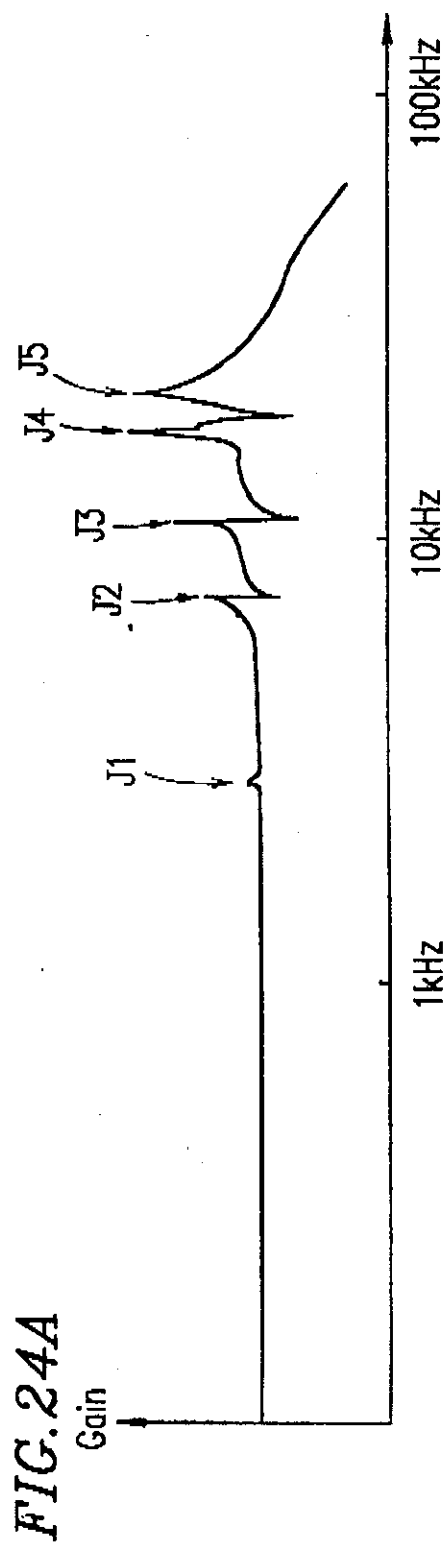


FIG. 25A

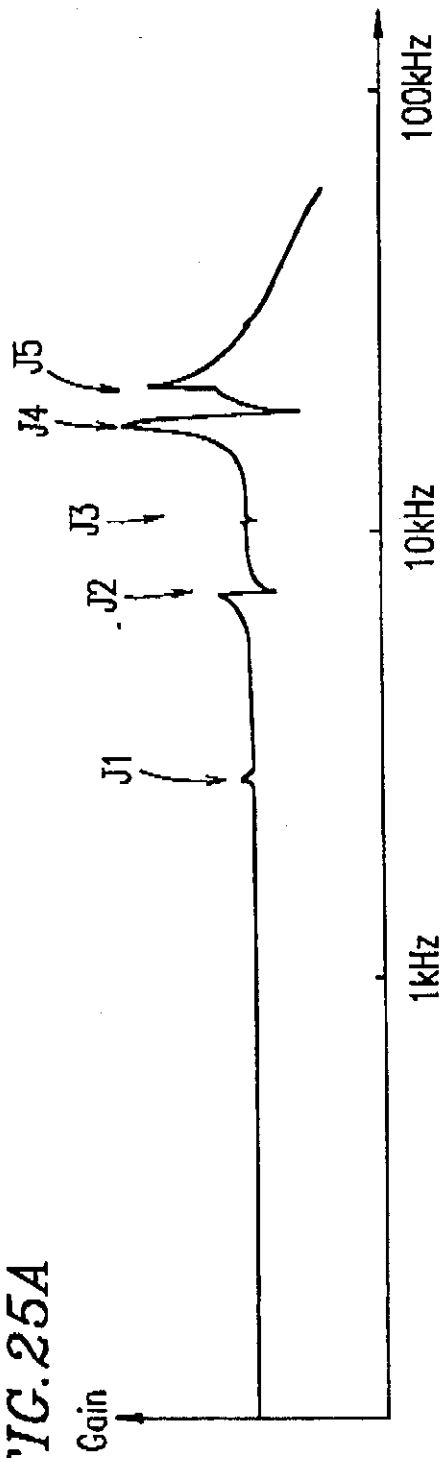


FIG. 25B

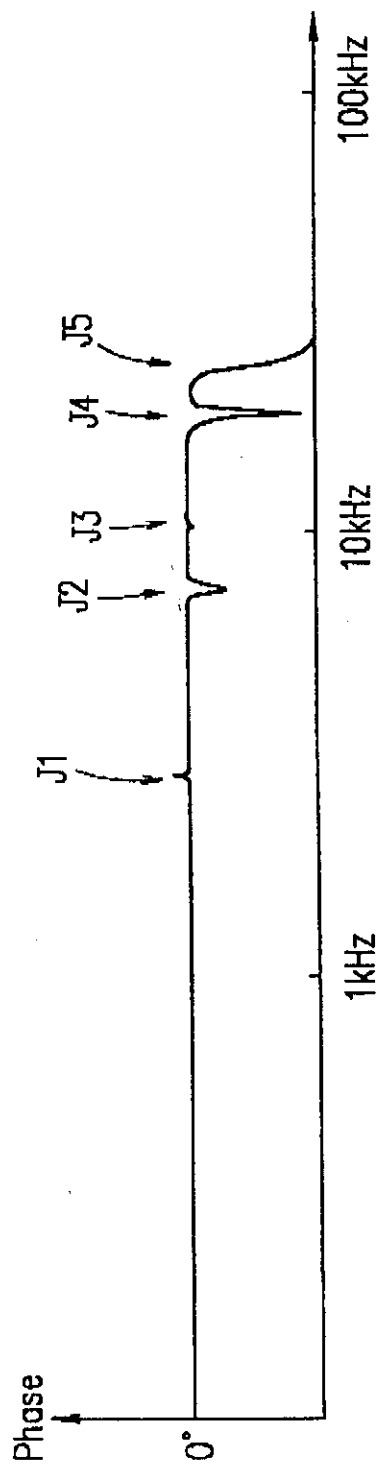


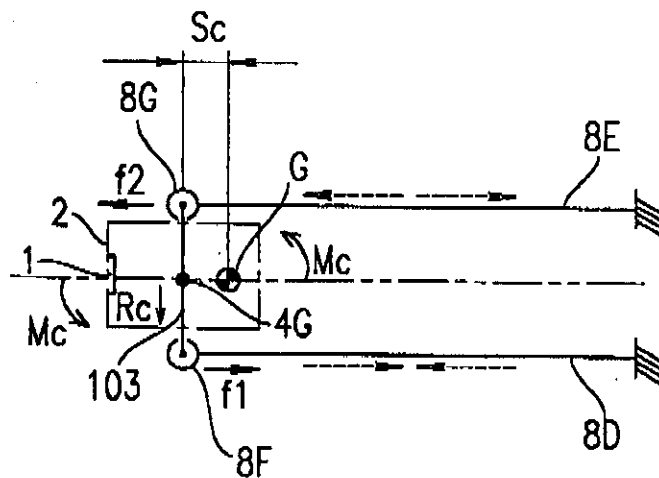
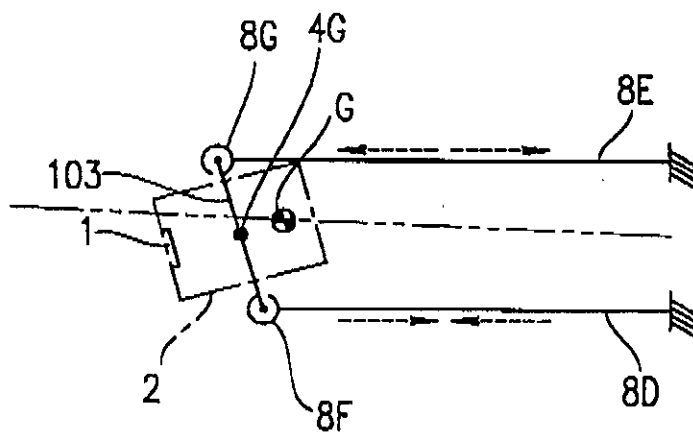
FIG. 26A**FIG. 26B**

FIG. 27A

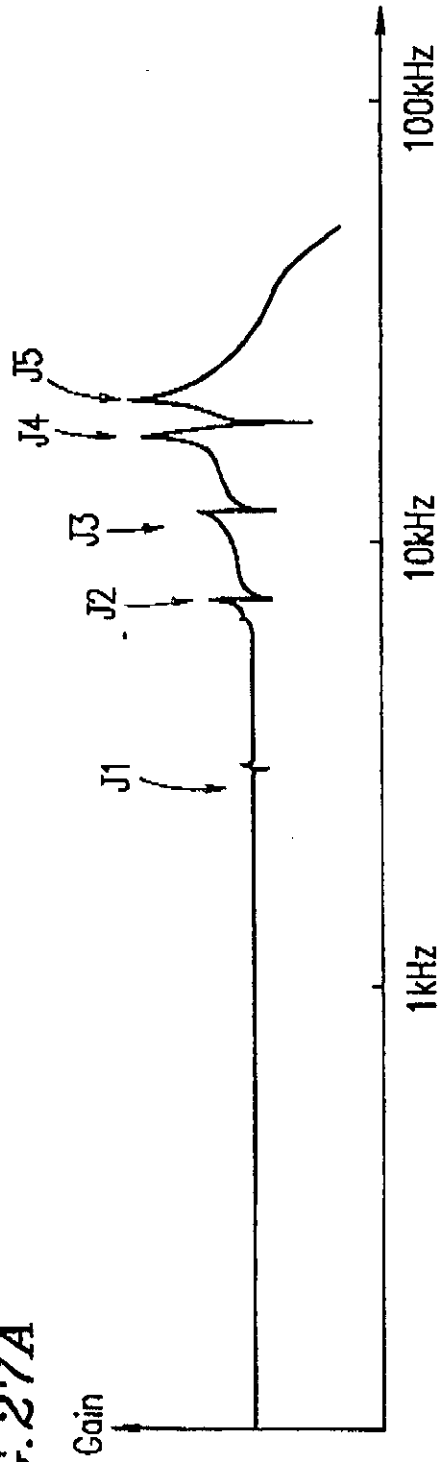
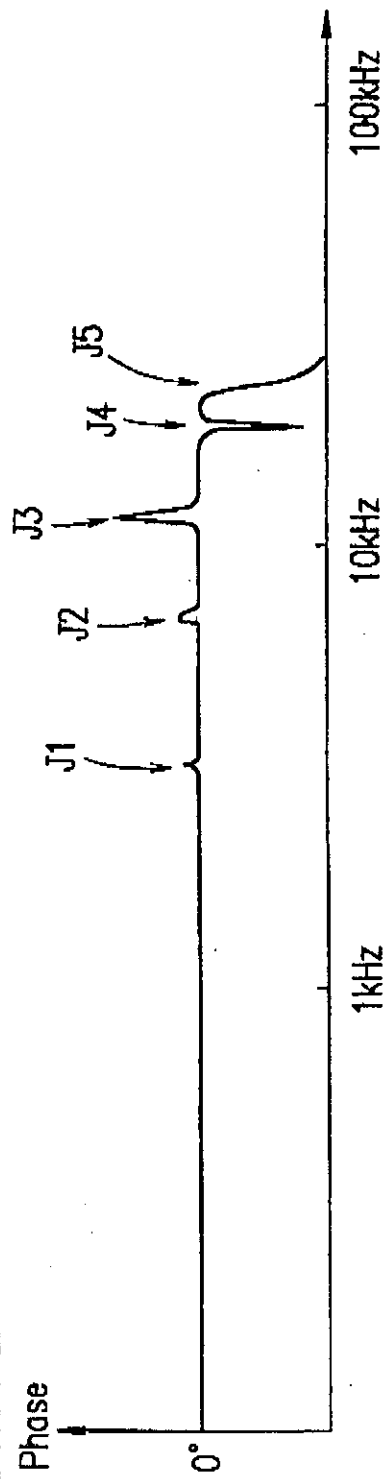
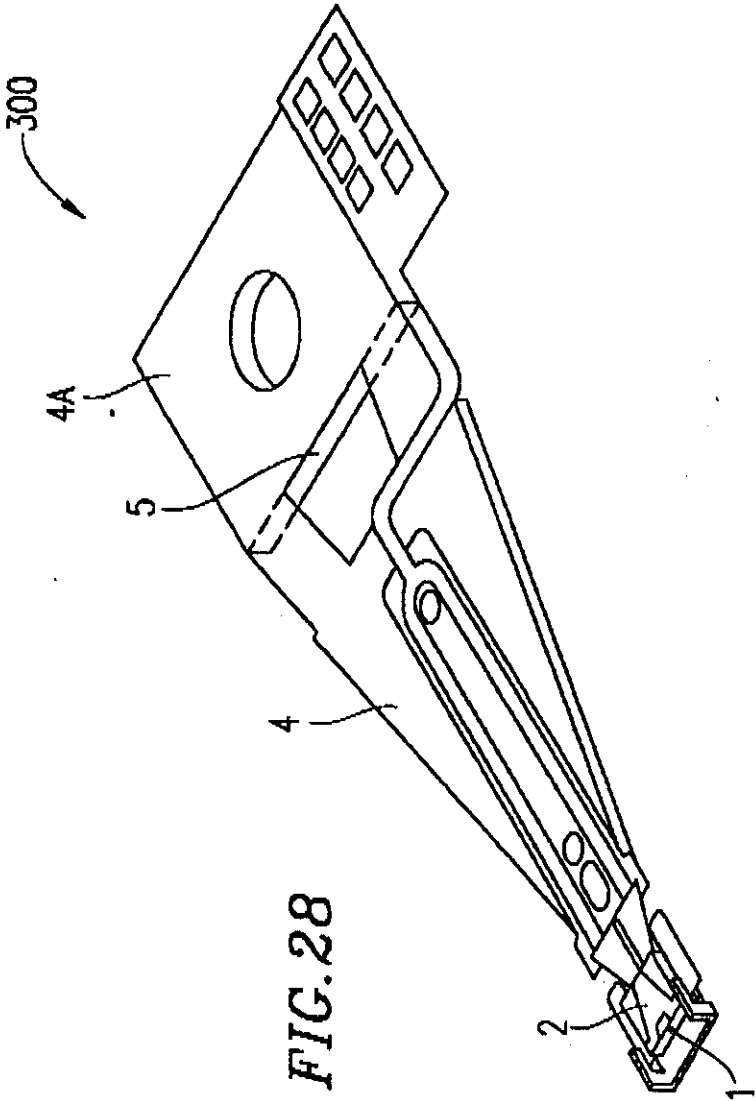
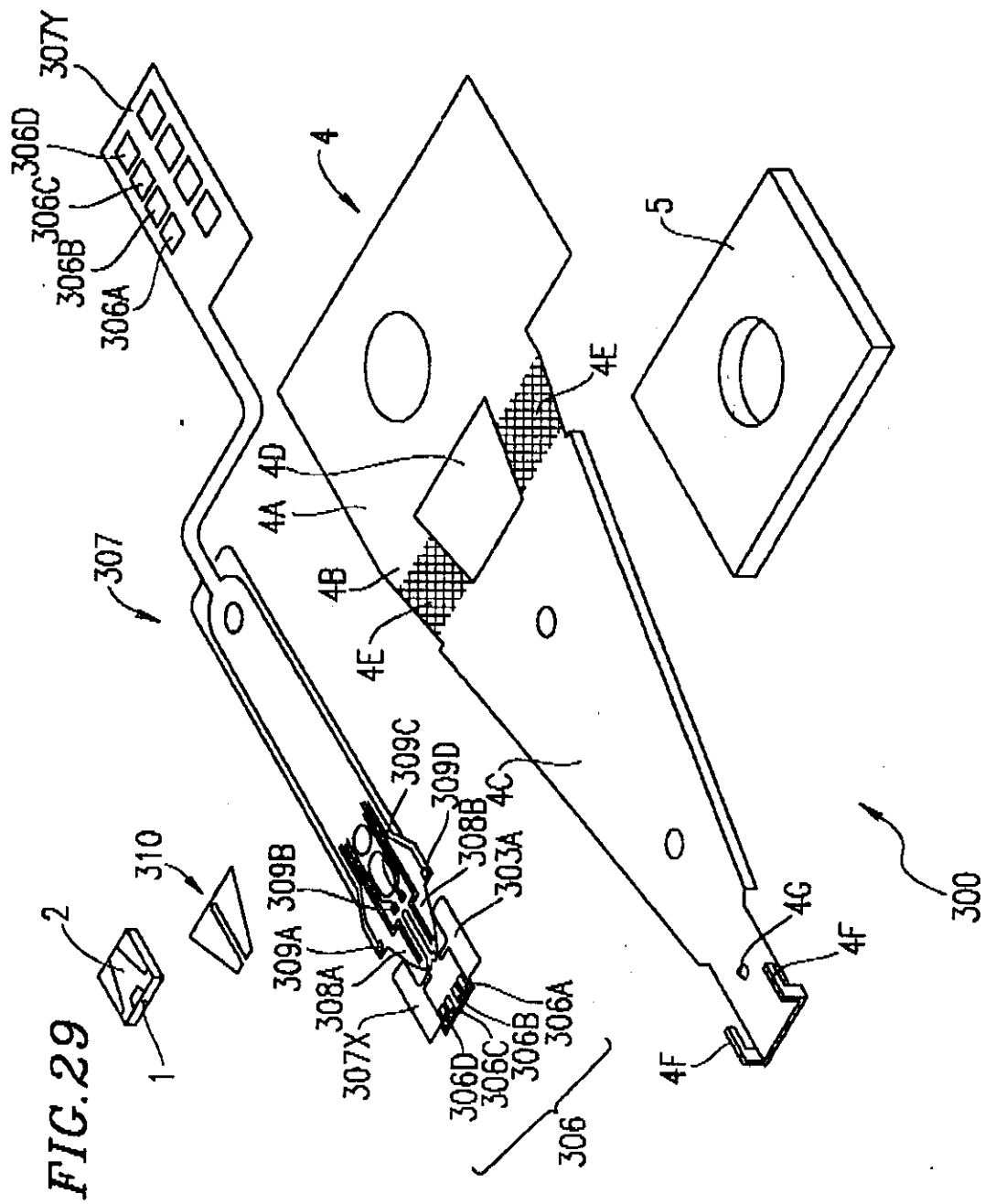


FIG. 27B







- 25 -

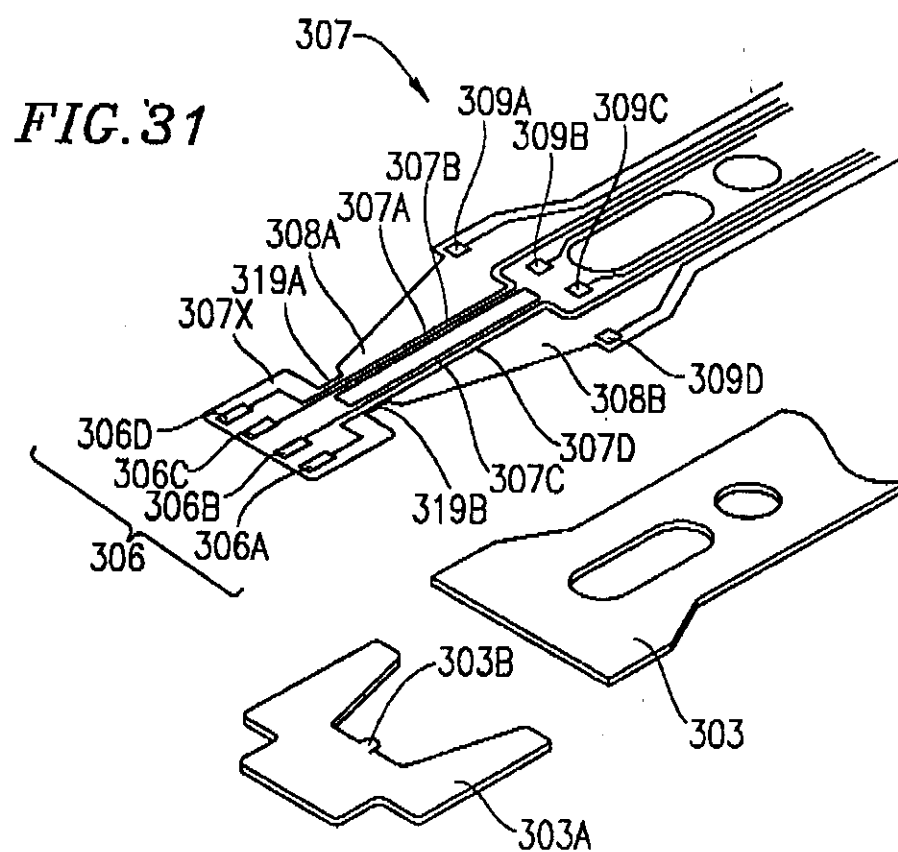
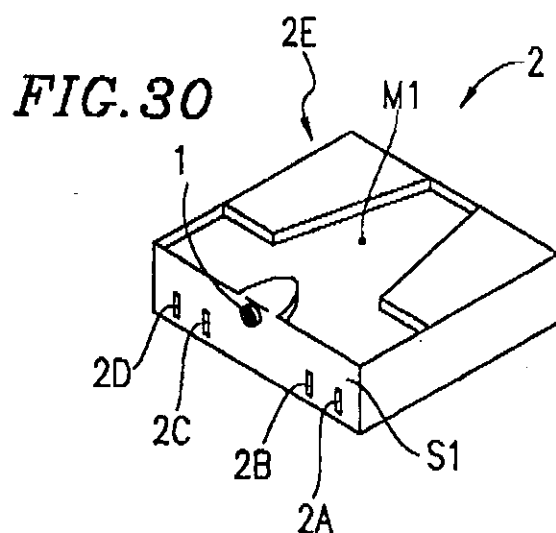


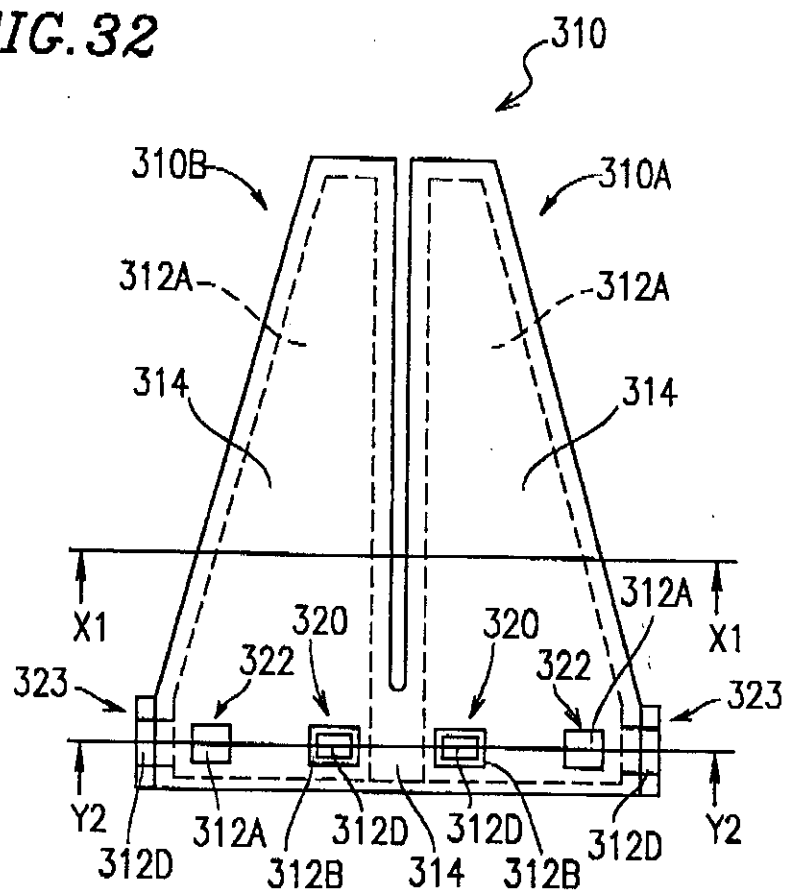
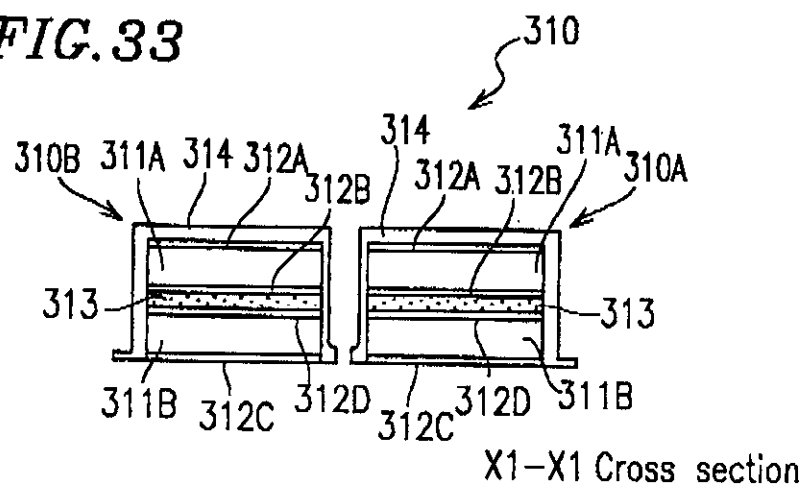
FIG. 32**FIG. 33**

FIG. 34

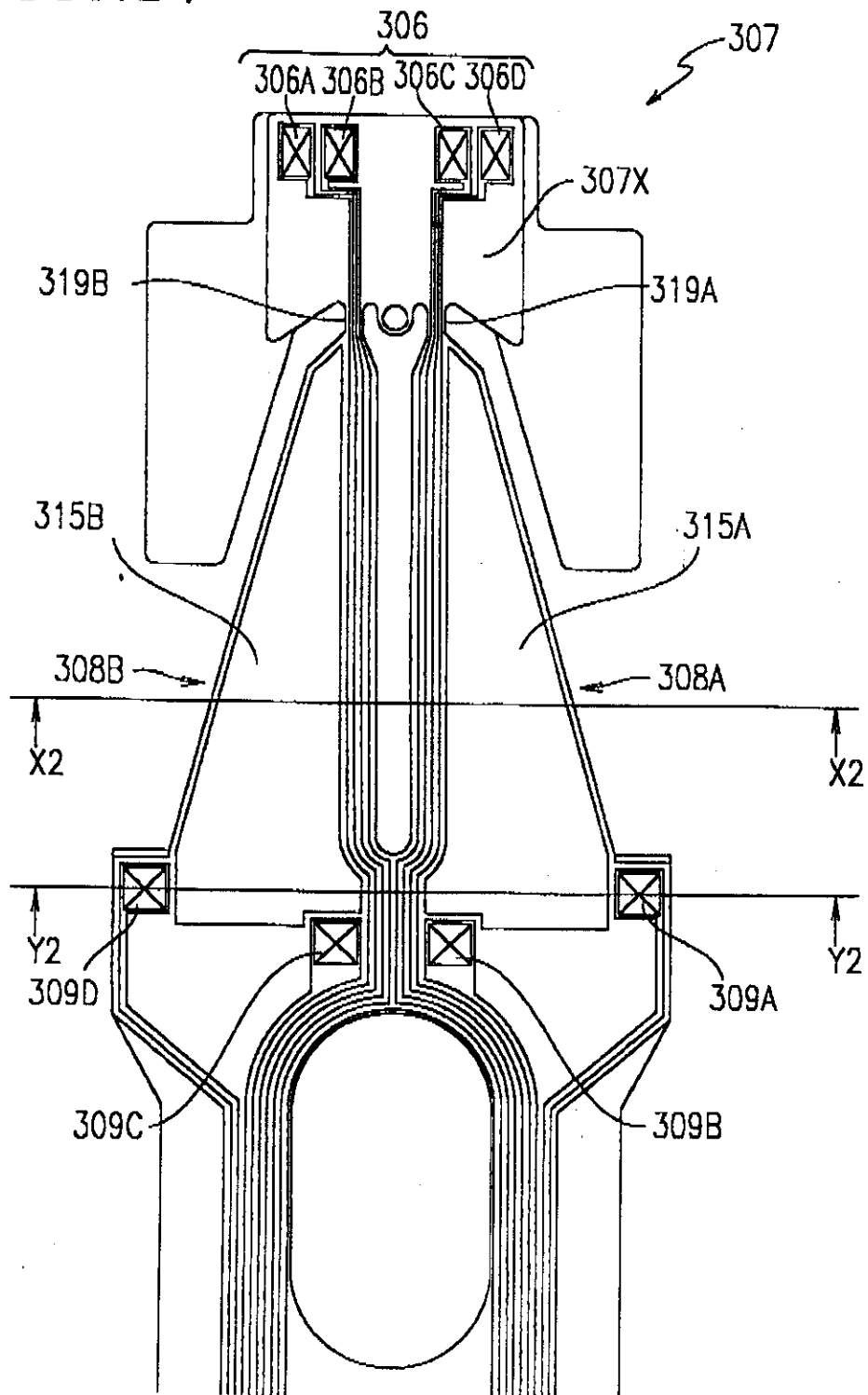
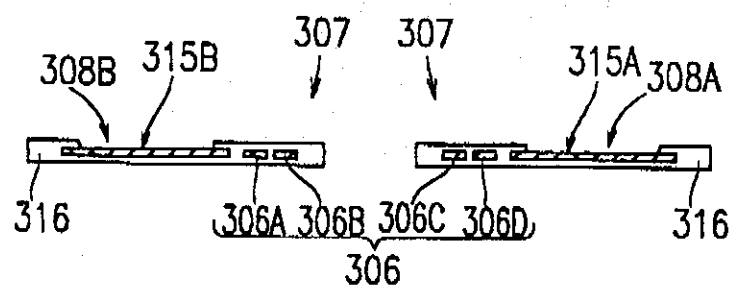


FIG. 35



X2-X2 Cross section

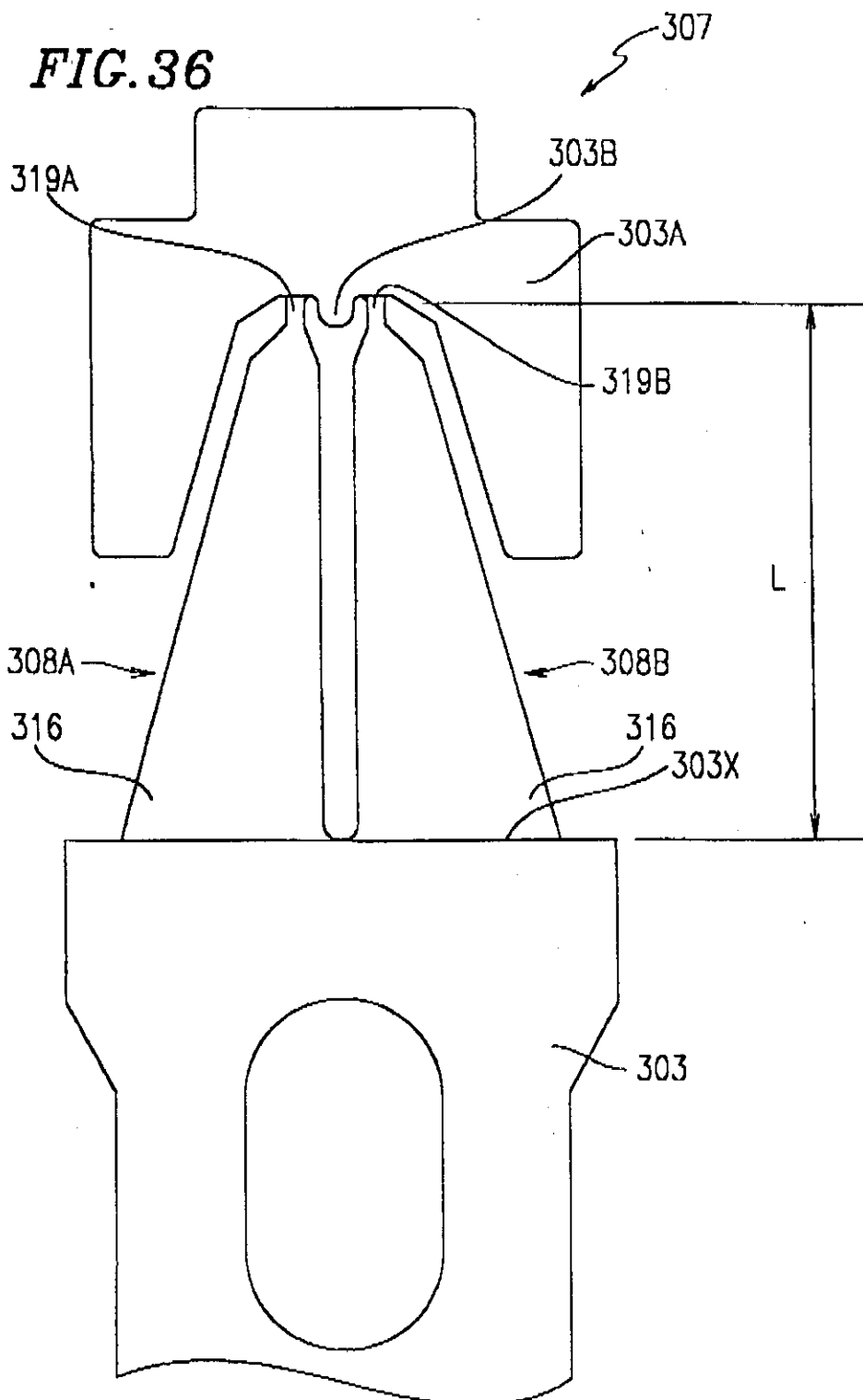


FIG. 37

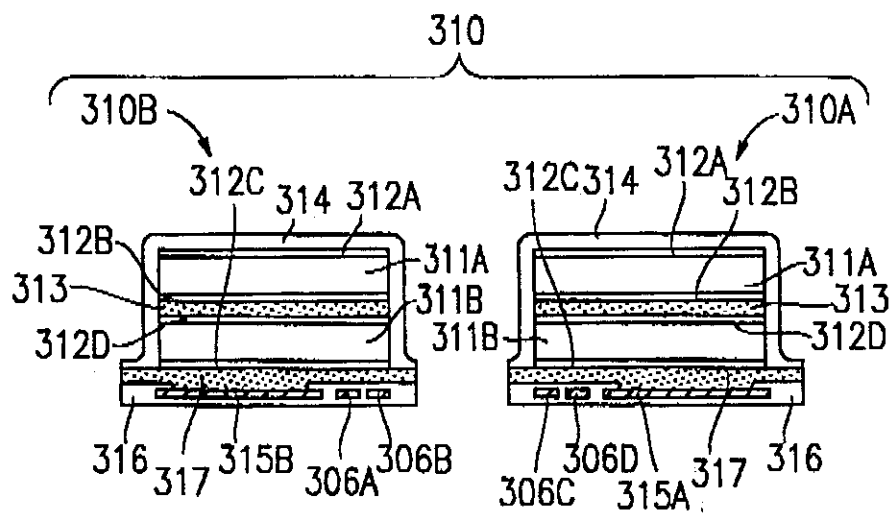


FIG. 38A

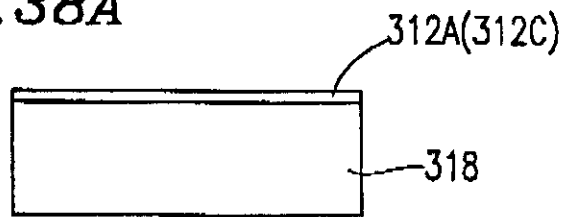


FIG. 38B

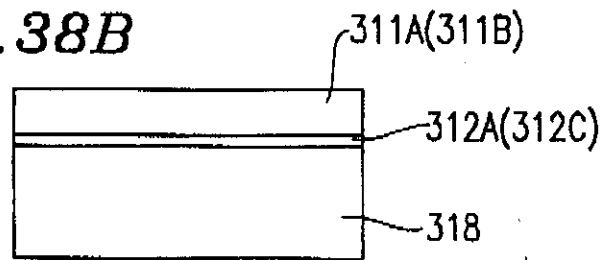


FIG. 38C

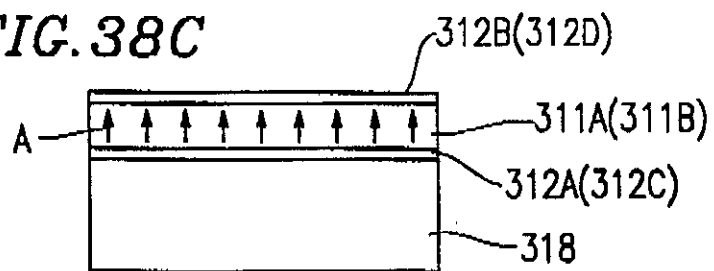


FIG. 39A

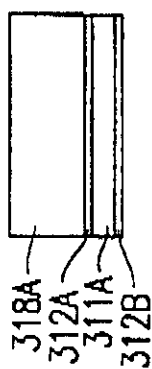


FIG. 39B

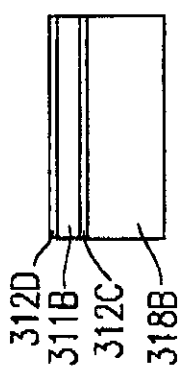


FIG. 39C

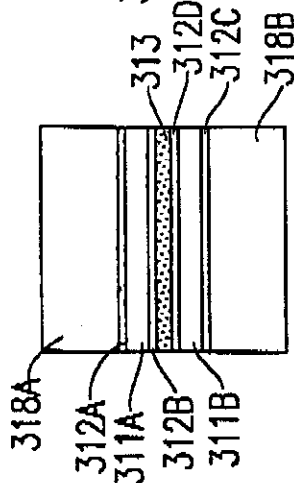


FIG. 39D

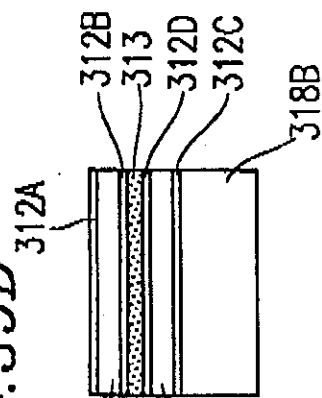


FIG. 39E

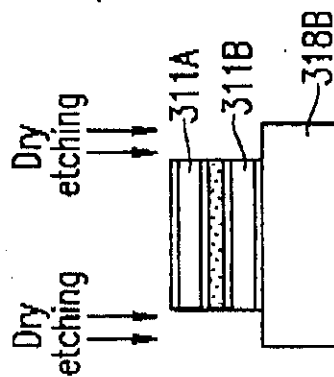


FIG. 39F

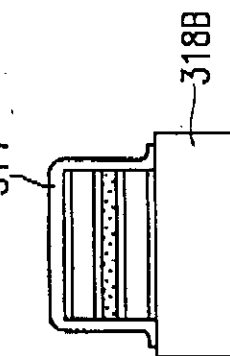


FIG. 39G

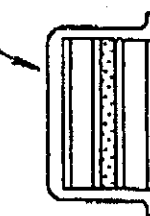
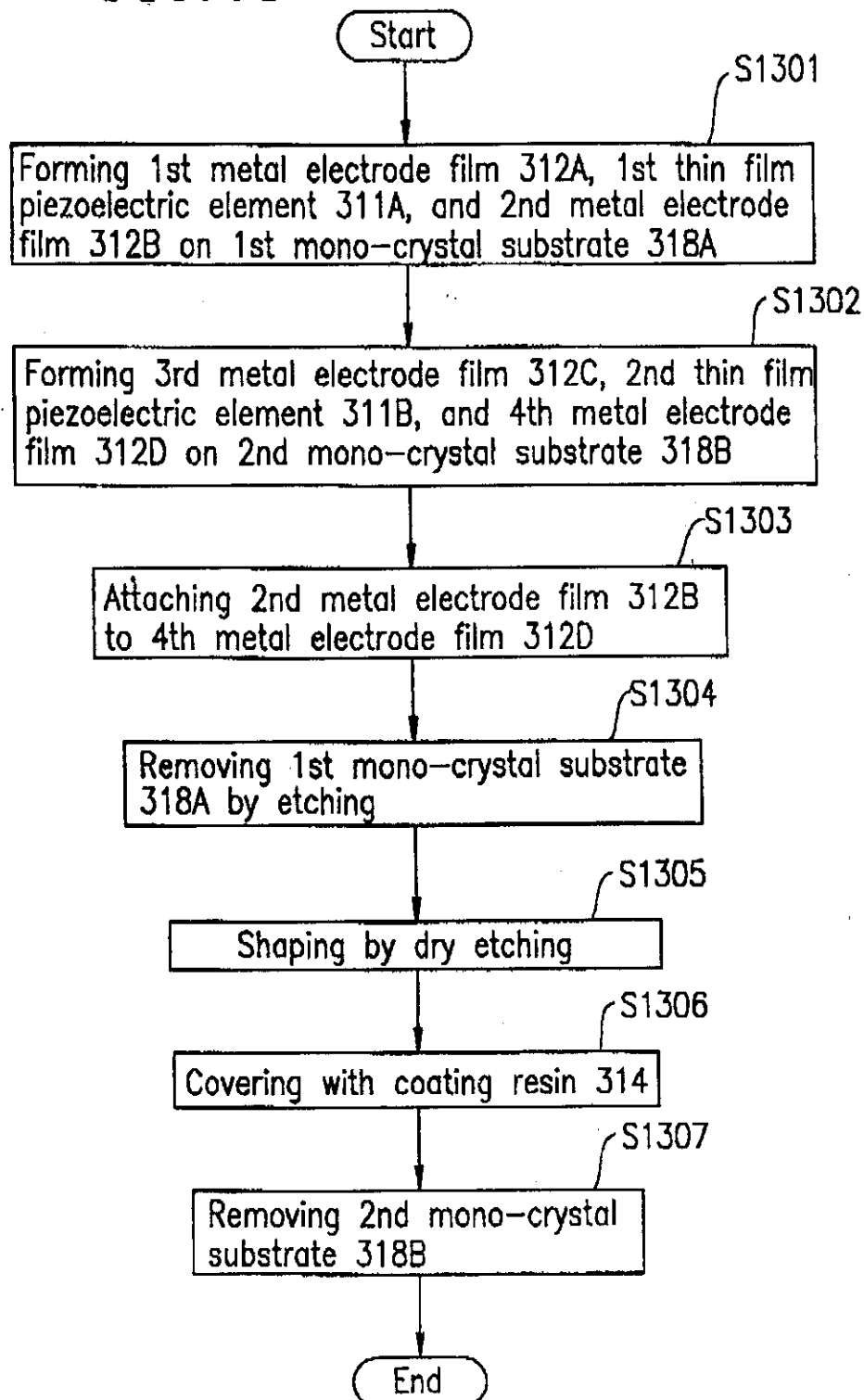
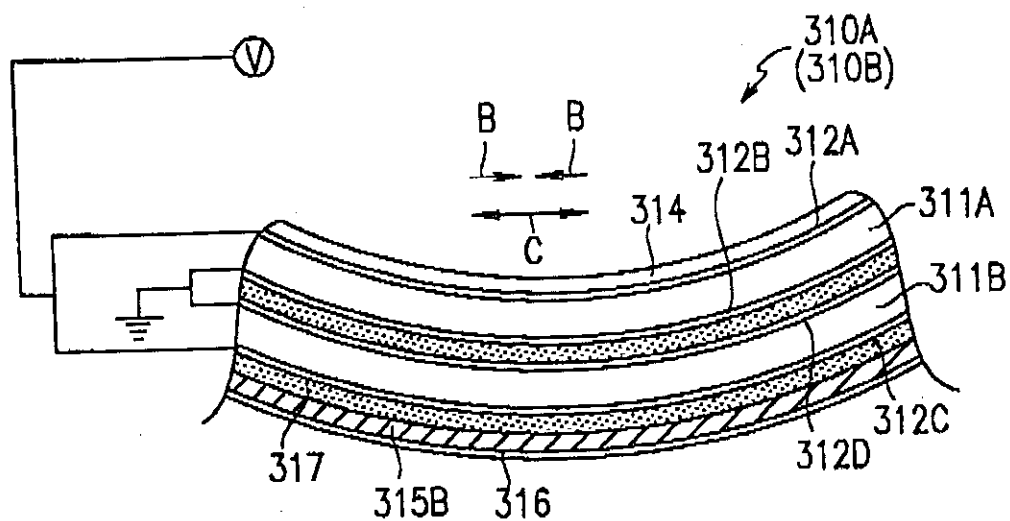
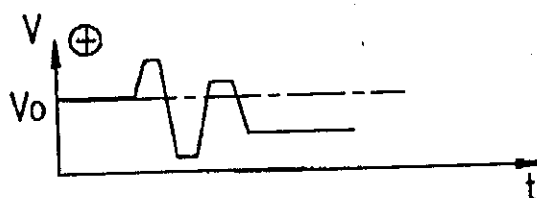


FIG. 40

This cross-sectional view shows a semiconductor device with a central channel region (310A) and side regions (310B). The device includes a substrate (309A, 309D) with a base layer (313) and a patterned layer (317). A central channel (311A, 311B) is formed in the substrate, with a gate stack (312A, 312B, 312C, 312D) on top. The gate stack consists of a gate dielectric (312A, 312B), a gate electrode (312C, 312D), and a gate spacer (312E, 312F). The side regions (310B) are doped with impurities (314) and have a gate stack (312A, 312B, 312C, 312D) on top. The device is surrounded by a protective layer (320, 321, 322, 323, 324).

FIG. 43A**FIG. 43B**

Voltage applied to
thin film piezoelectric
terminal 309A

**FIG. 43C**

Voltage applied to
thin film piezoelectric
terminal 309D

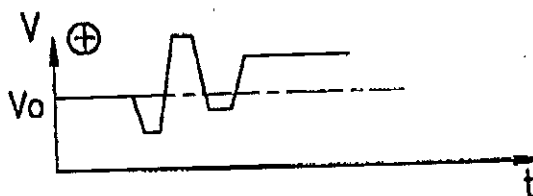


FIG. 44A

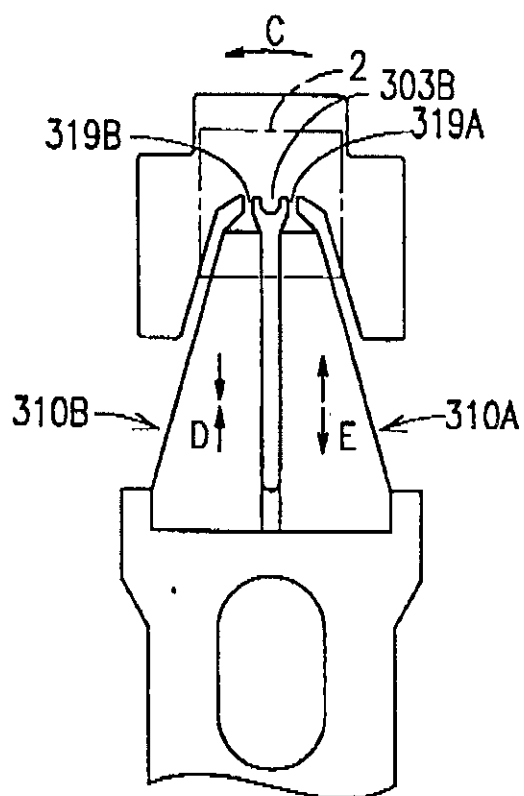
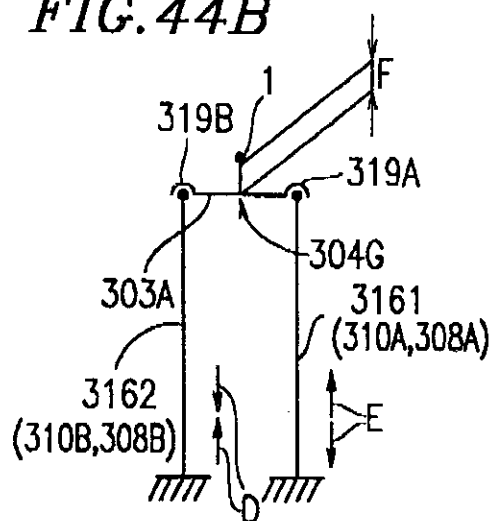


FIG. 44B



400

