CLAIMS

1. A control circuit, comprising a bias module, the bias module being configured to provide a bias current for a functional module,

the bias module comprising a first bias module and a second bias module, the first bias module being configured to provide a first bias current, and the second bias module being configured to provide a second bias current, wherein the first bias current is smaller than the second bias current, the first bias module is configured to be in a normally open state after being powered on, and the second bias module is configured to receive a bias enabling signal and provide the second bias current based on the bias enabling signal;

wherein the functional module is configured to receive an excitation signal and to be started based on the excitation signal, wherein a time point when the functional module receives the excitation signal is later than a time point when the bias module receives the bias enabling signal;

wherein the control circuit further comprises an enabling module, wherein

the enabling module is configured to receive a power switching signal and output the bias enabling signal and the excitation signal based on the power switching signal, wherein the power switching signal characterizes starting the functional module.

2. The control circuit of claim 1, wherein the power switching signal comprises a preceding first changing edge and a subsequent second changing edge, and

the enabling module is further configured to output the bias enabling signal at the first changing edge, and configured to output the excitation signal at the second changing edge.

3. The control circuit of claim 2, wherein a changing direction of the first changing edge is opposite to a changing direction of the second changing edge.

4. The control circuit of claim 2, wherein the first changing edge is switched from a low level state to a high level state, and the second changing edge is switched from a high level state to a low level state.

5. The control circuit of claim 1, wherein

the enabling module is further configured to receive a state signal, perform logical operation processing based on the power switching signal and the state signal, and output the bias enabling signal and the excitation signal, wherein the state signal characterizes that the control circuit is in a Power Down State or a Power On State.

6. The control circuit of claim 5, wherein the enabling module comprises a first logic module and a second logic module, wherein

the first logic module is configured to receive the power switching signal and the state signal, and perform first logic operation on the power switching signal and the state signal to output the bias enabling signal, and

the second logic module being configured to receive the power switching signal and the state signal, and perform second logic operation on the power switching signal and the state signal to output the excitation signal.

7. The control circuit of claim 6, wherein the first logic module comprises a first NOR gate, a

second NOR gate and a first NOT gate, wherein

one input end of the first NOR gate is configured to receive the power switching signal, the other input end of the first NOR gate is connected with an output end of the second NOR gate, one input end of the second NOR gate is connected with an output end of the first NOR gate, the other input end of the second NOR gate is configured to receive the state signal, and the output end of the second NOR gate is also connected with an input end of the first NOT gate.

8. The control circuit of claim 6, wherein the second logic module comprises a second NOT gate, a first NAND gate, a second NAND gate and a third NOT gate, wherein

an input end of the second NOT gate is configured to receive the state signal, an output end of the second NOT gate is connected with one input end of the first NAND gate, the other input end of the first NAND gate is connected with an output end of the second NAND gate, an output end of the first NAND gate is connected with one input end of the second NAND gate, the other input end of the second NAND gate is configured to receive the power switching signal, and the output end of the first NAND gate is also connected with an input end of the third NOT gate.

9. The control circuit of any one of claims 1-8, wherein the functional module comprises an input buffer circuit.

10. The control circuit of any one of claims 1-8, wherein the first bias module is connected in parallel with the second bias module, the first bias module comprises a first bias resistor, and the second bias module comprises a second bias resistor,

wherein a resistance value of the first bias resistor is greater than a resistance value of the second bias resistor.

11. The control circuit of claim 10, wherein the first bias module further comprises a first transistor, a second transistor, a third transistor and a fourth transistor, wherein

a drain electrode of the first transistor and a drain electrode of the second transistor are both connected with a power supply terminal,

a gate electrode of the first transistor and a gate electrode of the second transistor are both connected with a ground terminal,

a source electrode of the first transistor is connected with a drain electrode of the third transistor, a source electrode of the second transistor is connected with a drain electrode of the fourth transistor,

a gate electrode of the third transistor and a gate electrode of the fourth transistor are both connected with a source electrode of the third transistor, the source electrode of the third transistor is connected with the ground terminal through the first bias resistor, and

a source electrode of the fourth transistor is connected with the functional module, and configured to provide the first bias current for the functional module.

12. The control circuit of claim 10, wherein the second bias module further comprises a fifth transistor, a sixth transistor, a seventh transistor and an eighth transistor, wherein

a drain electrode of the fifth transistor and a drain electrode of the sixth transistor are both connected with a power supply terminal,

a gate electrode of the fifth transistor and a gate electrode of the sixth transistor are

both connected with the bias enabling signal,

a source electrode of the fifth transistor is connected with a drain electrode of the seventh transistor, a source electrode of the sixth transistor is connected with a drain electrode of the eighth transistor,

a gate electrode of the seventh transistor and a gate electrode of the eighth transistor are both connected with a source electrode of the seventh transistor, the source electrode of the seventh transistor is connected with the ground terminal through the second bias resistor, and

a source electrode of the eighth transistor is connected with the functional module, and configured to provide the second bias current for the functional module.