

IMPLEMENTATION METHOD AND SYSTEM OF RISV_V VECTOR INSTRUCTION SET VSETLI INSTRUCTION

ABSTRACT

The invention relates to the technical field of CPUs, in particular to a
 5 method and system for implementing a *risv_v* vector instruction set *vsetli*
 instruction. It allocates *vectag[n:0]* information in the rename module when
 the CPU executes out of order, and determines whether the instruction is
vsetli. If the instruction is *vsetli*, *vectag+1* is added. If it is a non-*vsetli*
 instruction, the *vectag* remains unchanged; it is sent to the execution unit,
 10 and the *vsetli* instruction is distributed to the *csr* module; the corresponding
 other vector instructions are distributed to the *vpu* module. When it is
 judged that the instruction *vectag* is consistent with the *vectag* broadcast by
 the ROB, the instruction is transmitted from the server station to the
 execution unit; the instruction execution is completed, and in the ROB
 15 module, it is graduated in order, and the register *vectag* is updated when it
 graduates, and the execution ends. The non- *vsetli* Vector instruction
 execution efficiency of the present invention is high. Data is selected by
 mask, which reduces power consumption, reduces execution cycle and
 latency, and has strong market application prospects.

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(The most illustrative figure is FIG 1)