

The present invention relates to a fast control circuit for power field effect transistors.

It applies to the production of power supplies and chopper converters and to the production of dc motor control devices.

The power transistors which are used in these applications must be able to switch rapidly in order to reduce energy losses and to increase the chopping frequency. The reduction of energy losses allows an increase in efficiency, simplification of the cooling systems and an increase in reliability. Increasing the chopping frequency allows a reduction in the size and price of the inductances, transformers and capacitors used and increases the response speed of slaved systems.

However, the development of these devices is slowed down by two principal obstacles which limit the switching speed of field effect transistors, these obstacles being the large values of the gate-source input capacity C_{GS} and of the drain-gate input capacity C_{DG} , the first one (C_{GS}) by simple capacitive effect and the second one by the Miller effect. These two capacities increase the rise time of the control signals applied to the gate inputs of field effect transistors and determine the time necessary to change from the voltage $V_{GS(off)}$ for which the transistor is in the off state to the voltage $V_{GS(on)}$ for which it is in the on state.

In order to reduce the opening or closing time of a power field effect transistor, a known solution consists in increasing the current passing through the gate of the transistor. This leads to interposing a fast switching current amplifier between the control circuit and the gate of the power transistor, but this solution encounters a few adaptation difficulties when, in certain embodiments, it is necessary to interpose galvanic isolation between the control circuit and the gate. This situation is encountered in particular when, for a static dc power supply for example, the chopper configuration is such that the source of one or more power transistors is taken to a large or variable potential or when, for

safety considerations, it is necessary to isolate the chopper circuit from the mains by means of a photocoupler or by means of a transformer.

5 Although a photocoupler allows the transmission of the signal as an information signal, it has the disadvantage that it must be followed by a fast amplifier supplied by an energy source which is itself galvanically isolated, which complicates this type of embodiment.

10 The use of a transformer, such as shown for example in the publication of the German patent application DE 3,243,660 A, on the other hand eliminates this disadvantage. In this circuit, capacitors are coupled to the secondary winding of the transformer. At the same time as the charging of the said capacitors, the gates of
15 the field effect transistors are submitted to the control signals supplied by the transformer. However, in order to be efficient, this transformer must have a low leakage inductance in order to have a response compatible with the control time of a few nanoseconds of power field
20 effect transistors, which makes this type of embodiment onerous.

 The purpose of the invention is to overcome the abovementioned disadvantages.

25 For this purpose, the subject of the invention is a fast control circuit for at least one power field effect transistor comprising a transformer with a primary winding and a secondary winding in order to transmit control signals to the gates of the field effect transistors, such control signals having alternately a first and
30 a second voltage level, such levels being of opposite sign, comprising:

35 - energy storing means coupled with the transformer in order to store, on the appearance of the control signals, the energy necessary for the control of the gate of the power field effect transistor during a first time interval during which the control signal is at its first voltage level,

 - transmission means coupled with the secondary winding of the transformer and solely supplied by the

energy storing means in order to transfer the energy stored in the energy storing means to the control gate of the power field effect transistor solely during a second time interval during which the control signal is at its second voltage level, and

- isolating means coupled between the secondary winding and the energy storing means in order to prohibit the transfer of energy from the secondary winding to the energy storing means and also to the energy transmission means during the second time interval during which the control signal is at its second voltage level.

Other characteristics and advantages of the invention will appear with the help of the following description given with reference to the appended drawings in which:

- Figures 1 and 2 are graphs illustrating the behaviour of a power field effect transistor in response to any control signal applied to its gate electrode;

- Figure 3 shows the known arrangement for controlling a power field effect transistor;

- Figure 4 shows a control signal;

- Figure 5 is a circuit diagram of an embodiment of a push-pull transformer control device for two power field effect transistors;

- Figure 6 is an example of an embodiment of a fast control circuit for power field effect transistors according to the invention.

The graphs shown in Figures 1 and 2 show the known general variation of the gate-source voltage V_{gs} of a field effect transistor as a function of the gate current I_g which is applied to it by its external gate control circuit. These graphs result from the fact that the two input capacities, the gate-source input capacity C_{gs} and the drain-gate input capacity C_{dg} of a transistor limit the derivative dV_{gs}/dt of the gate-source voltage V_{gs} with respect to the time t applicable to the gate by the control circuit and therefore determine the minimum time necessary for changing from the gate voltage $V_{gs(off)} = 0$ to the gate voltage $V_{gs(on)}$, and the time for changing from

the voltage $V_{GS(on)}$ to the voltage $V_{GS(off)}$ (switching off). The time for changing from $V_{GS(off)}$ to $V_{GS(on)}$ is, to a first approximation, equal to the sum of the charging times of the input capacity C_{GS} and of the discharge time of the drain-gate capacity C_{DG} . In figures 1 and 2 the gate-source capacity C_{GS} is charged between the times t_0 and t_1 by receiving a quantity of electricity Q_1 and then, between the times t_2 and t_3 , by receiving a quantity of electricity Q_3 and the drain-gate capacity is discharged between the times t_1 and t_2 by returning a quantity of electricity Q_2 .

Between the times t_0 and t_1 , the totality of the gate current I_g passes through the gate-source capacity C_{GS} . At the time t_1 the quantity of electricity Q_1 stored in the gate-source capacity C_{GS} satisfies the equation:

$$Q_1 = \int_{t_0}^{t_1} I_g \cdot dt$$

Between the times t_1 and t_2 , the voltage V_{GS} is stabilised by the Miller effect at the value $V_{GS(M)}$, the gate-source capacity C_{GS} receives a zero current and the drain-gate capacity C_{DG} receives the totality of the gate current I_g . At the time t_2 the quantity of electricity which has passed through the drain-gate capacity C_{DG} satisfies the equation

$$Q_2 = \int_{t_1}^{t_2} I_g \cdot dt$$

Between the times t_2 and t_3 , the totality of the gate current I_g flows in the gate-source capacity C_{GS} . Between t_2 and t_3 , the quantity of electricity stored in the gate-source capacity C_{GS} satisfies the equation

$$Q_3 = \int_{t_2}^{t_3} I_g \cdot dt.$$

In the general case, the function $I_g = f(t)$ being unknown, it is not possible to calculate its primitive $\int I_g \cdot dt$. But as the initial and final states t_0 and t_3 are themselves defined and, to a first approximation, the

current I_g can be considered as approximately constant in these intervals, it is possible to write

$$\int_{t_0}^{t_1} I_g \cdot dt = \left[\xi_{1g} \right]_{t_0}^{t_1} = I_{1g} (t_1 - t_0)$$

$$\int_{t_1}^{t_2} I_g \cdot dt = \left[\xi_{2g} \right]_{t_1}^{t_2} = I_{2g} (t_2 - t_1)$$

$$\int_{t_2}^{t_3} I_g \cdot dt = \left[\xi_{3g} \right]_{t_2}^{t_3} = I_{3g} (t_3 - t_2)$$

5 $\xi_1(g)$, $\xi_2(g)$ and $\xi_3(g)$ are primitives of the functions $I_g(t)$ defined over the intervals t_0 to t_1 , t_1 to t_2 and t_2 to t_3 , respectively. I_{1g} , I_{2g} and I_{3g} are the average gate currents between t_0 and t_1 , t_1 and t_2 , t_2 and t_3 . These time intervals are defined by the equations

$$t_1 - t_0 = \frac{Q_1}{I_{1g}} = \frac{V_{GS(M)} \cdot C_{GS}}{I_{1g}}$$

$$t_2 - t_1 = \frac{Q_2}{I_{2g}} = \frac{V_{DS(off)} \cdot C_{GD}}{I_{2g}}$$

$$t_3 - t_2 = \frac{Q_3}{I_{3g}} = \frac{V_{GS(on)} - V_{GS(M)} \cdot C_{GS}}{I_{3g}}$$

10 The total switching time is, under these conditions, equal to $t_c = t_3 - t_0$ and equal to $t_3 - t_2 + t_2 - t_1 + t_1 - t_0$ which is again equal to:

$$t_c = \frac{V_{GS(M)} \cdot C_{GS}}{I_{1g}} + \frac{V_{DS(off)} \cdot C_{GD}}{I_{2g}} + \frac{V_{GS(on)} - V_{GS(M)} \cdot C_{GS}}{I_{3g}}$$

15 These equations taken together show that the times necessary for switching a field effect transistor on or off can be reduced by increasing the value of the average current I_{2g} .

But the dispersions of the voltage V_{gsth} which represents the threshold gate-source voltage, on the one hand, and the necessity of fast immunity to noise both on closing and on opening on the other hand, also lead to increasing the values of the average currents $I_1(g)$ and $I_3(g)$.

Thus, in order to profit from one of the principal advantages of a field effect transistor conferred by its speed, it is necessary to forgo the great advantage provided by its voltage control facilities. Taking for example the case of a transistor of the IRF350 type, and taking account of the fact that its gate-source capacity C_{gs} and its drain-source capacity C_{ds} cannot be considered as constants for voltages V_{ds} included in the range 0 to 50 volts, the quantity of electricity to be applied to the gate in order to obtain complete switching is $Q_1 + Q_2 + Q_3 = Q_c = 120$ nanocoulombs. In order to carry out a switching under these conditions and in a time $(t_3 - t_0)$ 60 nanoseconds, the average current I_g applied to the gate must be equal to:

$$I_g = \frac{Q_c}{t_3 - t_0} = \frac{120 \text{ nanocoulombs}}{60 \text{ nanoseconds}} = 2 \text{ amperes}$$

This leads, in the known solutions, to the interposing of fast switching current amplifiers 1 between the control circuits 2 of the power field effect transistors 3 in the way which is shown in Figure 3, supplied between a voltage potential V_A and an earth circuit M. But these solutions, when they are implemented by carrying out a galvanic isolation by means of a transformer, are costly. On the other hand, the leakage inductances L of the transformers must be reduced as much as possible in order to be compatible with the control times of a few tens of nanoseconds of the field effect transistors.

The solution proposed by the invention consists in interposing, between each transformer and power field effect transistor signal receiver, at least one element

which:

1) demands energy from the transformer during the non-significant phases of the signal and stores this energy,

5 2) receives the significant phases of the signal while exhibiting an infinite impedance without consequently demanding energy from the transformer and without affecting the signal and, finally,

10 3) transmits this signal with the necessary energy to the envisaged receiver, this energy being taken from the store of energy produced during the non-significant phases of the signal.

 This principle can not only be applied to embodiments of signal receiver controls with devices according
15 to the invention interposed between a secondary winding of a transformer supplying the control signal and each signal receiver device, but can also apply, as shown in Figure 5, to several devices 5, 6, according to the invention, interposed between signal receivers formed by
20 two transistors 8, 9 connected in series push-pull and supplying a common load 10 shown dotted; and secondary windings respectively referenced 7₂ and 7₃ of transformers 7 whose primary 7₁ is controlled by signals of rectangular type, having the shape of the one which is shown in
25 Figure 4, having positive and negative alternations during the time intervals A and C respectively and a zero amplitude during an intermediate time interval B between the intervals A and C.

 An example of embodiment of the circuits 5 and 6
30 is shown in Figure 6.

 The circuit according to the invention which is shown in Figure 6 is placed between a signal transformer 11 comprising two windings, a primary winding and a secondary winding, respectively referenced 11₁ and 11₂,
35 and a signal receiver represented in Figure 6 by a half-stage 12 of a series power push-pull configuration, the other half-stage 13 being dotted. The power receiver is controlled by two "MOSFET" stages connected in series 14 and 15 whose gates are respectively connected, one of

them directly to a terminal A of the secondary winding 11₁, and the other of them via a capacitor 16 and a resistor 17 connected in parallel.

5 The capacitors at 18 and 19 are connected in parallel with the terminals of the secondary 11₂, via two diodes 20 and 21 connected by an anode and by a cathode respectively to the terminal A in order to form, with the capacitors 18 and 19, a voltage doubler.

10 Assuming that a signal of the type which is shown in Figure 4 is applied to the primary 11₁ of the transformer 11, the functioning of the circuit shown in Figure 6 is as follows. This signal, on appearing at the terminals of the secondary winding 11₂, charges the capacitors 18 and 19 during the times marked A and C in
15 Figure 4, via the diodes 20 and 21, to its peak values, the transistors 14 and 15 being closed during the time intervals A and C respectively of the signal. The charge currents of the capacitors 18 and 19 are zero during the rising and falling edges of the signal which, under these
20 conditions, is not affected. The energy necessary for the functioning of the transistors 14 and 15, which are in the source follower configuration, is then supplied by the capacitors 18 and 19 which are then isolated from the secondary 11₂ by the diodes 20 and 21 during the significant
25 phases of the signal, the transistors 14 and 15 being open during the time intervals C and A respectively. In this way, no energy is taken from the transformer during the significant phases of the signal. In order to make the circuit according to the invention
30 even more efficient, it will be possible to select the input capacities of the transistors 14 and 15 in such a way that they are in the order of 100 times lower than that of the power transistors 12 in order to solve the rise time and decay time problems. Similarly, the values
35 of the resistors 17, 22 and of the capacitor 16 will be chosen in order to effectively bias the transistor 15 in order to compensate for the threshold voltages V_{esth} and to lower the level of the signal below a voltage of 0 in order to improve noise immunity.



CLAIMS

1. Fast control circuit for at least one power field effect transistor (12, 13) comprising a transformer with a primary winding (11₁) and a secondary winding (11₂) in order to transmit control signals to the gates of the field effect transistors, such control signals having alternately a first and a second voltage level, such levels being of opposite sign, comprising:

- energy storing means (18, 19) coupled with the transformer (11) in order to store, on the appearance of the control signals, the energy necessary for the control of the gate of the power field effect transistor (12, 13) during a first time interval (A and, respectively, C) during which the control signal is at its first voltage level,

- transmission means (14, 15) coupled with the secondary winding of the transformer and solely supplied by the energy storing means (18, 19) in order to transfer the energy stored in the energy storing means (18, 19) to the control gate of the power field effect transistor (12, 13) solely during a second time interval (C and respectively, A) during which the control signal is at its second voltage level, and

- isolating means (20, 21) coupled between the secondary winding (11₂) and the energy storing means (18, 19) in order to prohibit the transfer of energy from the secondary winding (11₂) to the energy storing means (18, 19) and also to the energy transmission means (14, 15) during the second time interval during which the control signal is at its second voltage level.

2. Circuit according to Claim 1, characterised in that the energy storing means (18, 19) comprise at least one capacitor connected in parallel with the terminals of the secondary winding (11₂) of the transformer via at least one diode (20, 21).

3. Control circuit according to either one of Claims 1 or 2, characterised in that the transmission means are constituted by field effect transistors (14, 15)



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configured as a voltage follower stage and fed by the storing means (18, 19).

4. Control circuit according to Claim 3, characterised in that the transmission means (14, 15) are
- 5 constituted by a push-pull stage formed by two complementary field effect transistors (14, 15) connected in series and with their source electrodes connected to at least one gate of the power field effect transistors (12, 13) to be controlled.