

## **ZERO-MISALIGNMENT TWO-VIA STRUCTURES USING PHOTOIMAGEABLE DIELECTRIC, BUILDUP FILM, AND ELECTROLYTIC PLATING**

### **FIELD**

- 5 Embodiments relate to semiconductor devices. More particularly, the embodiments relate to packaging semiconductor devices with that include zero-misalignment two via structures.

### **BACKGROUND**

10 One of the main drivers for packaging semiconductor devices and package design rules is the maximum 1D linear number density of routing traces per mm per layer. Limitations to routing traces/mm/layer are derived from process limitations during substrate manufacturing, and typically vary by process. As such, a key set of process limitations directly stem from the ability to align the features in a given layer to the vertical interconnects, which connect that layer to the layers above and below it.

15 Package layers and the vertical interconnects coupled with them are fabricated on a substrate in a serial fashion, with common sets of fiducials included within the layers. Fiducials are used to measure overlay and misalignment between process steps. Errors in fiducial fabrication translate to misalignment, as do errors in reading fiducials. Even when fiducials are fabricated and read precisely, inherent tool overlay errors results in additional misalignment.

20 Finally, deformation of the substrate introduces locally variable misalignment and global distortion that cannot be corrected. This distortion and misalignment varies with substrate materials and with process parameters such as applied stress and temperature-gradient induced stress. These factors add up to limit the misalignment of routing lines to the vertical interconnects that intersect them.

25 For example, in order to allow for misalignment between layers and vertical interconnects that connect them, critical dimensions must be enlarged in the routing layer to allow for misalignment error. Unfortunately, enlarging critical dimension will significantly limit the design rules for package design. Since so many of the misalignment drivers are process specific, design rules must be either overly conservative to allow for process variation or else  
30 require more design resources to optimize around variable design rules.

Recently, there have been three main solutions which have attempted to overcome these limitations and problems – only to have their own drawbacks. First, improvements have been made to lithography (litho) and laser patterning overlay capability. Many of these solutions result in increased capital equipment costs or reduced throughput. For instance, locally aligned  
35 lithography exposures come with an inherently lower throughput, mainly due to the time needed

to align to more fiducials and to move between fields. Second, interposers and bridge are fabricated and assembled to the substrate, but these are not always cost-effective due to the cost of fabricating and testing the interposers or bridges and due to the additional assembly costs. Thirdly, routing layers are fabricated on silicon or glass carriers such that the substrate is stabilized dimensionally. This is cost-effective only for a subset of package sizes.

One of the packaging solutions is lithographically defined vias on a pad. In this case, the line density may be significantly reduced by the presence of a pad that must accommodate a via as well as account for the misalignment associated with via lithography on the pad. Another packaging solution is typically referred to as self-aligned via (SAV) technology. The SAV approach is generally applied when lithography capability limits the minimum space between traces to values that are at or slightly above twice the misalignment capability of the exposure tool. Lastly, there is also a misalignment-via approach (or a zero-misalignment via (ZMV)) that schematically resembles SAV, but due to a different manufacturing process, the space between traces is only limited by the exposure tool resolution capability.

The misalignment-via approach maximizes trace density in all cases for any exposure tool, while SAV can get close to the maximum for specific cases and design rules. These solutions, however, have their own problems and drawback. For example, with the misalignment-via and SAV approaches, the main problems is that a trace can be connected to self-aligned or zero-misaligned vias only in one direction (either above or below the trace). However, this leads to a major problem in package design rules, which may require a connection to both a top layer and bottom layer without reducing the trace density (*i.e.*, this is referred to as a two-via structure). In these cases, the misalignment-via and SAV approaches cannot help and end up as the vias on the pad approach that is fully or in part dependent on the design.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

Embodiments described herein are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar features. Furthermore, some conventional details have been omitted so as not to obscure from the inventive concepts described herein.

Figure 1 is a perspective view of a conductive trace with zero-misaligned vias, according to one embodiment.

Figure 2A is a perspective view of one or more conductive traces with zero-misaligned vias, according to one embodiment.

Figure 2B is a projection view of a portion of the one or more conductive traces with zero-misaligned vias in a semiconductor package, according to one embodiment.

Figure 3A is a plan view of a semiconductor package having interconnect package layers with one or more conductive traces with zero-misaligned vias, according to one embodiment.

Figure 3B is a projection view of a portion of a semiconductor package having interconnect package layers with one or more conductive traces with zero-misaligned vias, according to one  
5 embodiment.

Figure 4A is a plan view of a semiconductor package having interconnect package layers with one or more conductive traces with zero-misaligned vias, according to one embodiment.

Figure 4B is a projection view of a portion of a semiconductor package having interconnect package layers with one or more conductive traces with zero-misaligned vias, according to one  
10 embodiment.

Figure 5A is a perspective view of one or more conductive traces with zero-misaligned vias, according to one embodiment. Figures 5B and 5C are corresponding cross-sectional views of one or more conductive traces with zero-misaligned vias, according to some embodiments.

Figure 6A is a perspective view of one or more conductive traces with zero-misaligned vias, according to one embodiment. Figures 6B and 6C are corresponding cross-sectional views of one or more conductive traces with zero-misaligned vias, according to some embodiments.  
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Figures 7A – 7M are a process flow illustrating a method of forming a conductive trace with zero-misaligned vias using a photoimageable dielectric (PID) stack and electrolytic plating, according to some embodiments.

Figures 8A – 8K are a process flow illustrating a method of forming a conductive trace with zero-misaligned vias using a buildup dielectric film stack and electrolytic plating, according to some embodiments.  
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Figures 9A – 9H are a process flow illustrating a method of forming a conductive trace with zero-misaligned vias using a dose selective resist and a multi-tone mask, according to some  
25 embodiments.

Figures 10A – 10I are a process flow illustrating a method of forming a conductive trace with zero-misaligned vias using a PID film stack with electrolytic plating on a substrate, according to some embodiments.

Figure 11 is a schematic block diagram illustrating a computer system that utilizes a  
30 device package with conductive trace with zero-misaligned vias, according to one embodiment.

## **DETAILED DESCRIPTION**

Described herein are systems that include zero-misalignment two-via stack (ZM2VS) for various signal routing application. In the following description, various aspects of the illustrative  
35 implementations will be described using terms commonly employed by those skilled in the art to

convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present embodiments may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations.

- 5 However, it will be apparent to one skilled in the art that the present embodiments may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

- Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present embodiments, however, the order of description  
10 should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

- One of the main drivers for package design rules is the input/output (I/O) linear number density per mm per layer (IO/mm/layer). The I/O density may be limited by process limitations during substrate manufacturing, for example, directly stemming from the ability to align the  
15 features in a given layer to the vertical interconnects, which connect that layer to a top layer and a bottom layer. As described above, ZMV maximizes trace density in all cases for any exposure tool, while SAV can get close to the maximum for specific cases and design rules. However, the drawback with ZMV and SAV approaches is that a trace can be connected to self-aligned or zero-misaligned vias only in one direction (either above or below the trace), hindering the  
20 connection to both layers on the top and bottom without reducing the trace density.

- Accordingly, embodiments described herein improve and address the above limitations by designing, utilizing, and fabricating one or more processes that form a zero-misalignment two-via stack (hereinafter referred to as ZM2VS, with the processes referred to as ZM2VS processes). These embodiments not only address the above limitations encountered by ZMV and  
25 SAV approaches, but also enable multiple applications that maximize line densities for one or more given set of design rules. In addition, embodiments of the ZM2VS enable that the top and bottom zero-misaligned vias to the conductive trace (also referred to as conductive line) in the middle do not have to be co-located along the line and thus the vias may be referred to as “trench” vias (*e.g.*, trench via 511 of Figures 5A – 5C) if needed. For example, the ZM2VS may  
30 include one or more “trench” vias and, as used herein, the “trench” vias may be conductive ZM2VS vias having a length that is at least twice the width of the via. The trench vias may form electrical connections to one or more terminals of a discrete device embedded within the semiconductor package. These trench vias can be exposed to the top surface of the package, or they can be buried within the package and electrically connected to the top or other surface of  
35 the package using ZM2VS vias that contact the trench vias.

Furthermore, the use of ZM2VS processes to form the zero-misaligned vias allows for an increased IO/mm/layer on multiple interconnected layers as well as increased line-density in combination with power-delivery or multi-layer signaling schemes. For example, whereas as a ZMV and SAV may be limited to a trace that can be connected to the ZMV/SAV vias only in one direction, the embodiments set forth below may include pre-aligning a routing layer to vias extending above and below by designing an enhanced photomask. For some embodiments, this enhanced photomask may simultaneously define both the dimensions and placement of the routing layer along with vias extending above and below the routing layer.

In some embodiments, the processes used to fabricate an enhanced photomask (*e.g.*, by fabricating multiple grayscale layers on one mask) are amenable to much more precise alignment, and thus the achievable misalignment is much less. Moreover, since the alignment is only done one time (*i.e.*, during mask fabrication), these embodiments help to replace the alignment costs (*e.g.*, due to reduced throughput) with the marginally increased cost of fabricating the photomask, which is used multiple times over, and may therefore displace the overall cost and maintain cost-efficiency. A corresponding set of processes has been designed to fabricate the resultant structures using a single lithographic exposure step along with several development and plating steps.

According to some embodiments, Figures 1 – 7 illustrate zero-misalignment two-via stacks using a photoimageable dielectric (PID) stack and electrolytic plating. As used herein, a “zero-misalignment two-via stack” (ZM2VS) refers to a routing layer or a conductive trace having zero-misalignment vias (also referred to as ZM2VS vias) that are pre-aligned and extend in both directions to a top layer and a bottom layer – without reducing the trace density. For example, the ZM2VS described herein may be fabricated using a single exposure step to define a zero-misalignment two via stack that simplifies the litho processing for any number of packaging needs, including but not limited to I/O density, routing density improvement, increase in packaging designs, etc. For some embodiments, the zero-misalignment vias as set forth below (*e.g.*, in Figures 1-11) may include (or may be formed with), but is not limited to, electroless copper (Cu), sputtered Cu-bearing titanium alloy (Ti/Cu), tantalum/copper (Ta/Cu) seed layer(s) under the line, traces of thin palladium (Pd) layers in one or more specific/defined places around the via structures, and/or buildup film material surrounding the entire via and line structure. In addition, for some embodiments, the ZM2VS is formed using at least one of a PID material and a buildup film as the dielectric.

Referring now to Figure 1, a perspective view of a conductive trace 110 with zero-misaligned vias 111-112 is illustrated, according to one embodiment. For one embodiment, the conductive trace 110 may be used as a package routing signal line (or trace) that is connected to

a top pad 120 on one end and to a bottom pad (or layer) 121 on the other end (note that the line may eventually be routed all the way to the second-level interconnect (SLI)). For one embodiment, the top pad 120 may be a first level interconnect (FLI) pad connecting a substrate to a die, while the bottom pad may be a SLI pad (note that the SLI pad may be a  
 5 second/subsequent layer or a bottommost layer/plane of the package/substrate).

According to one embodiment, the conductive trace 110 enables connectivity to both pads 120-121 with a maximal number density of connections for one or more given design rules (*e.g.*, a given design rule prescribing a minimum trace width and space width). In addition, as shown in Figure 1, the zero-misaligned via 111 is connected to the conductive trace 110 at one  
 10 end (*e.g.*, shown as a perpendicular junction from a zero-misaligned via to a trace) and at the other end the conductive trace 110 is connected to the zero-misaligned via 112 (*e.g.*, shown as a perpendicular junction from a trace to a zero-misaligned via). Note that the conductive trace 110 with the zero-misaligned vias 111-112 may be formed with one or more different process flows as described in further detail below (*e.g.*, Figures 7 – 10).

In addition, for some embodiments, the formation of the zero-misaligned vias 111-112 to the conductive trace 110 may allow for one or more traces to be parallel (*e.g.*, as shown in Figures 2A) without interfering with a pad at least on one end (*i.e.*, as would be the case if using only ZMVs or SAVs). These embodiments thus enable a semiconductor package to have two or more parallel conductive traces (such as conductive trace 110) in a dense routing configuration  
 20 without requiring a further increase in I/O congestion in a region around a pad. Accordingly, the conductive trace 110 with the zero-misaligned vias 111-112 allows for shorter and more efficient routing, which can lead to better signaling characteristics and to a reduced package form-factor.

Note that the ZM2VS trace/vias may include fewer or additional packaging components based on the desired packaging design.

Figure 2A is a perspective view of one or more conductive traces 210a-b with zero-misaligned vias 211-212, according to one embodiment. Note that the conductive traces 210a-b are similar to the conductive trace 110 of Figure 1, however the one or more conductive trace 210a-b are shown parallel to illustrate a routing and signaling improvement based on the ZM2VS process described herein. Also note that Figure 2A may be omitting one or more components  
 30 (*e.g.*, as shown below in the corresponding Figure 2B) to simplify and not obscure the illustrative implementations.

Referring now to Figure 2A, the conductive trace 210a-b may be formed as straight lines, but the conductive trace 210a-b can have one or more different shapes (*e.g.*, curved, zig-zag, etc.). For one embodiment, the one or more conductive trace 210a are signal traces and the one  
 35 or more conductive trace 210b are ground traces. For one embodiment, the collective one-

dimensional (1D) number density of the conductive traces 210a-b may be the same/equal to that of the zero-misaligned vias 211-212 (or the conductive traces 210a-b have a collective 1D number density that is substantially equal to a 1D number density of the first via 211 and a 1D number density of the second via 212).

5 For one embodiment, the one or more conductive traces 210a-b in a parallel-configuration enable an improved ground shielding for high-speed signals and a high ground-to-signal ratios (*e.g.*, up to 1:1). For example, a conductive trace 210a may be used as a signal trace to connect a FLI layer to a subsequent layer in a substrate (as shown in Figure 2B). For cross-talk minimization, for example, the conductive trace 210a (a signal trace) is surrounded by a  
10 conductive trace 210b (a ground trace), where a ground reference plane(s) may be located either below the traces or both on top and below the traces.

For some embodiments, each of the conductive traces 210a-b is formed with one or more zero-misaligned vias 211-212 on at least one end of the conductive trace 210a-b. The zero-misaligned vias 211-212 may be coupled with a top pad 220 and/or a bottom pad 221. For one  
15 embodiment, the zero-misaligned vias 211-212 may be formed to extend both upward to a top layer and downward to a bottom layer (*e.g.*, shown as a “T” junction where a top zero-misaligned via and a bottom zero-misaligned via have a “T” perpendicular junction from the zero-misaligned vias to a trace). Meanwhile, one or more of the conductive traces 210a-b may have one or zero-misaligned vias 211 and/or 212 on one end and have no vias formed on the  
20 other end.

Note that the conductive traces 210a-b with the zero-misaligned vias 211-212 may be formed with one or more different process flows as described in further detail below (*e.g.*, Figures 7 – 10).

Figure 2B is a corresponding projection view of a semiconductor package 200 having the  
25 one or more conductive traces 210a-b with zero-misaligned vias 211-212, according to one embodiment.

For one embodiment, the semiconductor package 200 has a dielectric layer 240 that includes the one or more conductive traces 210a-b (*e.g.*, as shown in Figure 2A). The one or more conductive traces 210a are signal lines and the one or more conductive traces 210b are  
30 ground lines. For some embodiments, the one or more conductive traces 210a-b are in parallel to enable an improved ground shielding for high-speed signals and a high ground-to-signal ratios (*e.g.*, up to 1:1) in the semiconductor package 200. For example, as shown in the transmission layer 240 of the semiconductor package 200, each of the signal conductive trace 210a is surrounded with at least one or more ground conductive trace 210b, where ground reference  
35 plane 230 and 231 are respectively deposited above the lines 210a-b and/or above and below the

lines 210a-b.

For example, a ground conductive trace 210b has a zero-misaligned via 211 coupled to the top ground plane 230, whereas another ground conductive trace 210b has a zero-misaligned via 212 coupled to the bottom ground plane 231. For one embodiment, the signal conductive trace 210a has a zero-misaligned via 211 coupled to a top pad 220 (*e.g.*, a signal FLI pad), where a solder ball (or bump) 245 is deposited on the top pad 220 of the semiconductor package 200. In addition, one or more of the top ground planes 230 and the bottom ground plane(s) 231 may be coupled to a top pad 219 (*e.g.*, a ground FLI pad), where a solder ball (or bump) 245 is deposited on the top pad 219 of the semiconductor package 200. In some embodiments, the layer 240 has one or more conductive trace 210a that may be used as signal traces to connect a FLI layer to a subsequent layer with the zero-misaligned vias 211 and/or 212 in the semiconductor package 200.

For some embodiments, each of the ground conductive trace 210b may be coupled to at least one of the ground planes 230-231. For one embodiment, each of the ground conductive trace 210b is coupled to both ground planes 230-231, where at least one of the ground conductive trace 210b is coupled to both ground planes 230-231 without misalignment using the zero-misaligned vias 211-212. Note that the conductive trace 210a-b directionality is not restricted to one-specified direction as such the conductive trace 210a-b can follow any directions, according to some embodiments.

Also note that the semiconductor package 200, as shown in Figure 2B, may include fewer or additional packaging components based on the desired packaging design. Figure 3A is a top view of a package 301 with one or more interconnect layers 340-344, according to one embodiment. In addition, Figure 3B is a corresponding cross-sectional view of a portion of a semiconductor device 300 with the package 301 on the A – A' axis, and Figure 3C is a corresponding cross-sectional view of the semiconductor device 300 with the package 301 on the B – B' axis. Figures 3B and 3C provide cross-sectional views that may be useful in showing how the one or more layers of the ZM2VS vias and lines are formed in the package 301 (also referred to as a substrate).

Figures 3A illustrates the package 301 and may omit one or more components for simplicity that may be illustrated in Figures 3B and 3C with projection views of a semiconductor device 300 with the package 301 on the A – A' axis and on the B – B' axis, respectively. Referring now to Figure 3A, the package 301 includes one or more interconnect layers 340-344. For one embodiment, the package 301 may include, but is not limited to, a substrate, a motherboard, and a printed circuit board (PCB). For one embodiment, the package 301 is a PCB. For one embodiment, the PCB is made of an FR-4 glass epoxy base with thin copper foil

laminated on both sides (not shown). For certain embodiments, a multilayer PCB can be used, with pre-impregnated (pre-preg) and copper foil (not shown) used to make additional layers. For example, the multilayer PCB may include one or more dielectric layers, where each dielectric layer can be a photosensitive dielectric layer (not shown). For some embodiments, holes (not shown) may be drilled in the package 301. For one embodiment, the package 301 may also include conductive copper traces, metallic pads, and holes (not shown).

For one embodiment, the one or more interconnect layers 340-344 can be a package layer with at least one of an I/O layer, a power plane, and a ground plane. For example, the interconnect layers 340-344 may include a power plane (*e.g.*, interconnect layer 340), a ground (GND) plane (*e.g.*, interconnect layers 341 and 343), and I/O traces (*e.g.*, interconnect layers 342 and 344) based on the desired architectural implementations.

As described herein, an “interconnect layer” may refer to a conductive layer used for electrical interconnection of circuit components on a substrate (*e.g.*, an integrated circuit). The interconnect layer may include, but is not limited to, a package layer, a power plane, a ground plane, and/or a signal trace (or a conductive trace) on the substrate. For some embodiments, one or more of the interconnect layers on the substrate may be formed with ZM2VS conductive traces/vias (as illustrated in Figures 1 – 2), where the interconnect layer has the ZM2VS vias leading from the interconnect layer to a second interconnect layer above or below that interconnect layer.

The one or more interconnect layers 340-344 may include, but is not limited to, I/O traces, a power delivery routing, traces or planes, and a GND routing, traces or planes. For one embodiment, the interconnect layer 340 can be a power plane, but the interconnect layer 340 can also be one or more power tracks, power routing(s), or a conductive plane (*e.g.*, a metal plane). The interconnect layer 340 may further include one or more vertical ZM2VS (*e.g.*, ZM2VS 334-334 as shown in Figure 3C) to deliver power within the package 301. For one embodiment, the interconnect layer 340 may be located below the other interconnect layers 341-344, and may include a plurality of power planes based on the desired packaging design, where the power planes may span the entirety of the package 301.

For some embodiments, the interconnect layers 341 and 343 may be one or more GND planes, and the interconnect layers 342 and 344 may be one or more I/O signal traces. For example, the interconnect layers 341 and 343 surround the interconnect layers 342 and 344 to shield the interconnect layers 342 and 344 from increased cross-talk. For one embodiment, each of the interconnect layers 340-344 may include one or more ZM2VS traces, vias, and/or pads (*e.g.*, vias on pad 311-312 as shown in Figures 3B and 3C). Note that the pads of the interconnect layers 341-344 may be configured as ZM2VS or vias-on-pads (*e.g.*, vias on pads

312 of Figure 3B).

According to some embodiments, the ZM2VS of the interconnect layers 340-344 may be formed with two stacked vias (*e.g.*, ZM2VS 330-331 of Figures 3B and 333-334 of Figures 3C) that are coupled in both directions (*i.e.*, above and below the interconnect layers). For example,  
5 the ZM2VS of the interconnect layers 340-344 may be used to connect each of the interconnect layers to another conductive layer (*e.g.*, a FLI layer).

Note that the interconnect layers of package 301 may be formed with one or more different process flows as described in further detail below (*e.g.*, Figures 7 – 10). Also note that the package 301, as shown in Figure 3A, may include fewer or additional packaging components  
10 based on the desired packaging design.

Figure 3B is a corresponding projection view of a semiconductor package 300 with the package 301 on the A – A' axis, according to one embodiment. For one embodiment, the semiconductor package 300 may have dies 302-303 coupled to the package 301 using the one or more interconnect layers 340-344. The interconnect layer 340-344 may include one or more  
15 ZM2VS 330-331 to connect the respective interconnect layers in either one or more both directions in the package 301. Note that package 301 illustrates the interconnect layers 340-344, however the package 301 may have fewer or more interconnect layers based on the desired packaging design.

For one embodiment, the semiconductor package 300 includes one or more dies 302-303  
20 disposed on the package 301 coupled by a plurality of solder balls 355 and a plurality of pads 356 (*e.g.*, controlled collapse chip connection (C4) pad layer). Each of the dies 302-303 may include, but is not limited to, a semiconductor die, an integrated circuit, a central processing unit (CPU), a microprocessor, a platform controller hub (PCH), a memory, and a field programmable gate array (FPGA). In addition, the package 301 may include a conductive layer 350 which may  
25 have one or more metals structures (*e.g.*, interconnects and/or routing on a pad layer). Note that the conductive layer 350 may be optional and thus may be added/omitted based on the desired packaging design.

For some embodiments, the semiconductor package 300 includes one or more interconnect layers 340-344 that may be sacrificed for (or implemented with) a vertical  
30 connection without necessitating a pad in the high-density layer of the semiconductor package 300 – which significantly reduces the trace density of the respective interconnect layer. Furthermore, as shown in Figure 3B, the one or more ZM2VS 330-331 facilitate vertical connections that couple one or more interconnect layers to the FLI pads 356 of the package 301 located above the high-density layers.

35 As shown in Figure 3B, each of the interconnect layers 340-344 may have one or more

ZM2VS. For example, the interconnect layer 341 may include the ZM2VS 330-331 formed within the package 301, where the first ZM2VS 330 is disposed above the second ZM2VS 331. Likewise, each of the interconnect layers 342-343 have at least one ZM2VS 330. For one embodiment, one or more of the first ZM2VS 330 may couple a via on pad 312 of a given  
5 interconnect layer to a pad 356 (*e.g.*, a C4 pad layer).

Accordingly, one of the advantages of these embodiments of the semiconductor package 300 is that for a connection to be enabled between only a power plane (*e.g.*, package layer 340) and the die (*e.g.*, die 302), a single I/O conductive trace needs to be removed at minimum (min) line (or width) and space (also referred to as min line/space). For example, typically if in an 8  
10 row deep I/O every 8<sup>th</sup> line is removed, the I/O density drops typically by only 12.5%. However, for one embodiment, when one or more ZM2VS vias 312 on pads are implemented on the package 301 for a min line/space of 2/2  $\mu\text{m}$ , the reduction in I/O density of the package 301 may be roughly between 37.5 – 50% (or even higher) based on, for example, the exposure tool alignment capability. Accordingly, the reduction in I/O density of the semiconductor package  
15 300 may necessitate an added/improved and unclear solution to return the total I/O count that is needed.

Note that the semiconductor package 300, as shown in Figure 3B, may include fewer or additional packaging components based on the desired packaging design.

Figure 3C is a corresponding projection view of a semiconductor package 300 with the package 301 on the B – B' axis, according to one embodiment. For one embodiment, the  
20 semiconductor package 300 may have dies 302-303 coupled to the package 301 using the one or more interconnect layers (*e.g.*, interconnect layers 340-341, and 343). The interconnect layers 340-341 and 343 may include one or more ZM2VS 333-334 to connect the respective interconnect layers in either one or more both directions in the package 301.

For one embodiment, the semiconductor package 300 includes one or more dies 302-303  
25 disposed on the package 301 coupled by a plurality of solder balls 355 and a plurality of pads 356 (*e.g.*, C4 pad layer). For some embodiments, the semiconductor package 300 includes the power interconnect layer 340 and the ground interconnect layers 341 and 343. Furthermore, as shown in Figure 3C, the one or more ZM2VS 330-331 facilitate vertical connections that couple  
30 one or more interconnect layers to the FLI pads 356 of the package 301 located above the high-density layers.

As shown in Figure 3C, each of the interconnect layers 340-341 and 343 may have one or more ZM2VS 333-334. For example, the interconnect layer 340 may include the ZM2VS 333-334 formed within the package 301, where the first ZM2VS 334 is disposed above the second  
35 ZM2VS 333. For one embodiment, one or more of the first ZM2VS 334 may couple a via on pad

312 of a given interconnect layer to a pad 356 (e.g., a C4 pad layer). Likewise, the second ZM2VS 333 may have a via on pad 311 of a given interconnect layer (e.g., interconnect layer 340) to, for example, a pad 312 on the GND layer. The interconnect layer 340 has ZM2VS 333-334 connecting the bottom power plane to the top layer (e.g., the C4 pad layer 356). Likewise, the interconnect layers 341 and 343 has ZM2VS 333-334 connecting both ground planes to the top layer (e.g., the C4 pad layer 356).

Note that the interconnect layers 340-344 of Figures 3A – 3C may have directionality that is not restricted to one-specified direction as such the conductive traces can follow any directions, according to some embodiments. Also note that the semiconductor package 300, as shown in Figure 3C, may include fewer or additional packaging components based on the desired packaging design.

Figure 4A is a top view of a package 401 with one or more interconnect layers 442 and 444, according to one embodiment. In addition, Figure 4B is a corresponding cross-sectional view of a portion of a semiconductor device 400 with the package 401 on the A – A' axis, and Figure 4C is a corresponding cross-sectional view of the semiconductor device 400 with the package 401 on the B – B' axis. Figures 4B and 4C provide cross-sectional views that may be useful in showing how the one or more layers of the ZM2VS vias and lines are formed in the package 401.

Figures 4A illustrates the package 401 and may omit one or more components for simplicity that may be illustrated in Figures 4B and 4C with projection views of a portion of a semiconductor device 400 with the package 401. Furthermore, Figures 4A – 4C show the package 401 that is similar to the package 301 of Figures 3A – 3C.

Referring now to Figure 4A, the package 401 includes one or more interconnect layers 442 and 444. For one embodiment, the package 401 may include, but is not limited to, a substrate, a motherboard, and a PCB. For one embodiment, the one or more interconnect layers 442 and 444 can be a package layer with at least one of an I/O layer, trace, and via. For example, the interconnect layer 444 may include a first signal layer and the interconnect layer 442 may include a second signal layer based on the desired architectural implementations. For one embodiment, the interconnect layer 442 on the package 401 may be formed with ZM2VS conductive traces/vias (as illustrated in Figures 1 – 3), where the interconnect layer 442 has the ZM2VS vias leading from the interconnect layer to a second interconnect layer above or below that interconnect layer. Meanwhile, the interconnect layer 444 may be formed with one or more ZMVs and/or zero-misaligned traces (ZMTs).

For some embodiments, the interconnect layers 442 and 444 are I/O signal traces that may be surrounded by one or more interconnect layers (i.e., GND planes) (not shown) to shield

the interconnect layers 442 and 444 from increased cross-talk. For one embodiment, at least one of the interconnect layers 442 and 444 may include at least one or more of ZM2VS traces, vias, and pads. Note that the pads of the interconnect layers 442 and 444 may be configured as ZM2VS or vias-on-pads.

5           Note that the interconnect layers 442 and 444 of package 401 may be formed with one or more different process flows as described in further detail below (*e.g.*, Figures 7 – 10). Also note that the package 401, as shown in Figure 4A, may include fewer or additional packaging components based on the desired packaging design.

10           Figure 4B is a corresponding projection view of a semiconductor package 400 with the package 401 on the A – A' axis, according to one embodiment. For one embodiment, the semiconductor package 400 may have dies 402-403 coupled to the package 401 using the one or more interconnect layers 442 and 444. The interconnect layer 444 may include one or more ZMVs (or ZMTs) to connect the interconnect layer 444 in either one or more both directions in the package 401. Note that package 401 illustrates the interconnect layer 444 (as shown in Figure  
15 4B), however the package 401 may have fewer or more interconnect layers based on the desired packaging design.

For one embodiment, the semiconductor package 400 includes one or more dies 402-403 disposed on the package 401 coupled by a plurality of solder balls 455 and a plurality of pads 456. Each of the dies 402-403 may include, but is not limited to, a semiconductor die, an  
20 integrated circuit, a central processing unit (CPU), a microprocessor, a platform controller hub (PCH), a memory, and a field programmable gate array (FPGA). As shown in Figure 4B, the interconnect layer 444 may use one or more ZMVs and/or conductive traces to connect die 403 to 402 with the pads 456 and solder bumps 455.

In addition, the interconnect layer 444 may be similar to the ZMVs and conductive traces  
25 of Figures 1-3. The interconnect layers may be implemented for high-density I/O block assembly while maintaining equal length lines for one or more different I/O layers (*e.g.*, as shown in Figures 4A – 4C). Note that the interconnect layers (*e.g.*, as shown in Figures 4A – 4C) can entail a lateral growth of the I/O layer, but any possible timing issue(s) that may arise between I/O layers can be minimized. Also note that the semiconductor package 400, as shown in Figure  
30 4B, may include fewer or additional packaging components based on the desired packaging design.

Figure 4C is a corresponding projection view of a semiconductor package 400 with the package 401 on the B – B' axis, according to one embodiment. For one embodiment, the interconnect layer 442 may include a ZM2VS (as described herein) to connect the respective  
35 interconnect layer 442 in either one or more both directions in the package 401. According to

one embodiment, the interconnect layer 442 may be disposed (or formed) below the interconnect layer 444 (not shown). For one embodiment, the interconnect layer 442 has the ZM2VS connecting the bottom (second) signal layer to the top layer (*e.g.*, the C4 pad layer 456). In addition, one of the advantages of these embodiments is that the interconnect layer 442 can connect through one layer with minimal change to the I/O density (*e.g.*, the I/O density may drop by roughly a factor of 2).

Note that the interconnect layers 442 and 444 of Figures 4A-4C may have directionality that is not restricted to one-specified direction as such the conductive traces can follow any directions, according to some embodiments. Also note that the semiconductor package 400, as shown in Figure 4C, may include fewer or additional packaging components based on the desired packaging design.

Figure 5A is a perspective view of a conductive shield 500 with one or more conductive trace 510a-b with vias 511-512 (or ZM2VS vias), according to one embodiment. Note that, as described above and based on the package design of the conductive shield 500, the vias 511-512 may be used as (or to form) trench vias. Figures 5B and 5C are corresponding cross-sectional views of the conductive shield 500, according to some embodiments. Note that the conductive trace 510a-b may be similar to the conductive trace of Figures 1-4 – in particular similar to the conductive trace of Figure 2A – however the one or more conductive trace 510a-b may be implemented for improved cross-talk reduction and data-rate increase. For example, the conductive trace to via and/or ZM2VS as shown in Figure 2A may be used to further convert the vias in at least one direction into vias (*e.g.*, vias 511-512) that enable reduced cross-talk and increased data-rate.

Referring now to Figure 5A, the conductive trace 510a-b may be formed as straight lines, but the conductive trace 510a-b can have one or more different shapes (*e.g.*, coaxial, zig-zag, etc.). For one embodiment, the conductive trace 510a is a signal line and the one or more conductive trace 510b are ground lines. Using the one or more conductive trace 510a-b in parallel enables an improved ground shielding for high-speed signals and a high ground-to-signal ratios (*e.g.*, up to 1:1). For example, a conductive trace 510a may be used as a signal line to connect a FLI layer (not shown) to a subsequent layer (not shown) in the conductive shield 500. For cross-talk minimization, the conductive trace 510a is surrounded by the ground lines 510b, where a ground reference plane(s) may be located either below the traces or both on top and below the traces. For example, the conductive shield 500 has the ground lines 510b connected to a top ground plane 531 with trench vias 511, where one of the ground lines 510b has a trench via 512 that may be used to connect to a bottom layer (not shown). In addition, the conductive shield 500 has the signal line 510a connected to a trench via 530 that extends upward to a top layer (not

shown).

For some embodiments, each of the ground lines 510b is formed with one or more vias 511 (also referred to as trench vias) on at least one end of each ground lines 510b. The vias 511 may be coupled with the top ground plane 531. In addition, the ground lines 510b may also be  
5 formed with one or more vias 512 on the other end of the ground lines 510b. The vias 512 may be coupled with a bottom pad/layer (not shown). For one embodiment, the vias 511-512 are deposited on one or more of the ground lines 510b to extend upward on one end to a top GND layer 530 and to extend downward on the opposite end to a bottom layer (*i.e.*, shown as a “L” junction where a top ZM2VS via and a trench ground line have a perpendicular junction to form  
10 a ZM2VS via to a line on one end, and the line to a bottom ZM2VS via on the other end). Note that the conductive traces 510a-b with the vias 511-512 and 530 may be formed with one or more different process flows as described in further detail below (*e.g.*, Figures 7 – 10).

According to an additional embodiment, the use of trench vias to extend the thickness of conductive trace may also be utilized to form coaxial conductive trace within a package  
15 substrate. Such an embodiment is illustrated in Figures 5A – 5C. Figures 5A – 5C only illustrate the conductive features within the package, and the dielectric layers are omitted to not unnecessarily obscure particular embodiments.

Note that the conductive shield (and package) 500 may include fewer or additional packaging components based on the desired packaging design.

20 Referring now to Figures 5B and 5C. Figure 5B is a corresponding cross-sectional view of the conductive shield 500 on the A – A’ axis, and Figure 5C is a corresponding cross-sectional view of the conductive shield 500 on the B – B’ axis. Figures 5B and 5C provide cross-sectional views that may be useful in showing how the one or more layers of the ZM2VS vias and lines are formed around the conductive shield 500.

25 As illustrated in Figure 5B, the one or more conductive traces 510a-b may be formed as zero-misalignment two via stacks using a PID (and/or a buildup film dielectric) and electrolytic plating (as the process flows of forming the ZM2VS lines/vias are described in further detail below in Figures 7-10). For one embodiment, the one or more ground lines 510b may be formed with a width that is substantially equal to the sidewalls (*i.e.*, the ZM2VS vias 511 extending  
30 upward to the top ground plane 531) that are formed along opposite edges of the conductive shield 500. For another embodiment, the conductive trace 510a may be formed with a width that is substantially equal to the ZM2VS via 530.

For one embodiment, the ground conductive trace 510b are coupled with the trench vias 511 as the trench vias 511 extend upward connecting to the top GND plane 531 (*i.e.*, forming a  
35 conductive shield 500 having two “T-shaped” grounding sidewalls surrounding the “I-shaped”

signal conductive trace/via based on the A – A' axis). Meanwhile, as shown in Figure 5C, the ground lines 510b are coupled with the trench vias 511 that connect upward to the top ground plane 531 (without a separation in the top GND plane as shown on Figure 5B), which surrounds the signal conductive trace 510a (*i.e.*, forming a conductive shield 500 having semi-coaxial shape with the ground lines/vias/plane that surround the conductive trace based on the B – B' axis).

For one embodiment, the conductive trace 510a-b may be separated from the top GND plane 531 by a single dielectric layer. However, it is to be appreciated that the top GND plane 531 may have more than one layer of dielectric material separating the plane 531 from the transmission/trench lines 510a-b. In such embodiments, the sidewalls and conductive trace 510a-b of the conductive shield 500 may have one or more ZM2VS vias deposited above and/or below the ZM2VS conductive trace/vias 510a-b, respectively.

According to an alternative embodiment, a plurality of conductive trace may be formed in a single conductive shield 500. For example, a twin-axial conductive trace may be formed within the conductive shield 500, where a first conductive trace and a second conductive trace may be surrounded by the ground conductive traces 510b. Such a device may be beneficial when a differential signal with low interference is needed. Furthermore, it is to be appreciated that other types of trace(s)/line(s) may be formed within a conductive shield. For example, entire byte groups or busses may be implemented within a coaxial configuration that is made possible with lithographically defined line vias, according to embodiments of the invention.

Also note, as described above in Figures 2A and 2B, one or more conductive traces are also not limited to passing a signal along a single layer of dielectric material (*e.g.*, a PID material and/or a buildup film). For example, a conductive trace (*e.g.*, conductive traces 510a-b) that includes one or more junctions with one or more ZM2VS vias that allow for the conductive trace to travel along the plane of the one or more dielectric layers (not shown) and pass through one or more dielectric layers (not shown) in one or both vertical directions (to a top and/or a bottom layer) with the ZM2VS via(s) (*e.g.*, ZM2VS vias 511-512). At the junction(s) where the conductive trace transitions to being routed through dielectric layers in the vertical direction, embodiments of the invention may include one or more ZM2VS line vias and/or pads that also extend through the dielectric layers.

In addition, while the illustrated embodiment includes one line via for each conductive trace (in the vertical direction), it is to be appreciated that more line vias may be included if the conductive trace continues in the vertical direction (in both the upward and/or downward directions) through additional dielectric layers, or fewer line vias may be needed if the conductive trace passes through fewer dielectric layers.

Those skilled in the art may also recognize that the trench lines (or the intermediate wall lines) and pads that are formed on the same dielectric level may be formed as a single continuous feature that are connected to each other out of the plane, and therefore, may be referred to with the same reference numeral. According to another embodiment, the ZM2VS line vias that are  
5 formed through the same dielectric layers may also be one or more ZM2VS line vias that are connected out of the plane and may be formed as a single continuous feature.

Additionally, it is to be appreciated that as the ZM2VS line vias are formed with a zero-misalignment two via stack using PID (and/or a buildup stack) and electrolytic plating process, the one or more intermediate wall lines may be omitted. In addition to some embodiments that  
10 have a coaxial transmission line passing through multiple layers of the package substrate, other embodiments may also include a conductive trace that is surrounded by a conductive shield in some portions of the package and is a strip-line conductive trace without a conductive shield in other portions of the package. According to an embodiment, the vertical ZM2VS vias and sidewalls may have any desired shape, such as circular or elliptical, and are not limited to  
15 rectangular shapes.

Figure 6A is a perspective view of a conductive shield 600 having a coaxial waveguide with flat walls using ZM2VS and trench vias 610a-b and one or more layers/planes 631 and 633, according to one embodiment. Figures 6B and 6C are corresponding cross-sectional views of the conductive shield 600, according to some embodiments. Note that the trench lines 610a-b may  
20 be similar to the transmission lines of Figures 1-5 – in particular similar to the transmission/trench lines of Figures 2 and 5 – however both the top and bottom ground connections (*e.g.*, ground layers 631 and 633, respectively) have been extended to the trench vias 610b creating a near-perfect rectangular coaxial waveguide for minimal losses and maximal I/O bandwidth. These embodiment, as shown in Figures 6A – 6C, provide several advantages as the  
25 walls have a near-perfect alignment needed to reach top bandwidths at minimal losses compared to the typical (or currently pursued) waveguides where the walls around the signal are not smooth and equidistant due to alignment requirements.

Referring now to Figure 6A, the conductive traces 610a-b may be formed as straight lines, but the conductive traces 610a-b can have one or more different shapes. For one  
30 embodiment, the conductive trace 610a is a signal line and the one or more conductive traces 610b are ground lines. Using the one or more conductive traces 610a-b in parallel enables an improved ground shielding for high-speed signals and a high ground-to-signal ratios (*e.g.*, up to 1:1). For example, the signal line 610a may be used with vias 630 and 632 to connect a top layer (not shown) in the conductive shield 600. For cross-talk minimization, the signal line 610a is  
35 surrounded by the ground lines 610b, where a top ground layer 631 is deposited above the trench

lines/vias 610a-b and a bottom ground layer 633 is deposited below the trench lines/vias 610a-b. For example, the conductive shield 600 has the ground lines/vias 610b connected to both the top ground layer 631 and the bottom ground layer 633, forming a near-perfect rectangular coaxial waveguide (or intermediate walls) between both layers 631 and 633.

5           According to an additional embodiment, the use of trench vias to extend the thickness of transmission lines may also be utilized to form coaxial conductive traces within a package substrate. Such an embodiment is illustrated in Figures 6A – 6C. Figures 6A – 6C only illustrate the conductive features within the package, and the dielectric layers are omitted to not unnecessarily obscure particular embodiments.

10           A coaxial conductive trace is formed by surrounding a conductive trace 610a with a conductive shield 600. According to one embodiment, the conductive shield 600 include the lower layer 633 that is coupled to the top layer 631 by one or more layers of trench lines/vias 610b that serve as sidewalls for the conductive shield 600, where the shield 600 may be held at ground potential. Accordingly, the conductive trace 610a and vias 630 and 632 are formed  
15           within the conductive shield 600 to transmit data with cross-talk reduction and data-rate increase with neighboring lines outside of the conductive shield 600.

          Note that the conductive shield (and package) 600 may include fewer or additional packaging components based on the desired packaging design.

          Referring now to Figures 6B and 6C. Figure 6B is a corresponding cross-sectional view  
20           of the conductive shield 600 on the A – A' axis, and Figure 6C is a corresponding cross-sectional view of the conductive shield 600 on the B – B' axis. Figures 6B and 6C provide cross-sectional views that may be useful in showing how the one or more layers of the ZM2VS trench lines/vias 610a-b with the top and bottom layers 631 and 633 are deposited in the conductive shield 600. Note that the formation of the walls of the conductive shield 600 are similar to the walls  
25           described in detail above in Figures 5A-5C.

          As illustrated in Figure 6B, the one or more conductive traces 610a-b may be formed as zero-misalignment two via stacks using a PID (and/or a buildup film dielectric) and electrolytic plating (as the process flows of forming the ZM2VS lines/vias are described in further detail below in Figures 7-10). For one embodiment, the one or more ground trench line/via 610b may  
30           be formed with a width that is substantially equal to the sidewalls connecting to the top and bottom layers 631 and 633 that are formed along opposite edges of the conductive shield 600. For another embodiment, the conductive trace 610a may be formed with a width that is substantially equal to the ZM2VS vias 630 and 632 extending upwards along the opposite edges of the conductive trace 610a.

35           For one embodiment, the ground trench lines 610b are coupled with the sidewalls of the

conductive shield 600 as the ground trench lines/vias 610b are connected to the top layer 631 and the bottom layer 633. Note, as shown on the A – A' axis, the top layer 631 has an opening for the transmission via 630 that is coupled to the conductive trace 610a. Meanwhile, as shown in Figure 6C, the ground trench lines 610b are coupled with the sidewalls of the conductive shield 600 as the ground trench lines/vias 610b are connected to the top layer 631 and the bottom layer 633 (without a separation in either the top and bottom layers), which surrounds the signal conductive trace 610a (*i.e.*, forming a conductive shield 500 having a coaxial waveguide with the ground lines/vias/plane surrounding the conductive trace based on the B – B' axis).

For one embodiment, the conductive traces 610a-b may be separated from the top layer 631 and the bottom layer 633 by a single dielectric layer. However, it is to be appreciated that the top layer 631 and the bottom layer 633 may have more than one layer of dielectric material separating the either layers 631 and 633 from the conductive traces 610a-b. In such embodiments, the sidewalls and conductive traces 610a-b of the conductive shield 600 may have one or more ZM2VS vias deposited above and below the ZM2VS conductive traces/vias 610a-b, respectively.

Additionally, it is to be appreciated that as the ZM2VS trench lines/vias are formed with a zero-misalignment two via stack using PID (and/or a buildup stack) and electrolytic plating process, the one or more intermediate wall lines may be omitted. In addition to some embodiments that have a coaxial conductive trace passing through multiple layers of the package substrate, other embodiments may also include a conductive trace that is surrounded by a conductive shield in some portions of the package and is a strip-line conductive trace without a conductive shield in other portions of the package. According to an embodiment, the vertical ZM2VS vias and sidewalls may have any desired shape, such as circular or elliptical, and are not limited to rectangular shapes.

Figures 7A – 7M are a process flow illustrating a method of forming a zero-misalignment two via stack (ZM2VS) using a PID stack and electrolytic plating, according to some embodiments. These embodiments as shown with respect to Figures 7A – 7M provide a single patterning step to develop a ZM2VS that improves (and simplifies) the litho patterning processing for any desired packaging needs, including, but not limited to, I/O density reduction, routing density improvement, and increased packaging designs. The ZM2VS formed with the process flow of Figures 7A – 7M is similar to (and may be used as) the ZM2VS conductive traces/vias illustrated in Figures 1 – 6, when the packaging design needs a PID stack and electrolytic plating process.

One such embodiment is illustrated and described based on Figures 7A – 7M, which illustrates cross-sectional views of a package layer used to form the ZM2VS. In the illustrated

embodiments, the formation of the ZM2VS is shown, however it is to be appreciated that additional features, such as additional lines, vias, and/or pads, may be formed at the same time and with the same processing operations, according to the embodiments described herein.

Referring now to Figure 7A, embodiments of the process flow include a conductive layer 730 (or an initial top metal layer) deposited above a dielectric layer 705, where the conductive layer 730 has one or more pads deposited on the dielectric layer 705. For one embodiment, the package layer of Figure 7A illustrates at least one interconnect layer that has the conductive layer 730 and the dielectric layer 705. According to one embodiment, this package layer is shown with the conductive layer 730 that has existing pads, vias, and traces. For example, the conductive layer 730 may facilitate the foundation of the zero-misalignment two via stack. In one embodiment, the dielectric layer 705 may include, but is not limited to, a buildup film (BF) and/or a PID layer. The dielectric layer 705 may be deposited over one or more metal traces and pads of the conductive layer 730. According to some embodiments, several of the advantages of using PID materials to form the dielectric layer(s) is the reduction of assembly steps (*i.e.*, a single patterning step of a PID layer to form the ZM2VS as shown below) and their ease of processing (*i.e.*, exposure and subsequent develop to create any structure as defined by a mask). In contrast, using a BF as the dielectric layer may require reactive-ion etching (RIE) or other physical etching methods to be patterned/removed (*i.e.*, processes/tools may not be readily available in current panel-level manufacturing).

By way of example, as described above, the dielectric layer 705 may be a polymer material, such as a polyimide, an epoxy or a BF. In one embodiment, the dielectric layer 705 may be one layer in a stack that includes a plurality of dielectric layers used to form a build-up structure. As such, the dielectric layer 705 may be formed over another dielectric layer. Additional embodiments may include forming the dielectric layer 705 as the first dielectric layer over, for example, a core material on which the stack is formed.

Referring now to Figure 7B, according to some embodiments, a PID layer 715 (or a PID lamination) is deposited above and around the conductive layer 730, and then a seed layer 735 is deposited (*e.g.*, sputtered) on the PID layer 715. For one embodiment, the PID layer 715 may be deposited with a lamination, spray coating, spin coating, or other known deposition methods. For one embodiment, the seed layer 735 may not be transparent to any light, for example, from any light source of any lithography exposure tool. The seed layer 735 may include sputtered Cu, Ti/Cu, Ta/Cu, tungsten (W)/Cu, and the like, such as, where Ti, Ta, W may facilitate the adhesion layers as well as barriers. Note the seed layer, as described herein, may have a gradient between one or more regions of the seed layer. Note that, based on the process flow described in Figures 7A – 7M, the seed layer 735 uses an electrolytic plating process to be deposited on the

PID layer 715. According to an additional embodiment, the seed layer 735 may include palladium (Pd) seed clusters/layers at specified regions (*e.g.*, the seed layer at certain location may be less than roughly one or a few atomic layers thick, for example, less than 10 nm layers thick).

5 Referring now to Figure 7C, a resist layer 725 is deposited (or deposited) on the seed layer 735. For example, the resist layer 725 may be laminated when using a dry resist material or slit-coated when using a liquid resist material. For one embodiment, the resist layer 725 is a dose sensitive resist that can be chemically amplified. For additional embodiments, the resist layer 725 may be positive tone, but may also be negative tone. As such, the resist layer 725 may be  
10 exposed with a mask 780 (*e.g.*, a multi-tone mask) that has one or more intensity regions 781-783 (note that the mask can be implemented with a specified number intensity regions based on the desired packaging design and/or the desired patterning for a ZM2VS line/via).

For example, the one or more intensity regions 781-783 of the mask 780 may include four intensity regions, such as a dark region (shown as dark blocks on the mask 780), a light  
15 region 781, a first gray region 782, and a second gray region 783, where for example the second gray region 783 may be darker (and thus allows less light exposure) than the first gray region 782. Accordingly, exposing light through mask 780 (*e.g.*, to a light source, a radiation source, a mercury arc, etc.) adequately transfers image onto resist layer 725 to produce one or more dose levels shown as 725a-c. For one embodiment, each of the dose levels 725a-c has an individual  
20 development-time requirement based on the level of exposure (*e.g.*, the highest dose exposure usually has the fastest/shortest development time, and so on). After the exposure of the mask 780 on the resist layer 725, the resist layer 725 is now imprinted with a first region 725a that has a highest dose and a faster/shorter development time, a second region 725b that has a medium dose and a slower development time, and a third region 725c that has a lowest dose and a  
25 slowest development time. Note that the unexposed regions of the resist layer are labelled 725, *e.g.*, the unexposed regions are on opposite ends/edges of the resist layer 725 as shown in one embodiment. For other embodiments, a resist layer may have less than three or more than three dose levels printed on the resist layer. Also note that one or more features may have been omitted or simplified in order to not obscure the illustrative implementations.

30 Referring now to Figure 7D, for one embodiment, a first develop step (also referred to as a fast/shortest development step) removes only the resist region exposed with the highest dose from layer 725. As such, after the first development on the resist layer 725, the first region 725a is removed from the resist layer 725, where the resist layer 725 is thus patterned to provide an opening to expose a portion of the seed layer 735 for the formation of a ZM2VS via (*e.g.*,  
35 ZM2VS via 712 as shown in Figure 7I).

Referring now to Figure 7E, the exposed portion of the seed layer 735 is then etched and thus subsequently exposing a portion of the PID layer 715. According to one embodiment, the exposed portion of the seed layer 735 may be removed with a seed etching process. Referring now to Figure 7F, a flood exposure 790 is implemented on the resist layer 725 and the exposed region of the PID layer 715. For one embodiment, the flood exposure 790 may use an intransparent seed as a mask (not shown) to expose only the portion of the PID layer 715, where the seed layer 735 has been removed. For example, in order to avoid further exposure of the resist layer 725 as the PID layer 715 is exposed, the PID layer 715 may need to be either a lot more sensitive than the resist layer 725 (*i.e.*, requiring a very low dose to become developable) or sensitive to another wavelength. It is to be understood that multiple exposure tools, especially in panel-level manufacturing, are equipped or can be upgraded to allow for exposure with one or more different wavelengths (*e.g.*, between 365nm and 403nm).

Referring now to Figure 7G, after the flood exposure 790, the exposed region of the PID layer 715 is developed (or patterned) to provide a via opening 740 that exposes a top surface of the conductive layer 730. For one embodiment, the developed region of the PID layer 715 forms the bottom via opening 740 to the existing conductive layer 730. Referring now to Figure 7H, a second develop step (also referred to as a slower development step) is exposed on the resist layer 725 to remove the resist region exposed with the medium dose (or 2nd highest dose). As such, after the second develop exposure on the resist layer 725, the second region 725b is removed from the resist layer 725, and thus the resist layer 725 is patterned to provide a via opening 740 to expose a portion of the seed layer 735 for the formation of a ZM2VS via (*e.g.*, ZM2VS via 711 as shown in Figure 7I). In one embodiment, region 715a (exposed with broadband light) and 725b can be simultaneously develop out to provide a via opening 740 exposing portions of both conductive pad 730 and seed layer 735 for the formation of ZM2VS vias.

Referring now to Figure 7I, a second seed layer 736 may be deposited on both of the via openings 740. For example, the second seed layer 736 is deposited on the exposed top surface of the conductive layer 730 and the exposed portion of the seed layer 735. For one embodiment, the second seed layer is a Pd seed layer and/or any other catalytic metal(s) that may be similar to a Pd material(s). Accordingly, a conductive material (*e.g.*, Cu or the like) is electrolytically grown on the via openings 740 and above the second seed layers 736 to form one or more ZM2VS vias 711 and 712. For one embodiment, the ZM2VS vias 711-712 may be formed/plated using an electroless (e-less) plating process or the like and electrically coupled to the first seed layer 735. Note that the top surface of the bottom via 712 may be deposited above and/or below the seed layer 735 (or on the same level/layer as the seed layer 735). Note that a second seed layer may not be needed to electrolytically plate metal simultaneously and directly on both conductive

layers 730 and 735.

Referring now to Figure 7J, a third develop step (also referred to as a longest/slowest development step) is exposed on the resist layer 725 to remove the resist region exposed with the lowest dose. As such, after the third develop process on the resist layer 725, the third region 725c is removed from the resist layer 725, and thus the resist layer 725 is patterned to provide a line opening 750 to expose a portion of the seed layer 735 for the formation of a ZM2VS line/trace (e.g., ZM2VS line 710 as shown in Figure 7K). For example, after the e-less plating step of the ZM2VS vias 711-712, the third region 725c is developed away (*i.e.*, this resist region has the longest development time) to expose the ZM2VS vias 711-712 and the seed layer 735.

Referring now to Figure 7K, the conductive material is deposited above and around the line opening 750 and the ZM2VS vias 711-712 to form the ZM2VS line 710. After depositing the conductive material, the ZM2VS top via 711 is now finalized. For one embodiment, the ZM2VS line 710 may be formed using the electrolytic plating process. Note that the top via 711 (or the bottom via) may have a slanted edge (or similar tapered shape) coupled to the line 710.

Referring now to Figure 7L, the resist layer 725 is stripped and the remaining portions of the seed layer 735 are removed. According to one embodiment, the seed layer 735 may be removed with a seed etching process. For one embodiment, the ZM2VS line/vias 710-712 are formed prior to the formation of a second dielectric layer. Such embodiments of the invention may be referred to as a line via first litho process.

As such, after the removal, the package layer (or device package) has formed the ZM2VS line via using a PID stack and electrolytic plating, as described herein. For some embodiments, the ZM2VS line via includes a dielectric 715 (e.g., the PID layer) on a conductive pad 730 (or the conductive layer, trace, line/via), a first via 712 extends vertically through the dielectric 715 to a first seed layer 736 (e.g., the Pd seed layer deposited on the exposed conductive pad) on a top surface of the conductive pad 730, a conductive trace 710 on the dielectric 715, and a second via 711 on a second seed layer 736 (note that the first and second seed layers 736 may be formed with the same layer and/or materials), the second seed layer 736 is on/above the dielectric 715, where the conductive trace 710 connects (or electrically couples) to the first via 712 and the second via 711, and where the second via 711 connects to an edge of the conductive trace 710 that is opposite from the first via 712 (*i.e.*, each of the vias are formed on opposite edges of the conductive trace). Accordingly, the conductive trace 710 may connect to both a top layer (not shown) with the top via 711 and a bottom layer (or the conductive pad 730) with the bottom via 712 without reducing the line density of the line/vias 710-712, where each of the line/vias have substantially the same (or equal) line densities (*i.e.*, the conductive trace 710 can be connected to the zero-misaligned vias 711-712 in both directions (above and/or below the conductive trace

710)). Note that the vias may be formed in both directions, the same directions, one direction, etc. (e.g., as shown in Figure 2A, the vias may be formed in one or more directions, including a “T” shaped line/vias coupled in both directions to a bottom and a top surface).

For an additional embodiment, a die (e.g., die 302 as shown in Figure 3B) may be disposed (or coupled) on a FLI pad (e.g., FLI package layer 345 as shown in Figure 3B), wherein the FLI pad connects (or electrically coupled) to a second via (e.g., via 711 of Figure 7 of Figures 7L and 7M), while an interconnect package layer (e.g., interconnect package layer 340 of Figure 3B) may be deposited on a SLI pad, wherein the SLI pad connects to a first via (e.g., via 712 of Figure 7 of Figures 7L and 7M).

Referring now to Figure 7M, a second dielectric layer 716 is deposited over the exposed ZM2VS vias 711-712 and ZM2VS conductive trace 710. For one embodiment, the second dielectric layer 716 (e.g., a PID or a BF layer) may be formed with any suitable process, such as lamination, spray or spin coating and curing. For one embodiment, the second dielectric layer 716 is formed to a thickness that may entirely cover a top surface 721 of the ZM2VS via 711. For example, as opposed to layer formation on crystalline structures (e.g., silicon substrates), each of the dielectric layers may not be highly uniform. Accordingly, the second dielectric layer 716 may be formed to a thickness that is greater than the ZM2VS via 711 to ensure that the proper thickness is reached across the entire substrate. When the second dielectric layer 716 is formed above the ZM2VS via 711, a via reveal process (or a controlled etching process) may be used to expose the top surface 721 of the via 711, as illustrated in Figure 7M. The via reveal process may include mechanical or chemical-mechanical polishing/removing.

In one embodiment, the dielectric removal process may include a wet etch, a dry etch (e.g., a plasma etch), a wet blast, or a laser ablation (e.g., by using excimer laser). According to one additional embodiment, the depth controlled dielectric removal process may be performed only proximate to the ZM2VS via 711. For example, laser ablation of the second dielectric layer 716 may be localized proximate to the location of the via 711. In some embodiments, the thickness of the second dielectric layer 716 may be minimized in order to reduce the etching time required to expose the via 711. In alternative embodiments, when the thickness of the dielectric can be well controlled, the via 711 may extend above the top surface of the second dielectric layer 716 and the controlled dielectric removal process may be omitted.

Note that the zero-misalignment two via stack formed with the process flow of Figures 7A – 7M may include fewer or additional steps and/or packaging components based on the desired packaging design.

Figures 8A – 8K are a process flow illustrating a method of forming a zero-misalignment two via stack (ZM2VS) using a buildup stack and electrolytic plating, according to some

embodiments. These embodiments as shown with respect to Figures 8A – 8K provide an additional single patterning step to develop a ZM2VS that improves (and simplifies) the litho patterning processing for any desired packaging needs, including, but not limited to, I/O density reduction, routing density improvement, and increased packaging designs. The ZM2VS formed with the process flow of Figures 8A – 8K is similar to the ZM2VS conductive traces/vias illustrated in Figures 1 – 6, when the packaging design needs a buildup stack and electrolytic plating process.

One such embodiment is illustrated and described based on Figures 8A – 8K, which illustrates cross-sectional views (and a corresponding plan view as shown in Figure 8D) of a package layer used to form the ZM2VS. In the illustrated embodiments, the formation of the ZM2VS is shown, however it is to be appreciated that additional features, such as additional lines, vias, and/or pads, may be formed at the same time and with the same processing operations, according to the embodiments described herein.

Referring now to Figure 8A, embodiments of the process flow include a package layer that includes, but is not limited to, a conductive layer 830, a dielectric layer 815, a seed layer 835, a first resist layer 825, a second resist layer 826, and a mask 880. For one embodiment, the dielectric layer 815 is deposited above and around the conductive layer 830 (or an initial top metal layer). For one embodiment, the package layer of Figure 8A illustrates at least one interconnect layer that has the conductive layer 830 and the dielectric layer 815. According to one embodiment, the conductive layer 830 includes existing pads, vias, and/or traces. In one embodiment, the dielectric layer 815 may be a BF layer.

According to some embodiments, several of the advantages of using a BF are its improved mechanical properties (*e.g.*, as compared for example to a PID), which enable (i) a lower coefficient of thermal expansion (CTE) ranging, for example, from 3-30 ppm/°C, and (ii) a higher modulus than PID materials. In addition, BF materials facilitate a lowered total cost as compared to other dielectric materials. Meanwhile, the formation of a BF layer may require a physical removal method, such as RIE, inductively coupled plasma (ICP) RIE, or other plasma etch processes, which may be used on next-generation panel-level processing (or a panel process line).

For some embodiments, the dielectric layer 815 may be a polymer material, such as a polyimide, an epoxy or a BF. In one embodiment, the dielectric layer 815 may be one layer in a stack that includes a plurality of dielectric layers used to form a build-up structure. As such, the dielectric layer 815 may be formed over another dielectric layer. Additional embodiments may include forming the dielectric layer 815 as the first dielectric layer over, for example, a core material on which the stack is formed.

According to some embodiments, the seed layer 835 is deposited on the dielectric layer 815. The seed layer 835 may not be transparent to any light, for example, from any light source of any lithography exposure tool. The seed layer 835 may include, but is not limited to, electroless deposited Cu, and/or sputtered Cu, Ti/Cu, Ta/Cu, tungsten (W)/Cu, and the like, such as, where Ti, Ta, W may facilitate the adhesion layers as well as barriers. Note that, based on the process flow described in Figures 8A – 8K, the seed layer 835 uses an electrolytic plating process to be deposited on the dielectric layer 815. According to an additional embodiment, the seed layer 835 may include a palladium (Pd) seed materials/clusters/layers (*e.g.*, the seed layer at certain location may be less than roughly one or a few atomic layers thick, for example, less than 10 atomic layers thick).

For one embodiment, the first resist layer 825 is deposited on the seed layer 835, while the second resist layer 826 is deposited/stacked above the first resist layer 826. For example, the first and second resist layers 825-826 may be laminated when using a dry resist material or slit-coated when using a liquid resist material. For one embodiment, the first and second resist layers 825-826 may include negative-tone dry film resist materials. In addition, the first and second resist layers 825-826 may be deposited in liquid form (and then dry-baked), and the resist layers 825-826 may also be positive-tone. Note, however, that both the first and second resist layers 825-826 may need to be of the same tone.

According to one embodiment, the second resist layer 826 is thinner (or has a smaller *z*-height) than the first resist layer 825 (*i.e.*, the second resist layer 826 aims to be as thin as possible), while the first resist layer 825 has a thickness that allows for plating of trace and via thickness and accommodates plating variation (*e.g.*, based on the desired design/application the thickness may be as low as 4  $\mu\text{m}$  and as high as 50  $\mu\text{m}$ ). For another embodiment, when using negative-tone resists, the second resist layer 826 has a low dose sensitivity (*e.g.*, a dose sensitivity of 10  $\text{mJ}/\text{cm}^2$  – 150  $\text{mJ}/\text{cm}^2$ ), and the first resist layer 825 has a high dose sensitivity (*e.g.*, a dose sensitivity of 20  $\text{mJ}/\text{cm}^2$  – 450  $\text{mJ}/\text{cm}^2$ ). As such, based on this embodiment, the second resist layer 826 has a lower dose sensitivity than the first resist layer 825. Note that, when using positive-tone resists, the resist layers may have the opposite dose sensitivity configuration (as compared to the negative-tone resist layers).

According to some embodiments, each of the first and second resist layers 825-826 has a dose-selective resist layer that can be chemically amplified. Furthermore, the stacked resist layers 825-826 are exposed using the mask 880 (*e.g.*, a grayscale mask) that has one or more intensity regions 881-882 (note that the mask can be implemented with a specified number of intensity regions based on the desired packaging design and/or the desired patterning for a ZM2VS trace/via).

For example, the one or more intensity regions 881-882 of the mask 780 may include one or more regions, such as a gray region 881, and one or more dark regions 882 (shown as dark blocks on the mask 880), where for example the one or more regions may be used to expose and develop resists layers to have one or more different dose sensitivities (*e.g.*, developable, not developable, etc.). Accordingly, after the mask 880 is exposed onto the first and second resist layer 825-826, one or more dose levels 825a and 826a-b may be printed (or developed) on the first resist layer 825 and the second resist layer 826, respectively, where each of the dose levels 825a and 826a-b may have an individual development-time requirement based on the level of exposure. After the exposure of the mask 880 on the resist layers 825-826, the resist layer 825 may be printed with a first region 825a, where the first region 825a may have a slower development time as compared to the regions of resist layer 825 that are adjacent to the region 825a, which may have been exposed to the intensity regions 882 of the mask 880. Meanwhile, the resist layer 826 may be printed with one or more first regions 826a, where the first regions 826a may have a faster development time as compared to the second region 825b (*e.g.*, region 826b may be selected as a non-developable region).

Referring now to Figure 8B, a first develop step may be exposed on the first and second resist layers 825-826 to remove only the resist regions that are developable (*e.g.*, regions 826a and regions below those respective regions). As such, after the first develop exposure on the first and second resist layers 825-826, the one or more developable resist regions are removed/developed from the first and second resist layers 825-826, and thus the resist layers 825-826 are patterned to provide one or more openings to expose one or more portions of the seed layer 835.

For one embodiment, after development, the one or more different dose sensitivities (as indicated in Figure 8B of the negative-tone resists layers 825-826) of the resist regions 825a and 826a-b may assure a specified profile and structure of the first and second resist layers 825-826 (*i.e.*, as shown with the openings/structures developed on the resist layers). Note that this development can be a single step when both resists use the same developer, or a two-step when the resists use different development chemistries. Also note that the resist region 825a of the first resist layer 825 may be developed, for example, but may not be developed on the portion where the conductive trace (*e.g.*, trace 810) will be disposed.

Referring now to Figure 8C, a third resist layer 827 is deposited above and around the one or more openings of the first and second resist layers 825-826. The third resist layer 827 is further exposed and developed (as illustrated in Figure 8D). For one embodiment, the third resist layer 827 covers the one or more openings (*e.g.*, via openings 840 of Figures 8D and E) that may be used to form the ZM2VS vias to connect to the layer(s) above the conductive layer 830. The

third resist layer 827 can be at least one of a positive-tone resist and a negative-tone resist.

According to one embodiment, the third resist layer 827 may have a sensitivity to a different wavelength (*i.e.*, a different sensitivity than the sensitivities of the first and second resist layers). For example, the first and second resist layers 825-826 may typically be i-line sensitive (or sensitive to the lowest wavelength that may be available by the exposure tool/mask), while the third resist layer 827 may be sensitive to a longer wavelength such as H-line or G-line. Note that a majority of the panel-level exposure tools are capable of, or can be upgraded to, expose using different wavelengths from their light source (*e.g.*, usually mercury arc).

Referring now to Figure 8D, a cross-section view of the package layer on the A – A' axis and a corresponding top view of the package layer are shown. As illustrated by the cross-sectional view (on the left), the third resist layer 827 has been exposed and developed to form an opening 840 on both of the first and second resist layer 825-826 that exposes a portion of the seed layer 835. Meanwhile, as illustrated by the top-view (on the right), the third resist layer 827 has been exposed and develop to expose the opening 840 and the resist layer 826 (*e.g.*, a varying portion of the resist region 826a may be exposed or may remain covered based on the desired design), where the third resist layer 827 is now only covering one of the via openings.

Referring now to Figure 8E, the exposed portion of the seed layer 835 in the opening 840 is then etched. According to one embodiment, the exposed portion of the seed layer 835 may be removed with a seed etching process. Furthermore, after the exposed seed layer 835 is etched, the via opening 840 is etched into the dielectric layer 815 with RIE or other physical etching methods to expose the top surface of the conductive layer 830.

Referring now to Figure 8F, the third resist layer 827 is exposed and developed to pattern via opening 840 and expose a portion of the seed layer 835. For one embodiment, the third resist layer 827 is removed with a resist stripping chemistry (or other removal processes). As such, after the third resist layer 827 is removed, the resist region 826b and the remaining second resist layer 826 is removed and accordingly, the previously patterned first resist layer 825 is also removed to provide one or more via openings 840 for the formation of one or more ZM2VS vias (*e.g.*, ZM2VS vias 811-812 as shown in Figure 8G). In one embodiment, the second resist layer 826 may be removed at the same time as the third resist layer 827 (*i.e.*, both resist layers removed in one step) or with an additional wet or dry-ash removal process/step.

Referring now to Figure 8G, a second seed layer 836 may be deposited on both of the via openings 840. For example, the second seed layer 836 is deposited on the exposed top surface of the conductive layer 830 and the exposed portion of the seed layer 835. For one embodiment, the second seed layer is a Pd seed layer and/or any other catalytic metal(s) that may be similar to a

Pd material(s). Accordingly, a conductive material (*e.g.*, Cu or the like) is deposited (disposed or grown-on) the via openings 840 and above the second seed layers 836 to form one or more ZM2VS vias 811 and 812. For one embodiment, the ZM2VS vias 811-812 may be formed with an e-less plating process or the like and electrically coupled to the first seed layer 835. Note that  
5 a second seed layer may not be needed to electrolytically plate metal simultaneously and directly on both conductive layers 830 and 835.

Referring now to Figure 8H, a second develop step is exposed on the first resist layer 825 to remove the resist region 825a. As such, after the second develop process step of the first resist layer 825, the resist region 825a is developed out from the resist layer 825, leaving a line  
10 opening 850 to expose a portion of the first seed layer 835 for the formation of a ZM2VS line/trace (*e.g.*, ZM2VS line 810 as shown in Figure 8I).

Referring now to Figure 8I, the conductive material is deposited above and around the line opening 850 and the ZM2VS vias 811-812 to form the ZM2VS line 810. For one embodiment, the ZM2VS line 810 is plated with an electrolytic plating (or electroplate) process  
15 using the first seed layer 835. After disposing the conductive material, the ZM2VS top via 811 is now finalized. Note that the top via 811 may have a slanted edge (or similar tapered shape) coupled to the line 810.

Referring now to Figure 8J, the first resist layer 825 is removed and then the exposed portions of the first seed layer 835 are etched. According to one embodiment, the first seed layer  
20 835 may be removed with a seed etching process. For one embodiment, the ZM2VS line/vias 810-812 are formed prior to the formation of a second dielectric layer.

As such, after the removal, the package layer has formed the ZM2VS line via using electrolytic plating and a buildup stack with a grayscale mask, as described herein. For some embodiments, the ZM2VS line via includes a dielectric 815 (*e.g.*, the BF layer) on a conductive  
25 pad 830, a first via 812 extends vertically through the dielectric 815 to a first seed layer 836 (*e.g.*, the Pd seed layer deposited on the exposed conductive pad) on a top surface of the conductive pad 830, a conductive trace 810 on the dielectric 815, and a second via 811 on a second seed layer 836, the second seed layer 836 is on/above the dielectric 815, where the conductive trace 810 electrically couples to the first via 812 and the second via 811, and where  
30 the second via 811 electrically couples to an edge of the conductive trace 810 that is opposite from the first via 812. Accordingly, the conductive trace 810 may connect to both a top layer (not shown) with the top via 811 and a bottom layer (or the conductive pad 830) with the bottom via 812 without reducing the line density of the line/vias 810-812 (*i.e.*, the conductive trace 810 can be connected to the zero-misaligned vias 811-812 in both directions (above and/or below the  
35 conductive trace 810)).

Referring now to Figure 8K, a second dielectric layer 816 is deposited over the exposed ZM2VS vias 811-812 and ZM2VS conductive trace 810. For one embodiment, the second dielectric layer 816 (*e.g.*, a BF layer) may be formed with any suitable process, such as lamination, spray or spin coating and curing. For one embodiment, the second dielectric layer 816 is formed to a thickness that may entirely cover a top surface 821 of the ZM2VS via 811. For example, as opposed to layer formation on crystalline structures (*e.g.*, silicon substrates), each of the dielectric layers may not be highly uniform. Accordingly, the second dielectric layer 816 may be formed to a thickness that is greater than the ZM2VS via 811 to ensure that the proper thickness is reached across the entire substrate. When the second dielectric layer 816 is formed above the ZM2VS via 811, a via reveal process (or a controlled etching process) may be used to expose the top surface 821 of the via 811, as illustrated in Figure 8K. The via reveal process may include mechanical or chemical-mechanical polishing/removing.

In one embodiment, the dielectric removal process may include a wet etch, a dry etch (*e.g.*, a plasma etch), a wet blast, or a laser ablation (*e.g.*, by using excimer laser). According to one additional embodiment, the depth controlled dielectric removal process may be performed only proximate to the ZM2VS via 811. For example, laser ablation of the second dielectric layer 816 may be localized proximate to the location of the via 811. In some embodiments, the thickness of the second dielectric layer 816 may be minimized in order to reduce the etching time required to expose the via 811. In alternative embodiments, when the thickness of the dielectric can be well controlled, the via 811 may extend above the top surface of the second dielectric layer 816 and the controlled dielectric removal process may be omitted.

Note that the zero-misalignment two via stack formed with the process flow of Figures 8A – 8K may include fewer or additional steps and/or packaging components based on the desired packaging design.

Figures 9A – 9H are a process flow illustrating a method of forming a zero-misalignment two via stack (ZM2VS) using a dose selective resist, a BF layer, and electrolytic plating, according to some embodiments. These embodiments as shown with respect to Figures 9A – 9H provide an additional process flow that implements dose selective resist and multiple development passes with a multi-tone mask (*e.g.*, mask 980 as shown in Figure 9A). One of the advantages of this process flow is that it simplifies the manufacturing process by using a dose-selective resist that can be chemically amplified and is typically positive-tone (note that the resist may also be a negative-tone). This allows for less assembly steps, including a single exposure, a single development, and a resist removal chemistry.

These embodiments as shown with respect to Figures 9A – 9H provide an additional patterning step to develop a ZM2VS stack, as described herein. The ZM2VS formed with the

process flow of Figures 9A – 9H is similar to the ZM2VS conductive traces/vias illustrated in Figures 1 – 6. One such embodiment is illustrated and described based on Figures 9A – 9H, which illustrates cross-sectional views of a package layer used to form the ZM2VS. In the illustrated embodiments, the formation of the ZM2VS is shown, however it is to be appreciated that additional features, such as additional lines, vias, and/or pads, may be formed at the same time and with the same processing operations, according to the embodiments described herein.

Referring now to Figure 9A, embodiments of the process flow include a dielectric layer 915 is deposited on a conductive layer 930, where the conductive layer 930 has one or more pads surrounded by the dielectric layer 915. In one embodiment, the dielectric layer 915 may be a BF layer. For one embodiment, the dielectric layer 915 may be one layer in a stack that includes a plurality of dielectric layers used to form a build-up structure. As such, the dielectric layer 915 may be formed over another dielectric layer. Additional embodiments may include forming the dielectric layer 915 as the first dielectric layer over, for example, a core material on which the stack is formed.

According to some embodiments, a seed layer 935 is deposited on the dielectric layer 915. For one embodiment, the seed layer 935 may not be transparent to any light, for example, from any light source of any lithography exposure tool. The seed layer 935 may include, but is not limited to, e-less deposited Cu, and/or sputtered Cu, Ti/Cu, Ta/Cu, tungsten (W)/Cu, and the like, such as, where Ti, Ta, W may facilitate the adhesion layers as well as barriers. For another embodiment, the seed layer 935 may use an electrolytic plating process to be deposited on the dielectric layer 915, and may include Pd seed materials/layers.

For some embodiments, a resist layer 925 is deposited on the seed layer 935. For example, the resist layer 925 may be laminated when using a dry resist material or slit-coated when using a liquid resist material. For one embodiment, the resist layer 925 is a dose-selective resist layer that can be chemically amplified. For additional embodiments, the resist layer 925 may be positive tone, but may also be negative tone. As such, the resist layer 925 may be exposed with a mask 980 (*e.g.*, a multi-tone mask with four regions) that has one or more intensity regions 981-983.

For example, the one or more intensity regions 981-983 of the mask 980 may include four intensity regions, such as a dark region (shown as dark blocks on the mask 980), a light region 981, a first gray region 982, and a second gray region 983, where for example the second gray region 983 may be darker (and thus allows less light exposure) than the first gray region 982. Accordingly, after the mask 980 is exposed on the resist layer 925, one or more dose levels 925a-c may be developed on the resist layer 925, where each of the dose levels 925a-c has an individual development-time requirement based on the level of exposure. After the exposure of

the mask 980 on the resist layer 925, the resist layer 925 is now printed with a first region 925a that has a highest dose and a faster/shorter development time, a second region 925b that has a medium dose and a slower development time, and a third region 925c that has a lowest dose and a slowest development time. Note that the unexposed regions of the resist layer are labelled 925,  
5 *e.g.*, the unexposed regions are on opposite ends/edges of the resist layer 925 as shown in one embodiment.

Referring now to Figure 9B, for one embodiment, a first develop step (or a fast development step) is exposed on the resist layer 925 to remove only the resist region exposed with the highest dose. As such, after the first develop exposure on the resist layer 925, the first  
10 region 925a is removed from the resist layer 925, where the resist layer 925 is thus patterned to provide an opening to expose a portion of the seed layer 935 for the formation of a ZM2VS via (*e.g.*, ZM2VS via 912 as shown in Figure 9E).

Referring now to Figure 9C, the exposed portion of the seed layer 935 is then etched and thus subsequently exposing a portion of the dielectric layer 915. According to one embodiment,  
15 the exposed portion of the seed layer 935 is removed with a seed etching process, and then the dielectric layer 915 is removed with RIE (or a similar removal process). Accordingly, after the removal of the seed layer 935, the exposed region of the dielectric layer 915 is removed and patterned to provide a via opening 940 that exposes a top surface of the conductive layer 930. For one embodiment, the dielectric layer 915 forms the bottom via opening 940 to the existing  
20 conductive layer 930.

Referring now to Figure 9D, a second develop step (or a slower development step) is exposed on the resist layer 925 to remove only the resist region exposed with the medium dose. As such, after the first develop exposure on the resist layer 925, the first region 925b is removed from the resist layer 925, where the resist layer 925 is thus patterned to provide an opening to  
25 expose a portion of the seed layer 935 for the formation of a ZM2VS via (*e.g.*, ZM2VS via 911 as shown in Figure 9E).

Referring now to Figure 9E, a second seed layer 936 may be deposited on both of the via openings 940. For example, the second seed layer 936 is deposited on the exposed top surface of the conductive layer 930 and the exposed portion of the seed layer 935. For one embodiment, the  
30 second seed layer is a Pd seed layer and/or any other catalytic metals/materials. Accordingly, a conductive material (*e.g.*, Cu or the like) is deposited on the via openings 940 and above the second seed layers 936 to form one or more ZM2VS vias 911 and 912. For one embodiment, the ZM2VS vias 911-912 may be formed/plated using an e-less plating process and electrically coupled to the first seed layer 935. Note that a second seed layer may not be needed to  
35 electrolytically plate metal simultaneously and directly on both conductive layers 930 and 935.

Referring now to Figure 9F, a third develop step (or a slowest development step) is exposed on the resist layer 925 to remove the resist region exposed with the lowest dose. As such, after the third develop exposure on the resist layer 925, the third region 925c is removed from the resist layer 925, and thus the resist layer 925 is patterned to provide a line opening 950 to expose a portion of the seed layer 935 for the formation of a ZM2VS line/trace (e.g., ZM2VS line 910 as shown in Figure 9G). For example, after the e-less plating step of the ZM2VS vias 911-912, the third region 925c is developed away to expose the ZM2VS vias 911-912 and the seed layer 935.

Referring now to Figure 9G, the conductive material is deposited above and around the line opening 950 and the ZM2VS vias 911-912 to form the ZM2VS line 910. After disposing the conductive material, the ZM2VS top via 911 is now finalized. For one embodiment, the ZM2VS line 910 may be formed using the electrolytic plating process. Note that the top via 911 may have a slanted edge (or similar tapered shape) coupled to the line 910. Referring now to Figure 9H, the resist layer 925 is stripped and the remaining portions of the seed layer 935 are removed. For one embodiment, the ZM2VS line/vias 910-912 are formed prior to the formation of a second dielectric layer.

As such, after the removal, the package layer has formed the ZM2VS line via using electrolytic plating and a buildup stack with a multi-tone mask, as described herein. For some embodiments, the ZM2VS line via includes a dielectric 915 (e.g., the BF layer) on a conductive pad 930, a first via 912 extends vertically through the dielectric 915 to a first seed layer 936 on a top surface of the conductive pad 930, a conductive trace 910 on the dielectric 915, and a second via 911 on a second seed layer 936, the second seed layer 936 is on/above the dielectric 915, where the conductive trace 910 electrically couples to the first via 912 and the second via 911, and where the second via 911 electrically couples to an edge of the conductive trace 910 that is opposite from the first via 912. Accordingly, the conductive trace 910 may connect to both a top layer (not shown) with the top via 911 and a bottom layer (or the conductive pad 930) with the bottom via 912 without reducing the line density of the line/vias 910-912 (i.e., the conductive trace 910 can be connected to the zero-misaligned vias 911-912 in both directions (above and/or below the conductive trace 910)).

According to additional embodiments, a second dielectric layer may be deposited over the exposed ZM2VS vias 911-912 and ZM2VS conductive trace 910. For the additional embodiments, when the second dielectric layer is formed above the ZM2VS via 911, a via reveal process (or a controlled etching process) may be used to expose a top surface of the via 911.

Note that the zero-misalignment two via stack formed with the process flow of Figures 9A – 9H may include fewer or additional steps and/or packaging components based on the

desired packaging design.

Figures 10A – 10I are a process flow illustrating a method of forming a conductive trace with zero-misaligned transmission vias using a PID film stack with electrolytic (e-lytic) plating on a transparent substrate, according to some embodiments. These embodiments as shown with  
5 respect to Figures 10A – 10I provide an e-lytic process to form a free standing ZM2VS that may use a positive-tone resist and dielectric combination on a carrier substrate, such as a transparent substrate (*e.g.*, a glass carrier, a polyethylene terephthalate (PET), a dielectric film/layer, an organic transparent material, and/or any other transparent material).

Figures 10A – 10I illustrate an additional process flow that implements dose-selective  
10 resist and multiple development passes with a multi-tone mask (*e.g.*, mask 1080 as shown in Figure 10B). Some of the advantages of this process flow is that it enables a single lithographic exposure step along with several development and plating steps. In particular, these embodiments are compatible with transparent carriers/substrates which allows the implemented/assembled ZM2VS stack to be fully laminated (or transferred) onto any substrate.  
15 As such, these embodiments (i) enable a process flow of a zero-misalignment to via stack using a single lithography exposure step (*e.g.*, using a single exposure step with a well-designed grayscale mask), but also further enable (ii) the process flow to be compatible as a free standing stack (or film) that is compatible with transparent carriers, substrates, and/or flexible materials. The ZM2VS formed with the process flow of Figures 10A – 10I is similar to the ZM2VS  
20 conductive traces/vias illustrated in Figures 1 – 6. One such embodiment is illustrated and described based on Figures 10A – 10I, which illustrates cross-sectional views of a package layer used to form the ZM2VS. In the illustrated embodiments, the formation of the ZM2VS is shown, however it is to be appreciated that additional features, such as additional lines, vias, and/or pads, may be formed at the same time and with the same processing operations, according to the  
25 embodiments described herein.

Referring now to Figure 10A, according to some embodiments, a conductive layer 1030 is deposited on a substrate 1001a. For one embodiment, the substrate 1001a (or a bottom substrate) may include, but is not limited to, a carrier substrate, a transparent substrate, a glass carrier, a PET, a polydimethylsiloxane (PDMS), a dielectric layer, an organic transparent  
30 material, and/or any other transparent material. Additionally, for one embodiment, a PID layer 1015 is deposited above and around a conductive layer 1030, and then a seed layer 1035 is deposited on the PID layer 1015. For one embodiment, the PID layer 1015 may be deposited with a lamination, spray coating, spin coating, or other known deposition methods. The conductive layer 1030 may include one or more pads (or vias/lines) surrounded by the PID layer  
35 1015.

For one embodiment, the seed layer 1035 may not be transparent to any light, for example, from any light source of any lithography exposure tool. The seed layer 1035 may include, electroless deposited Cu, and/or sputtered Cu, Ti/Cu, Ta/Cu, tungsten (W)/Cu, and the like. For one embodiment, the seed layer 1035 may use an electrolytic plating process to be deposited on the PID layer 1015, and/or may be deposited on the PID layer 1015 using standard deposition methods.

For some embodiments, a resist layer 1025 is deposited on the seed layer 1035. For example, the resist layer 1035 may be laminated when using a dry resist material or slit-coated when using a liquid resist material. For one embodiment, the resist layer 1025 is a dose-selective resist layer that can be chemically amplified. For additional embodiments, the resist layer 1025 may be positive tone, but may also be negative tone. Furthermore, a substrate 1001b (or a top substrate) is deposited on the resist layer 1025, where the substrate 1001b may include, but is not limited to, a carrier substrate, a transparent substrate, a glass carrier, a PET, a PDMS, a dielectric layer, an organic transparent material, and/or any other transparent material.

Referring now to Figure 10B, the resist layer 1025 may be exposed with a mask 1080 (*e.g.*, a multi-tone mask with four regions) that has one or more intensity regions 1081-1083 (note that the transparent substrate 1001b does not interfere with the exposure of the mask 1080). For example, the one or more intensity regions 1081-1083 of the mask 1080 may include four intensity regions, such as a dark region (shown as dark blocks on the mask 1080), a light region 1081, a first gray region 1082, and a second gray region 1083, where for example the second gray region 1083 may be darker (and thus allows less light exposure) than the first gray region 1082. Accordingly, after the mask 1080 is exposed on the resist layer 1025, one or more dose levels 1025a-c may be developed on the resist layer 1025, where each of the dose levels 1025a-c has an individual development-time requirement based on the level of exposure.

After the simultaneous, selective exposure of the mask 1080 on the resist layer 1025, the resist layer 1025 is now printed with a first region 1025a that has a highest dose and a faster/shorter development time, a second region 1025b that has a medium dose and a slower development time, and a third region 1025c that has a lowest dose and a slowest development time. Note that the unexposed regions of the resist layer are labelled 1025, *e.g.*, the unexposed regions are on opposite ends/edges of the resist layer 1025 as shown in one embodiment.

Referring now to Figure 10C, once the resist layer 1025 has been selectively exposed with the mask 1080, the substrate 1001b may be removed. In addition, a first develop step is exposed on the resist layer 1025 to remove only the resist region exposed with the highest dose (*i.e.*, with minimal impact to the other exposed regions). As such, after the first develop exposure on the resist layer 1025, the first region 1025a is removed from the resist layer 1025, where the

resist layer 1025 is thus patterned to provide an opening to expose a portion of the seed layer 1035 for the formation of a ZM2VS via (e.g., ZM2VS via 1012 as shown in Figure 10F).

Referring now to Figure 10D, the exposed portion of the seed layer 1035 is then etched and thus subsequently exposing a portion of the dielectric layer 1015. According to one  
5 embodiment, the exposed portion of the seed layer 1035 is removed with a seed etching process, and thus the removed exposed portion of the seed layer 1035 can now be used as a mask to pattern the exposed region of the underlining PID layer 1015.

Referring now to Figure 10E, a flood exposure is implemented on the resist layer 1025 and the exposed region of the PID layer 1015. For another embodiment, the flood exposure may  
10 use an intransparent seed as a mask (not shown) to expose only the portion of the PID layer 1015, where the seed layer 1035 has been removed. For example, in order to avoid further exposure of the resist layer 1025 as the PID layer 1015 is exposed, the PID layer 1015 may need to be either a lot more sensitive than the resist layer 1025 (i.e., requiring a very low dose to become developable) or sensitive to another wavelength.

After the flood exposure, the exposed region of the PID layer 1015 is developed (or  
15 patterned) to provide a via opening 1040 that exposes a top surface of the conductive layer 1030. For one embodiment, the developed region of the PID layer 1015 forms the bottom via opening 1040 to the existing conductive layer 1030, where the PID layer 1015 may be selectively triggered through dose, wavelength, or other means. For example, the PID layer 1015 may only  
20 be exposed when a specified dose or wavelength is achieved, while the resist layer 1025 is not impacted by the additional flood exposure. Continuing with the above example, the PID layer 1015 may be triggered at  $< 10 \text{ mJ/cm}^2$ , but the previously exposed medium/low dose regions 1025b-c of the resist layer 1025, in particular, may only be triggered above  $>>> 10 \text{ mJ/cm}^2$  (i.e., the remaining dose regions of the resist layer 1025 may not be impacted/affected by the flood  
25 exposure step of the PID layer 1015). Note, this is an example and the dose is not limited to  $10 \text{ mJ/cm}^2$ , but may illustrate the need for a difference in doses between the photoresist layer 1025 and PID layer 1015.

For one embodiment, a second develop step is exposed on the resist layer 1025 to remove the resist region exposed with the medium dose (or 2nd highest dose). As such, after the second  
30 develop exposure on the resist layer 1025, the second region 1025b is removed from the resist layer 1025, and thus the resist layer 1025 is patterned to provide a via opening 1040 to expose a portion of the seed layer 1035 for the formation of a ZM2VS via (e.g., ZM2VS via 1011 as shown in Figure 10F).

Referring now to Figure 10, a second seed layer 1036 may be deposited on both of the  
35 via openings 1040. For example, the second seed layer 936 is deposited on the exposed top

surface of the conductive layer 1040 and the exposed portion of the seed layer 935. For one embodiment, the second seed layer is a Pd seed layer and/or any other catalytic metals/materials. Accordingly, a conductive material (*e.g.*, Cu or the like) is deposited on the via openings 1040 and above the second seed layers 1036 to form one or more ZM2VS vias 1011 and 1012. For one embodiment, the ZM2VS vias 1011-1012 may be formed/plated using an e-less plating process and electrically coupled to the first seed layer 935. Note that a second seed layer may not be needed to electrolytically plate metal simultaneously and directly on both conductive layers 930 and 935.

Referring now to Figure 10F, a conductive material (*e.g.*, Cu or the like) is grown on the via openings 1040 to form one or more ZM2VS vias 1011 and 1012 through an electrochemical reaction. For example, the conductive material is deposited on the exposed top surface of the conductive layer 1030 to form the bottom ZM2VS via 1012 and the exposed portion of the seed layer 1035 to form the top ZM2VS via 1011. For one embodiment, the ZM2VS vias 1011-1012 may be formed/plated using an e-less plating process and electrically coupled to the seed layer 1035. Note that the top surface of the bottom via 1012 may be deposited above and/or below the seed layer 1035 (or on the same level/layer as the seed layer 1035).

Referring now to Figure 10G, a third develop step is exposed on the resist layer 1025 to remove the resist region exposed with the lowest dose. As such, after the third develop exposure on the resist layer 1025, the third region 1025c is removed from the resist layer 1025, and thus the resist layer 1025 is patterned to provide a line opening 1050 to expose a portion of the seed layer 1035 for the formation of a ZM2VS line/trace (*e.g.*, ZM2VS line 1010 as shown in Figure 10H). For example, after the e-less plating step of the ZM2VS vias 1011-1012, the third region 1025c is developed away to expose the ZM2VS vias 1011-1012 and the seed layer 1035.

Referring now to Figure 10H, accordingly, the conductive material is deposited above and around the line opening 1050 and the ZM2VS vias 1011-1012 to form the ZM2VS line 1010. After disposing the conductive material, the ZM2VS top via 1011 is now finalized. For one embodiment, the ZM2VS line 1010 may be formed using the electrolytic plating process. Note that the top via 1011 (or the bottom via) may have a slanted edge (or similar tapered shape) coupled to the line 1010.

Referring now to Figure 10I, the resist layer 1025 is stripped and the remaining portions of the seed layer 1035 are removed. For one embodiment, the ZM2VS line/vias 1010-1012 are formed prior to the formation of, for example, a second dielectric layer. For another embodiment, the package layer shown with Figure 10I may be transferred onto one or more various substrates via lamination or other known method (not shown) based on the desired packaging design. For example, the one or more substrates may include patterned BFs, silicon,

fabric, printed circuit boards (PCBs), flexible electronics, and any other desired substrate.

As such, after the removal, the package layer has formed the ZM2VS line via using electrolytic plating on a transparent substrate/carrier and a PID film stack with a mask (*e.g.*, a multi-tone, grayscale mask), as described herein. For some embodiments, the ZM2VS line via includes a dielectric 1015 (*e.g.*, the PID layer) on a conductive pad 1030, a first via 1012 extends vertically through the dielectric 1015 to a first seed layer 1036 on a top surface of the conductive pad 1030, a conductive trace 1010 on the dielectric 1015, and a second via 1011 on a second seed layer 1036, the second seed layer 1036 is on/above the dielectric 1015, where the conductive trace 1010 electrically couples to the first via 1012 and the second via 1011, and where the second via 1011 electrically couples to an edge of the conductive trace 1010 that is opposite from the first via 1012. Accordingly, the conductive trace 1010 may connect to both a top layer (not shown) with the top via 1011 and a bottom layer (or the conductive pad 1030) with the bottom via 1012 without reducing the line density of the line/vias 1010-1012 (*i.e.*, the conductive trace 1010 can be connected to the zero-misaligned vias 1011-1012 in both directions (above and/or below the conductive trace 1010)).

According to additional embodiments, a second dielectric layer may be deposited over the exposed ZM2VS vias 1011-1012 and ZM2VS conductive trace 1010. For the additional embodiments, when the second dielectric layer is formed above the ZM2VS via 1011, a via reveal process (or a controlled etching process) may be used to expose a top surface of the via 1011, where the exposed top surface may be used to couple to the one or more substrates (if the ZM2VS is transferred onto another substrate).

Some of the advantages of the process flow of Figures 10A – 10I is that a single step exposure and patterning process is illustrated that combines a dose-selective patternable resist layer (or photoresist (PR) layer), a metal seed, a dielectric layer, and a transparent carrier to build a via-trace-via with zero-misalignment between trace and vias. As such, the illustrated process flow may eliminate litho tool-to-tool misalignment and further simplify overall litho process. In addition, the process improves overall cost-efficiency by achieving zero-misalignment to via stack. Likewise, the process flow enables incorporation into a number of packaging needs, including, but not limited to, increasing I/O density, improving redistribution layers, and incorporation into a variety of packaging designs.

Note that the zero-misalignment two via stack formed with the process flow of Figures 10A – 10I may include fewer or additional steps and/or packaging components based on the desired packaging design.

Figure 11 is a schematic block diagram illustrating a computer system that utilizes a device package with conductive traces with zero-misaligned transmission vias, as described

herein. Figure 11 illustrates an example of computing device 1100. Computing device 1100 houses motherboard 1102. Motherboard 1102 may include a number of components, including but not limited to processor 1104, device package 1110, and at least one communication chip 1106. Processor 1104 is physically and electrically coupled to motherboard 1102. For some  
5 embodiments, at least one communication chip 1106 is also physically and electrically coupled to motherboard 1102. For other embodiments, at least one communication chip 1106 is part of processor 1104.

Depending on its applications, computing device 1100 may include other components that may or may not be physically and electrically coupled to motherboard 1102. These other  
10 components include, but are not limited to, volatile memory (*e.g.*, DRAM), non-volatile memory (*e.g.*, ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk  
15 drive, compact disk (CD), digital versatile disk (DVD), and so forth).

At least one communication chip 1106 enables wireless communications for the transfer of data to and from computing device 1100. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-  
20 solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. At least one communication chip 1106 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G,  
25 and beyond. Computing device 1100 may include a plurality of communication chips 1106. For instance, a first communication chip 1106 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1106 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.  
30

Processor 1104 of computing device 1100 includes an integrated circuit die packaged within processor 1104. Device package 1110 may be, but is not limited to, a packaging substrate and/or a printed circuit board. Device package 1110 may include one or more ZM2VS lines/vias (as illustrated in Figures 1-10) of the computing device 1100.

35 Note that device package 1110 may be a single component, a subset of components,

and/or an entire system, as the ZM2VS lines/vias may be limited to device package 1110 and/or any other component that requires ZM2VS in the computing device 1100.

For some embodiments, the integrated circuit die may be packaged with one or more devices on device package 1110 that include a thermally stable RFIC and antenna for use with wireless communications. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

At least one communication chip 1106 also includes an integrated circuit die packaged within the communication chip 1106. For some embodiments, the integrated circuit die of the communication chip may be packaged with one or more devices on the device package 1110, as described herein.

The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications.

The following examples pertain to further embodiments:

Example 1 is device package, comprising a dielectric on a conductive pad; a first via on a first seed, the first seed on a top surface of the conductive pad, wherein the first via extends through the dielectric; a conductive trace on the dielectric; and a second via on a second seed layer, the second seed is on the dielectric. The conductive trace connects to the first via and the second via. The second via connects to an edge of the conductive trace that is opposite from the first via.

In example 2, the subject matter of example 1 can optionally include further comprising a seed on the dielectric prior to the conductive trace on the dielectric. The seed electrically couples to the conductive trace.

In example 3, the subject matter of any of examples 1-2 can optionally include the conductive trace which electrically couples to the first via and the second via.

In example 4, the subject matter of any of examples 1-3 can optionally include further comprising a second dielectric on the dielectric, the conductive trace, and the first and second vias. The second dielectric exposes a top surface of the second via.

In example 5, the subject matter of any of examples 1-4 can optionally include the dielectric which includes a photoimageable dielectric film or a buildup film.

In example 6, the subject matter of any of examples 1-5 can optionally include prior to the formation of the conductive trace, the first via, and the second via, further comprising a selective resist on the seed. The selective resist includes a positive-tone dry film resist material; and a mask with one or more intensity regions. The mask prints one or more dose regions on the

selective resist based on the one or more intensity regions of the mask.

In example 7, the subject matter of any of examples 1-6 can optionally include the one or more dose regions on the selective resist have one or more different development times that pattern the selective resist for the conductive trace and the first and second vias.

5 In example 8, the subject matter of any of examples 1-7 can optionally include the one or more different development times of the selective resist including a first development time on a first dose region, a second development time on a second dose region, and a third development time on a third dose region.

10 In example 9, the subject matter of any of examples 1-8 can optionally include that the first dose region is patterned to form the first via, the second dose region is patterned to form the second via, and the third dose region is patterned to form the conductive trace.

In example 10, the subject matter of any of examples 1-9 can optionally include the conductive trace, the first via, and the second via are electrolytically plated.

15 In example 11, the subject matter of any of examples 1-10 can optionally include that the conductive pad is on a transparent substrate.

In example 12, the subject matter of any of examples 1-11 can optionally include the transparent substrate which includes a glass carrier, a polyethylene terephthalate (PET), a dielectric film, a polydimethylsiloxane (PDMS), an organic transparent material, or one or more transparent materials.

20 In example 13, the subject matter of any of examples 1-12 can optionally include the conductive trace that has a line density that is substantially equal to a line density of the first via and a line density of the second via.

In example 14, the subject matter of any of examples 1-13 can optionally include prior to the formation of the conductive trace, the first via, and the second via, further comprising a first  
25 selective resist and a second selective resist on the seed. The second selective resist is on the first selective resist. The first and second selective resist include negative-tone dry resist materials.

In example 15, the subject matter of any of examples 1-14 can optionally include the stacked first and second selective resists patterned to form one or more openings on the seed. A third resist is deposited on the one or more openings and the second selective resist.

30 In example 16, the subject matter of any of examples 1-15 can optionally include the second selective resist and the third resist are removed and patterned to form one or more via openings for the first and second vias.

In example 17, the subject matter of any of examples 1-16 can optionally include the conductive pad on the transparent substrate transferred and electrically coupled to a second  
35 substrate.

Example 18 is a method of forming a device package, comprising disposing a dielectric on a conductive pad; disposing a first via on a first seed and the first seed on a top surface of the conductive pad. The first via extends through the dielectric; disposing a conductive trace on the dielectric; and disposing a second via on a second seed layer, the second seed is on the dielectric.

5       The conductive trace connects to the first via and the second via. The second via connects to an edge of the conductive trace that is opposite from the first via.

In example 19, the subject matter of example 18 can optionally include further comprising disposing a seed on the dielectric prior to the conductive trace on the dielectric. The seed electrically couples to the conductive trace.

10       In example 20, the subject matter of any of examples 18-19 can optionally include the conductive trace electrically coupled to the first via and the second via.

In example 21, the subject matter of any of examples 18-20 can optionally include further comprising disposing a second dielectric on the dielectric, the conductive trace, and the first and second vias. The second dielectric exposes a top surface of the second via.

15       In example 22, the subject matter of any of examples 18-21 can optionally include the dielectric which includes a photoimageable dielectric film or a buildup film.

In example 23, the subject matter of any of examples 18-22 can optionally include prior to the formation of the conductive trace, the first via, and the second via, further comprising disposing a selective resist on the seed. The selective resist includes a positive-tone dry film resist material; and exposing a mask with one or more intensity regions on the selective resist. The mask prints one or more dose regions on the selective resist based on the one or more intensity regions of the mask.

20       In example 24, the subject matter of any of examples 18-23 can optionally include the one or more dose regions on the selective resist have one or more different development times that pattern the selective resist for the conductive trace and the first and second vias.

In example 25, the subject matter of any of examples 18-24 can optionally include the one or more different development times of the selective resist which include a first development time on a first dose region, a second development time on a second dose region, and a third development time on a third dose region.

30       In example 26, the subject matter of any of examples 18-25 can optionally include the first dose region patterned to form the first via, the second dose region patterned to form the second via, and the third dose region patterned to form the conductive trace.

In example 27, the subject matter of any of examples 18-26 can optionally include that the conductive trace, the first via, and the second via are electrolytically plated.

35       In example 28, the subject matter of any of examples 18-27 can optionally include that

the conductive pad is on a transparent substrate.

In example 29, the subject matter of any of examples 18-28 can optionally include the transparent substrate includes a glass carrier, a PET, a dielectric film, a PDMS, an organic transparent material, or one or more transparent materials.

5 In example 30, the subject matter of any of examples 18-29 can optionally include the conductive trace has a line density that is substantially equal to a line density of the first via and a line density of the second via.

10 In example 31, the subject matter of any of examples 18-30 can optionally include prior to the formation of the conductive trace, the first via, and the second via, further comprising disposing a first selective resist and a second selective resist on the seed. The second selective resist is on the first selective resist. The first and second selective resist include negative-tone dry resist materials.

In example 32, the subject matter of any of examples 18-31 can optionally include the stacked first and second selective resists are patterned to form one or more openings on the seed.  
15 A third resist is deposited on the one or more openings and the second selective resist.

In example 33, the subject matter of any of examples 18-32 can optionally include the second selective resist and the third resist are removed and patterned to form one or more via openings for the first and second vias.

20 In example 34, the subject matter of any of examples 18-33 can optionally include the conductive pad on the transparent substrate transferred and electrically coupled to a second substrate.

Example 35 is a device package, comprising a dielectric on a conductive pad; a first via on a first seed and the first seed on a top surface of the conductive pad. The first via extends through the dielectric; a conductive trace on the dielectric; a second via on a second seed layer and the second seed is on the dielectric. The conductive trace connects to the first via and the second via. The second via connects to an edge of the conductive trace that is opposite from the first via; a die on a first-level interconnect (FLI) pad. The FLI pad connects to the second via; and an interconnect package layer on a second-level interconnect (SLI) pad. The SLI pad connects to the first via.

30 In example 36, the subject matter of example 35 can optionally include further comprising one or more conductive traces having one or more first vias and one or more second vias, and the interconnect package layer having one or more interconnect package layers stacked on each other. The one or more package layers connect to the one or more conductive traces, first vias, and second vias.

35 In example 37, the subject matter of any of examples 35-36 can optionally include further

comprising a seed on the dielectric prior to the conductive trace on the dielectric. The seed electrically couples to the conductive trace.

In example 38, the subject matter of any of examples 35-37 can optionally include the conductive trace electrically couples to the first via and the second via.

- 5 In example 39, the subject matter of any of examples 35-38 can optionally include further comprising a second dielectric on the dielectric, the conductive trace, and the first and second vias. The second dielectric exposes a top surface of the second via.

In example 40, the subject matter of any of examples 35-39 can optionally include the dielectric which includes a photoimageable dielectric film or a buildup film.

- 10 In example 41, the subject matter of any of examples 35-40 can optionally include prior to the formation of the conductive trace, the first via, and the second via, further comprising a selective resist on the seed. The selective resist includes a positive-tone dry film resist material; and a mask with one or more intensity regions. The mask prints one or more dose regions on the selective resist based on the one or more intensity regions of the mask.

- 15 In example 42, the subject matter of any of examples 35-41 can optionally include the one or more dose regions on the selective resist have one or more different development times that pattern the selective resist for the conductive trace and the first and second vias.

- In example 43, the subject matter of any of examples 35-42 can optionally include the one or more different development times of the selective resist which include a first development  
20 time on a first dose region, a second development time on a second dose region, and a third development time on a third dose region.

In example 44, the subject matter of any of examples 35-43 can optionally include the first dose region patterned to form the first via, the second dose region patterned to form the second via, and the third dose region patterned to form the conductive trace.

- 25 In example 45, the subject matter of any of examples 35-44 can optionally include the conductive trace, the first via, and the second via electrolytically plated.

In example 46, the subject matter of any of examples 35-45 can optionally include the conductive pad on a transparent substrate.

- In example 47, the subject matter of any of examples 35-46 can optionally include the  
30 transparent substrate which includes a glass carrier, a PET, a dielectric film, a PDMS, an organic transparent material, or one or more transparent materials.

In example 48, the subject matter of any of examples 35-47 can optionally include that the conductive trace has a line density that is substantially equal to a line density of the first via and a line density of the second via.

- 35 In example 49, the subject matter of any of examples 35-48 can optionally include prior

to the formation of the conductive trace, the first via, and the second via, further comprising a first selective resist and a second selective resist on the seed. The second selective resist is on the first selective resist. The first and second selective resist include negative-tone dry resist materials.

- 5           In example 50, the subject matter of any of examples 35-49 can optionally include the stacked first and second selective resists are patterned to form one or more openings on the seed. A third resist is deposited on the one or more openings and the second selective resist.

- In example 51, the subject matter of any of examples 35-50 can optionally include the second selective resist and the third resist are removed and patterned to form one or more via  
10 openings for the first and second vias.

          In example 52, the subject matter of any of examples 35-51 can optionally include the conductive pad on the transparent substrate is transferred and electrically coupled to a second substrate.

- In the foregoing specification, embodiments have been described with reference to  
15 specific exemplary embodiments thereof. It will be evident that various modifications may be made thereto without departing from the broader spirit and scope. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.