What is claimed:

1. A system, comprising:

a memory component; and

a processing device, operatively coupled to the memory component, to reduce a supply voltage sensitivity of an output current of a bias current generator circuit provided to the memory component, wherein the bias current generator circuit includes:

a plurality of transistors; and

a plurality of resistors coupled to the plurality of transistors, wherein:

a first one of the plurality of resistors is directly coupled to a source/drain region of a first one of the plurality of transistors and a source/drain region of a second one of the plurality of transistors;

a second one of the plurality of resistors is directly coupled to a source/drain region of a third one of the plurality of transistors and gates of both the second one of the plurality of transistors and a fourth one of the plurality of transistors; and

the first and third one of the plurality of transistors are directly coupled to ground; and

wherein the processing device is to reduce the supply voltage sensitivity of the output current of the bias current generator circuit by applying a second bias current generated by the bias current generator circuit to a first bias current generated by the bias current generator circuit.

2. The system of claim 1, wherein the first bias current is proportional to a supply voltage minus one diode drop.

3. The system of claim 1, wherein the second bias current is proportional to a supply voltage minus two diode drops.

4. The system of claim 1, wherein applying the second bias current to the first bias current reduces a variance of a magnitude of the first bias current.

5. The system of claim 1, wherein a magnitude of the output current of the bias current generator circuit is in a range of two percent (2%) greater than or less than an intended magnitude of the output current of the bias current generator circuit.

6. The system of claim 1, wherein a magnitude of the first bias current is greater than a magnitude of the second bias current.

7. The system of any one of claims 1-6, wherein the first and second bias currents are direct currents.

8. A system, comprising:

a memory component; and

bias current generator circuitry, including:

a plurality of transistors; and

a plurality of resistors coupled to the transistors, wherein:

a first one of the plurality of resistors is coupled to a source/drain region of a first one of the plurality of transistors and a source/drain region of a second one of the plurality of transistors;

a second one of the plurality of resistors is coupled to a source/drain region of a third one of the plurality of transistors and gates of both the second one of the plurality transistors and a fourth one of the plurality of transistors; and

the first and third one of the plurality of transistors are coupled to ground; and

wherein the bias current generator circuitry is to reduce a variance of a magnitude of an output current of the bias current generator circuitry provided to the memory component by generating a first bias current and a second bias current.

9. The system of claim 8, wherein the output current is generated by applying the second bias current to the first bias current.

10. The system of any one of claims 8-9, wherein the magnitude of the output current is closer to a magnitude of the second bias current than a magnitude of the first bias current.

11. The system of any one of claims 8-9, wherein:

the bias current generator circuitry is to generate the first bias current using the first one of the plurality of resistors; and

the bias current generator circuitry is to generate the second bias current using the second one of the plurality of resistors.

12. The system of claim 11, wherein the first and second one of the plurality of resistors are coupled in parallel.

13. A method, comprising:

reducing a supply voltage sensitivity of an output current of bias current generator circuitry by:

generating a first bias current using the bias current generator circuitry;

generating a second bias current using the bias current generator circuitry, wherein:

a first resistor of the bias current generator circuitry is coupled to a source/drain region of a first transistor of the bias current generator circuitry and a source/drain region of a second transistor of the bias current generator circuitry;

a second resistor of the bias current generator circuitry is coupled to a source/drain region of a third transistor of the bias current generator circuitry and gates of both the second transistor and a fourth transistor of the bias current generator circuitry; and

the first transistor and the third transistor are coupled to ground; and

applying the second bias current to the first bias current to reduce the supply induced common-mode bias current; and

providing the output current of the bias current generator circuitry to additional circuitry.

14. The method of claim 13, wherein the additional circuitry comprises comparison circuitry.

15. The method of any one of claims 13-14, further comprising providing the output current of the bias current generator circuitry to an input of a sense amplifier of the additional circuitry.

16. The method of claim 15, wherein the bias current generator circuitry couples the sense amplifier to ground.

17. The method of claim 15, wherein the bias current generator circuitry couples the sense amplifier to a source.

18. The method of any one of claims 13-14, further comprising providing the output current of the bias current generator circuitry to multiple separate circuits.